**VISVESVARAYA TECHNOLOGICAL UNIVERSITY**
**BELAGAVI**

Scheme of Teaching and Examinations and Syllabus
M.TechVLSI DESIGN & EMBEDDED SYSTEMS (EVE)
**(Effective from Academic year 2020 - 21)**

**M.TECH VLSI DESIGN & EMBEDDED SYSTEMS (EVE)**
**Choice Based Credit System (CBCS) and Outcome Based Education(OBE)**
**SEMESTER -I**

**ADVANCED ENGINEERING MATHEMATICS**

| | | | |
|---|---|---|---|
| Course Code | 20ELD11 | CIE Marks | 40 |
| TeachingHours/Week (L:T:P) | 4:0:0 | SEE Marks | 60 |
| Credits | 04 | Exam Hours | 03 |

**Module-1**

**Linear Algebra-I**
Introduction to vector spaces and sub-spaces, definitions, illustrative example. Linearly independent and dependent vectors- Basis-definition and problems. Linear transformations-definitions. Matrix form of linear transformations-Illustrative examples (Text Book:1).

**Module-2**

**Linear Algebra-II**
Computation of eigen values and eigen vectors of real symmetric matrices-Given's method. Orthogonal vectors and orthogonal bases. Gram-Schmidt orthogonalization process (Text. Book:1)

**Module-3**

**Calculus of Variations**
Concept of functional- Eulers equation. Functional dependent on first and higher order derivatives, Functional on several dependent variables. Isoperimetric problems-variation problems with moving boundaries. (Text.Book:2)

**Module-4**

**Probability Theory:** Review of basic probability theory. Definitions of random variables and probability distributions, probability mass and density functions, expectation, moments, central moments, characteristic functions, probability generating and moment generating functions-illustrations. Poisson, Gaussian and Erlang distributions examples. (Text Book: 3)

**Module-5**

**Engineering Applications on Random processes:** Classification. Stationary, WSS and ergodic random process. Auto-correlation function - properties, Gaussian random process. (Text Book: 3)

**Course outcomes:**
At the end of the course the student will be able to:
1. Understand vector spaces, basis, linear transformations and the process of obtaining matrix of linear transformations arising in magnification and rotation of images.
2. Apply the technique of singular value decomposition for data compression, least square approximation in solving inconsistent linear systems.
3. Utilize the concepts of functional and their variations in the applications of communication systems, decision theory, synthesis and optimization of digital circuits.
4. Learn the idea of random variables (discrete/continuous) and probability distributions in analyzing the probability models arising in control systems and system communications.
5. Analyze random process through parameter-dependent variables in various random processes.

**Question paper pattern:**
The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 60.
- The question paper will have ten full questions carrying equal marks.
- Each full question is for 20 marks.
- There will be two full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub question covering all the topics under a module.
- The students will have to answer five full questions, selecting one full question from each module.

**Textbook/ Textbooks**

| Sl No | Title of the book | Name of the Author/s | Publisher Name | Edition and year |
|---|---|---|---|---|
| 1 | Linear Algebra and its Applications | David C.Lay, Steven R. Lay and J.J.McDonald | Pearson Education Ltd. | 5th Edition, 2015 |
| 2 | Advanced Engineering Mathematics | E. Kreyszig | Wiley | 10th edition, 2015 |
| 3 | Probability and Random Process with application to Signal Processing | Scott L.Miller, Donald G. Childers | Elsevier Academic Press | 2nd Edition, 2013 |

**M.TECH VLSI DESIGN & EMBEDDED SYSTEMS(EVE)**
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**SEMESTER -I**

**ASIC DESIGN**

| | | | |
|---|---|---|---|
| Course Code | 20EVE12 | CIE Marks | 40 |
| TeachingHours/Week (L:T:P) | 4:0:0 | SEE Marks | 60 |
| Credits | 04 | Exam Hours | 03 |

**Module-1**

**Introduction to ASICs:** Full custom, Semi-custom and Programmable ASICs, ASIC Design flow, ASIC cell libraries.

**CMOS Logic:** Data path Logic Cells: Data Path Elements, Adders: Carry skip, Carry bypass, Carry save, Carry select, Conditional sum, Multiplier (Booth encoding), Data path Operators, I/O cells, Cell Compilers.

**Module-2**

**ASIC Library Design:** Logical effort: Predicting Delay, Logical area and logical efficiency, Logical paths, Multi stage cells, Optimum delay and number of stages, library cell design.

**Programmable ASIC Logic Cells:**

MUX as Boolean function generators, Acted ACT: ACT 1, ACT 2 and ACT 3 Logic Modules, Xilinx LCA: XC3000 CLB, Altera FLEX and MAX, Programmable ASIC I/O Cells: Xilinx and Altera I/O Block.

**Module-3**

**Low-level design entry:** Schematic entry: Hierarchical design, The cell library, Names, Schematic Icons & Symbols, Nets, Schematic Entry for ASICs, Connections, vectored instances & buses, Edit in place, attributes, Netlist screener.

**ASIC Construction:** Physical Design, CAD Tools System partitioning, Estimating ASIC size.

**Partitioning:** Goals and objectives, Constructive Partitioning, Iterative Partitioning Improvement, KL, FM and Look Ahead algorithms.

**Module-4**

**Floor planning and placement:** Goals and objectives, Measurement of delay in Floor planning, Floor planning tools, Channel definition, I/O and Power planning and Clock planning.

**Placement:** Goals and Objectives, Min-cut Placement algorithm, Iterative Placement Improvement, Time driven placement methods, Physical Design Flow.

**Module-5**

**Routing**: Global Routing: Goals and objectives, Global Routing Methods, Global routing between blocks, Back-annotation. Detailed Routing: Goals and objectives, Measurement of Channel Density, Left-Edge Algorithm, Area-Routing Algorithms, Multilevel routing, Timing –Driven detailed routing, Final routing steps, Special Routing, Circuit extraction and DRC.

**Course outcomes:**

At the end of the course the student will be able to:

1. Describe the concepts of ASIC design methodology, data path elements, logical effort and FPGA architectures.
2. Analyze the design of FPGAs and ASICs suitable for specific tasks, perform design entry and explain the physical design flow.
3. Design data path elements for ASIC cell libraries and compute optimum path delay.
4. Create floor plan including partition and routing with the use of CAD algorithms.
5. Design CAD algorithms and explain how these concepts interact in ASIC design.

**Question paper pattern:**

The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 60.

- The question paper will have ten full questions carrying equal marks.
- Each full question is for 20 marks.
- There will be two full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub question covering all the topics under a module.
- The students will have to answer five full questions, selecting one full question from each module.

**Textbook/ Textbooks**

| Sl No | Title of the book | Name of the Author/s | Publisher Name | Edition and year |
|---|---|---|---|---|
| 1 | Application - Specific Integrated Circuits | Michael John Sebastian Smith | Addison- Wesley Professional | 2005 |

**M.TECH VLSI DESIGN & EMBEDDED SYSTEMS(EVE)**
**Choice Based Credit System (CBCS) and Outcome Based Education(OBE)**
**SEMESTER -I**

**ADVANCED EMBEDDED SYSTEM**

| | | | |
|---|---|---|---|
| Course Code | 20EVE13 | CIE Marks | 40 |
| TeachingHours/Week (L:T:P) | 4:0:0 | SEE Marks | 60 |
| Credits | 04 | Exam Hours | 03 |

**Module-1**

**Embedded System:** Embedded vs General computing system, classification, application and purpose of ES. Core of an Embedded System, Memory, Sensors, Actuators, LED, Opto coupler, Communication Interface, Reset circuits, RTC, WDT, Characteristics and Quality Attributes of Embedded Systems (Text 1: Selected Topics from Ch -1, 2, 3).

**Module-2**

Hardware Software Co-Design, embedded firmware design approaches, computational models, embedded firmware development languages, Integration and testing of Embedded Hardware and firmware, Components in embedded system development environment (IDE), Files generated during compilation, simulators, emulators and debugging (Text 1: Selected Topics from Ch-7, 9, 12, 13).

**Module-3**

**ARM-32 bit Microcontroller:** Thumb-2 technology and applications of ARM, Architecture of ARM Cortex M3, Various Units in the architecture, General Purpose Registers, Special Registers, exceptions, interrupts, stack operation, reset sequence (Text 2: Ch 1, 2, 3)

**Module-4**

**Instruction Sets:** Assembly basics, Instruction list and description, useful instructions, Memory Systems, Memory maps, Cortex M3 implementation overview, pipeline and bus interface (Text 2: Ch-4, 5, 6).

**Module-5**

Exceptions, Nested Vector interrupt controller design, Systick Timer, Cortex-M3 Programming using assembly and C language, CMSIS (Text 2: Ch-7, 8, 10).

**Course outcomes:**

At the end of the course the student will be able to:

1. Understand the basic hardware components and their selection method based on the characteristics and attributes of an embedded system.
2. Explain the hardware software co-design and firmware design approaches.
3. Understand the suitability of the instruction sets of ARM processors to design of embedded systems.
4. Acquire the knowledge of the architectural features of ARM CORTEX M3, a 32-bit microcontroller including memory map, interrupts and exceptions.
5. Apply the knowledge gained for Programming ARM CORTEX M3 for different applications.

**Question paper pattern:**

The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 60.

- The question paper will have ten full questions carrying equal marks.
- Each full question is for 20 marks.
- There will be two full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub question covering all the topics under a module.
- The students will have to answer five full questions, selecting one full question from each module.

**Textbook/ Textbooks**

| Sl No | Title of the book | Name of the Author/s | Publisher Name | Edition and year |
|---|---|---|---|---|
| 1 | Introduction to embedded systems | K. V. Shibu | TMH education Pvt. Ltd. | 2009 |
| 2 | The Definitive Guide to the ARM Cortex-M3 | Joseph Yiu | Newnes, (Elsevier) | 2nd edn, 2010. |

**Reference Books**

| | | | | |
|---|---|---|---|---|
| 1 | Embedded systems - A contemporary design tool | James K. Peckol | John Wiley | 2008 |

**M.TECH VLSI DESIGN & EMBEDDED SYSTEMS(EVE)**
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**SEMESTER -I**

**VLSI TESTING**

| | | | |
|---|---|---|---|
| Course Code | 20EVE14 | CIE Marks | 40 |
| TeachingHours/Week (L:T:P) | 4:0:0 | SEE Marks | 60 |
| Credits | 04 | Exam Hours | 03 |

**Module-1**

**Faults in digital circuits**: Failures and Faults, Modeling of faults, Temporary Faults. (Text 1)
**Logic Simulation**: Applications, Problems in simulation based design verification, types of simulation, The unknown logic values, compiled simulation, event-driven simulation, Delay models, Element evaluation, Hazard detection, Gate-level event-driven Simulation. (Text 2)

**Module-2**

**Test generation for Combinational Logic circuits**: Fault Diagnosis of digital circuits, Test generation techniques for combinational circuits, Detection of multiple faults in Combinational logic circuits. (Text 1)
**Testable Combinational logic circuit design**: The Read-Muller expansion technique, Three level OR-AND-OR design, Automatic synthesis of testable logic. (Text 1)

**Module-3**

**Testable Combinational logic circuit design**: Testable design of multilevel combinational circuits, Synthesis of random pattern testable combinational circuits, Path delay fault testable combinational logic design, Testable PLA design. (Text 1)
**Test generation for Sequential circuits**: Testing of sequential circuits as Iterative combinational circuits, state table verification, Test generation based on Circuit Structure, Functional Fault models, test Generation based on Functional Fault models. (Text 1)

**Module-4**

**Design of testable sequential circuits**: Controllability and observability, Ad-Hoc design rules for improving testability, design of diagnosable sequential circuits, the scan-path technique for testablesequential circuit design, Level Sensitive Scan Design (LSSD), Random Access Scan Technique, Partial scan, testable sequential circuit design using Nonscan Techniques, Cross check, Boundary Scan. (Text 1)

**Module-5**

**Built-In Self Test**: Test pattern generation for BIST, Output response analysis, Circular BIST, BIST Architectures. (Text 1)
**Testable Memory Design**: RAM Fault Models, Test algorithms for RAMs, Detection of pattern-sensitive faults, BIST techniques for RAM chips, Test generation and BIST for embedded RAMs. (Text1)

**Course outcomes:**
At the end of the course the student will be able to:

1. Analyze the need for fault modeling and testing of digital circuits
2. Generate fault lists for digital circuits and compress the tests for efficiency
3. Create tests for digital memories and analyze failures in them
4. Apply boundary scan technique to validate the performance of digital circuits
5. Design built-in self tests for complex digital circuits

**Question paper pattern:**
The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 60.

- The question paper will have ten full questions carrying equal marks.
- Each full question is for 20 marks.
- There will be two full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub question covering all the topics under a module.
- The students will have to answer five full questions, selecting one full question from each module.

**Students have to conduct the following experiments as a part of CIE marks along with other Activities:**

The experiments constitute

a. Designing the RAMS and combinational circuits using Virtuso (cadence)
b. Generating functional patterns to verify the correctness of the circuit
c. Induce faults (opening/shorting the nodes)
d. Generating patterns to find the faulty nodes
    i. Each pattern considers one faulty node at a time

**Experiments**

1. Design a 2-BIT SRAM using 6T cells
    a. Generate patterns to test if the SRAM is working fine

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**Choice Based Credit System (CBCS) and Outcome Based Education(OBE)**
**SEMESTER -I**

**DIGITAL VLSI DESIGN**

| | | | |
|---|---|---|---|
| Course Code | 20EVE15 | CIE Marks | 40 |
| TeachingHours/Week (L:T:P) | 4:0:0 | SEE Marks | 60 |
| Credits | 04 | Exam Hours | 03 |

**Module-1**

**MOS Transistor:** The Metal Oxide Semiconductor (MOS) Structure, The MOS System under External Bias, Structure and Operation of MOS Transistor, MOSFET Current-Voltage Characteristics, MOSFET Scaling and Small-Geometry Effects.
**MOS Inverters-Static Characteristics**: Introduction, Resistive-Load Inverter, Inverters with n_Type MOSFET Load.

**Module-2**

**MOS Inverters-Static Characteristics:** CMOS Inverter.
**MOS Inverters**: Switching Characteristics and Interconnect Effects: Introduction, Delay-Time Definition, Calculation of Delay Times, Inverter Design with Delay Constraints, Estimation of Interconnect Parasitics, Calculation of Interconnect Delay, Switching Power Dissipation of CMOS Inverters.

**Module-3**

**Semiconductor Memories:** Introduction, Dynamic Random Access Memory (DRAM), Static Random Access Memory (SRAM), Nonvolatile Memory, Flash Memory, Ferroelectric Random Access Memory (FRAM)

**Module-4**

**Dynamic Logic Circuits**: Introduction, Basic Principles of Pass Transistor Circuits, Voltage Bootstrapping, Synchronous Dynamic Circuit Techniques, Dynamic CMOS Circuit Techniques, High Performance Dynamic CMOS circuits.
**BiCMOS Logic Circuits**: Introduction, Bipolar Junction Transistor (BJT): Structure and Operation, Dynamic Behavior of BJTs, Basic BiCMOS Circuits: Static Behavior, Switching Delay in BiCMOS Logic Circuits, BiCMOS Applications.

**Module-5**

**Chip Input and Output (I/O) Circuits**: Introduction, ESD Protection, Input Circuits, Output Circuits and L(di/dt) Noise, On-Chip Clock Generation and Distribution, Latch-Up and Its Prevention.
**Design for Manufacturability**: Introduction, Process Variations, Basic Concepts and Definitions, Design of Experiments and Performance Modeling.

**Course outcomes:**
At the end of the course the student will be able to:
1. Analyse issues of On-chip interconnect Modelling and Interconnect delay calculation.
2. Analyse the Switching Characteristics in Digital Integrated Circuits.
3. Use the Dynamic Logic circuits in state-of-the-art VLSI chips.
4. Study critical issues such as ESD protection, Clock distribution, Clock buffering, and Latch phenomenon
5. Use Bipolar and Bi-CMOS circuits in very high speed design.

**Question paper pattern:**
The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 60.
- The question paper will have ten full questions carrying equal marks.
- Each full question is for 20 marks.
- There will be two full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub question covering all the topics under a module.
- The students will have to answer five full questions, selecting one full question from each module.

**Textbook/ Textbooks**

| Sl No | Title of the book | Name of the Author/s | Publisher Name | Edition and year |
|---|---|---|---|---|
| 1 | CMOS Digital Integrated Circuits: Analysis and Design | Sung Mo Kang & Yusuf Leblebici | Tata McGraw-Hill | Third Edition |

**Reference Books**

| | | | | |
|---|---|---|---|---|
| 1 | Principles of CMOS VLSI Design: A System Perspective | Neil Weste and K. Eshraghian | Pearson Education (Asia) Pvt. Ltd | Second Edition, 2000 |
| 2 | Modern VLSI Design: System on Silicon | Wayne, Wolf | Prentice Hall PTR/ Pearson Education | Second Edition, 1998 |
| 3 | Basic VLSI Design | Douglas A Pucknell& Kamran Eshraghian | PHI | 3rdEdition |

| M.TECH VLSI DESIGN & EMBEDDED SYSTEMS (EVE)<br>Choice Based Credit System (CBCS) and Outcome Based Education(OBE)<br>SEMESTER -I | | | |
|---|---|---|---|
| VLSI & ES Lab-1 | | | |
| Course Code | 20EVEL16 | CIE Marks | 40 |
| TeachingHours/Week (L:T:P) | 0:0:4 | SEE Marks | 60 |
| Credits | 02 | Exam Hours | 03 |

| Sl. No | Experiments |
|---|---|
| | **Part – A: VLSI Digital Design**<br>Experiments to be done using<br>1. CADENCE/SYNOPSYS/MENTOR GRAPHICS/TANNER or any other equivalent Tool<br>2. FPGA/CPLD Boards with Xilinx or any other equivalent |
| | **ASIC-Digital Design Flow**<br><br>I. Write Verilog Code for the following circuits and their Test Bench for verification, observe the wave technological library (constraints to be given). Do the initial timing verification with gate level simulation.<br><br>1. An inverter, Buffer, Transmission gate and basic gates<br>2. Flip flop - RS, D, JK, MS, T<br>3. 4-bit counter [Synchronous & Asynchronous counter]<br><br>**Note: For the set of experiments listed above, students can make the following flow as a study:**<br>- Core Constrained flow<br>- Creation of I/O pad frame<br>- Use the created I/O pad frame for Pad constrained design.<br>- CTS flow Only for designs which have clock |
| | **FPGA DIGITAL DESIGN**<br><br>VLSI Front End Design programs:<br><br>Programming can be done using any compiler. Down load the programs on FPGA/CPLD boards and use pattern generator (32 channels and logic analyzer)/Chipscope pro apart from verification by simulation<br><br>1. Write Verilog code for the design of 8-bit<br>i. Carry Ripple Adder<br>ii. Carry Look Ahead adder<br>iii. Carry Skip Adder<br><br>2. Write Verilog Code for 8-bit<br>i. Array Multiplication (Signed and Unsigned)<br>ii. Booth Multiplication (Radix-4)<br><br>3. Write Verilog code for 4/8-bit<br>i. Magnitude Comparator<br>ii. LFSR<br>iii. Parity Generator<br>iv. Universal Shift Register<br><br>4. Design a Mealy and Moore Sequence Detector using Verilog to detect Sequence. Eg 11101 (with and without overlap) any sequence can be specified. |
| | **Part – B: Experiments to be done using ARM Cortex M3** |
| | **ARM Cortex M3 Programs** - Programming to be done using Keil uVision 4 and download the program on to a M3 evaluation board such as NXP LPC1768 or ATMEL ARM<br><br>a) Write an Assembly language program to calculate the sum and display the result for the addition of first ten numbers. SUM = 10+9+8+.....+1 |

**M.TECH VLSI DESIGN & EMBEDDED SYSTEMS (EVE)**

**Choice Based Credit System (CBCS) and Outcome Based Education(OBE)**

**SEMESTER -I**

**RESEARCH METHODOLOGY AND IPR**

| | | | |
|---|---|---|---|
| Course Code | 20RMI17 | CIE Marks | 40 |
| Teaching Hours/Week (L:T:P) | 2:0:0 | SEE Marks | 60 |
| Credits | 02 | Exam Hours | 03 |

**Module-1**

**Research Methodology:** Introduction, Meaning of Research, Objectives of Research, Motivation in Research, Types of Research, Research Approaches, Significance of Research, Research Methods versus Methodology, Research and Scientific Method, Importance of Knowing How Research is Done, Research Process, Criteria of Good Research, and Problems Encountered by Researchers in India.

**Defining the Research Problem:** Research Problem, Selecting the Problem, Necessity of Defining the Problem, Technique Involved in Defining a Problem, An Illustration.

**Module-2**

**Reviewing the literature:** Place of the literature review in research, Bringing clarity and focus to your research problem, Improving research methodology, Broadening knowledge base in research area, Enabling contextual findings, How to review the literature, searching the existing literature, reviewing the selected literature, Developing a theoretical framework, Developing a conceptual framework, Writing about the literature reviewed.

**Research Design:** Meaning of Research Design, Need for Research Design, Features of a Good Design, Important Concepts Relating to Research Design, Different Research Designs, Basic Principles of Experimental Designs, Important Experimental Designs.

**Module-3**

**Design of Sampling:** Introduction, Sample Design, Sampling and Non-sampling Errors, Sample Survey versus Census Survey, Types of Sampling Designs.

**Measurement and Scaling:** Qualitative and Quantitative Data, Classifications of Measurement Scales, Goodness of Measurement Scales, Sources of Error in Measurement Tools, Scaling, Scale Classification Bases, Scaling Technics, Multidimensional Scaling, Deciding the Scale.

**Data Collection**: Experimental and Surveys, Collection of Primary Data, Collection of Secondary Data, Selection of Appropriate Method for Data Collection, Case Study Method.

**Module-4**

**Testing of Hypotheses:** Hypothesis, Basic Concepts Concerning Testing of Hypotheses, Testing of Hypothesis, Test Statistics and Critical Region, Critical Value and Decision Rule, Procedure for Hypothesis Testing, Hypothesis Testing for Mean, Proportion, Variance, for Difference of Two Mean, for Difference of Two Proportions, for Difference of Two Variances, P-Value approach, Power of Test, Limitations of the Tests of Hypothesis.

Chi-square Test: Test of Difference of more than Two Proportions, Test of Independence of Attributes, Test of Goodness of Fit, Cautions in Using Chi Square Tests.

**Module-5**

**Interpretation and Report Writing:** Meaning of Interpretation, Technique of Interpretation, Precaution in Interpretation, Significance of Report Writing, Different Steps in Writing Report, Layout of the Research Report, Types of Reports, Oral Presentation, Mechanics of Writing a Research Report, Precautions for Writing Research Reports.

**Intellectual Property:** The Concept, Intellectual Property System in India, Development of TRIPS Complied Regime in India, Patents Act, 1970, Trade Mark Act, 1999,The Designs Act, 2000, The Geographical Indications of Goods (Registration and Protection) Act1999, Copyright Act,1957,The Protection of Plant Varieties and Farmers' Rights Act, 2001,The Semi-Conductor Integrated Circuits Layout Design Act, 2000, Trade Secrets, Utility Models, IPR and Biodiversity, The Convention onBiological Diversity (CBD) 1992, Competing Rationales for Protection of IPRs, Leading International Instruments Concerning IPR, World Intellectual Property Organisation (WIPO),WIPO and WTO, Paris Convention for the Protection of Industrial Property, National Treatment, Right of Priority, Common Rules, Patents, Marks, Industrial Designs, Trade Names, Indications of Source, Unfair Competition,

Patent Cooperation Treaty (PCT), Advantages of PCT Filing, Berne Convention for the Protection of Literary and Artistic Works, Basic Principles, Duration of Protection, Trade Related Aspects of Intellectual Property Rights(TRIPS) Agreement, Covered under TRIPS Agreement, Features of the Agreement, Protection of Intellectual Property under TRIPS, Copyright and Related Rights, Trademarks, Geographical indications, Industrial Designs, Patents, Patentable Subject Matter, Rights Conferred, Exceptions, Term of protection, Conditions on Patent Applicants, Process Patents, Other Use without Authorization of the Right Holder, Layout-Designs of Integrated Circuits, Protection of Undisclosed Information, Enforcement of Intellectual Property Rights, UNSECO.

**M.TECH VLSI DESIGN & EMBEDDED SYSTEMS (EVE)**
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**SEMESTER -II**

**Design of Analog and Mixed Mode VLSI Circuits**

| | | | |
|---|---|---|---|
| Course Code | 20EVE21 | CIE Marks | 40 |
| TeachingHours/Week (L:T:P) | 4:0:0 | SEE Marks | 60 |
| Credits | 04 | Exam Hours | 03 |

**Module-1**

**Basic MOS Device Physics**: General considerations, MOS I/V Characteristics, second order effects, MOS device models.
**Single stage Amplifier**: Basic Concepts, Common Source stage (Text 1)

**Module-2**

**Single stage Amplifier**: Source follower, common-gate stage, Cascode Stage, choice of device models.
**Differential Amplifiers**: Single ended and differential operation, Basic differential pair, Common mode response, Differential pair with MOS loads, Gilbert cell (Text 1)

**Module-3**

**Passive and Active Current Mirrors**: Basic current mirrors, Cascode Current mirrors, Active Current mirrors.
**Operational Amplifiers (part-1):** General Considerations, One Stage OP-Amp, Two Stage OP-Amp, Gain boosting (Text 1)

**Module-4**

**Operational Amplifiers (part-2)**: Common Mode Feedback, Slew rate, Power Supply Rejection.
**Phase Locked Loops**: Simple PLL, Charge pump PLLs, Non-ideal effects in PLLs, Delay-Locked Loops, Applications (Text 1)

**Module-5**

**Data Converter Architectures**: DAC & ADC Specifications, Current Steering DAC, Charge Scaling DAC, Cyclic DAC, Pipeline DAC, Flash ADC, Pipeline ADC, Integrating ADC, Successive Approximation ADC (Text 2)

**Course outcomes:**
At the end of the course the student will be able to:

1. Use efficient analytical tools for quantifying the behaviour of basic circuits by inspection.
2. Design high-performance, stable operational amplifiers with the trade-offs between speed, precision and power dissipation.
3. Design and study the behaviour of phase-locked-loops for the applications.
4. Identify the critical parameters that affect the analog and mixed-signal VLSI circuits' performance
5. Perform calculations in the digital or discrete time domain, more sophisticated data converters to translate the digital data to and from inherently analog world.

**Question paper pattern:**
The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 60.

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- Each full question will have sub question covering all the topics under a module.
- The students will have to answer five full questions, selecting one full question from each module.

**Textbook/ Textbooks**

| Sl No | Title of the book | Name of the Author/s | Publisher Name | Edition and year |
|---|---|---|---|---|
| 1 | Design of Analog CMOS Integrated Circuits | Behzad Razavi | TMH | 2007 |
| 2 | CMOS Circuit Design, Layout, and Simulation | R. Jacob Baker | Wiley | Second Edition |
| **Reference Books** | | | | |
| 1 | CMOS Analog Circuit Design | Phillip E. Allen, Douglas R. Holberg | Oxford University Press | Second Edition |

**M.TECH VLSI DESIGN & EMBEDDED SYSTEMS (EVE)**
**Choice Based Credit System (CBCS) and Outcome Based Education(OBE)**
**SEMESTER -II**

**Real Time Operating System**

| | | | |
|---|---|---|---|
| Course Code | 20EVE22 | CIE Marks | 40 |
| TeachingHours/Week (L:T:P) | 4:0:0 | SEE Marks | 60 |
| Credits | 04 | Exam Hours | 03 |

**Module-1**

**Real-Time Systems and Resources**: Brief history of Real Time Systems, A brief history of Embedded Systems. System Resources, Resource Analysis, Real-Time Service Utility, Scheduler concepts, Real-Time OS, State transition diagram and tables, Thread Safe Reentrant Functions. (Text 1: Selected sections from Chap. 1, 2)

**Module-2**

**Processing with Real Time Scheduling**: Scheduler Concepts, Preemptive Fixed Priority Scheduling Policies with timing diagrams and problems and issues, Feasibility, Rate Monotonic least upper bound, Necessary and Sufficient feasibility, Deadline –Monotonic Policy, Dynamic priority policies, Alternative to RM policy. (Text 1: Chap. 2,3,7)

**Module-3**

**Memory and I/O**: Worst case execution time, Intermediate I/O, Shared Memory, ECC Memory, Flash file systems. Multi-resource Services, Blocking, Deadlock and live lock, Critical sections to protect shared resources, Missed deadline, QoS, Reliability and Availability, Similarities and differences, Reliable software, Available software. (Text 1: Selected topics from Chap. 4,5,6,7,11)

**Module-4**

**Firmware Components**: The 3 firmware components, RTOS system software mechanisms, Software application components. Debugging Components, Exceptions, assert, Checking return codes, Single-step debugging, Test access ports, Trace Ports. (Text 1: Selected topics from Chap. 8,9)

**Module-5**

**Process and Threads**: Process and thread creations, Programs related to semaphores, message queue, shared buffer applications involving inter task/thread communication (Text 2: Chap. 11).

**Course outcomes:**

At the end of the course the student will be able to:

1. Develop programs for real time services, firmware and RTOS, using the fundamentals of Real Time Embedded System, real time service utilities,debugging methodologies and optimization techniques.
2. Select the appropriate system resources (CPU, I/O, Memory, Cache, ECCMemory, Microcontroller/FPGA/ASIC to improve the system performance.
3. Apply priority based static and dynamic real time scheduling techniques forthe given specifications.
4. Analyze deadlock conditions, shared memory problem, critical sectionproblem, missed deadlines, availability, reliability and QoS.
5. Develop programs for multithreaded applications using suitable techniquesand data structure

**Question paper pattern:**

The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 60.

- The question paper will have ten full questions carrying equal marks.
- Each full question is for 20 marks.
- There will be two full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub question covering all the topics under a module.
- The students will have to answer five full questions, selecting one full question from each module.

**Textbook/ Textbooks**

| Sl No | Title of the book | Name of the Author/s | Publisher Name | Edition and year |
|---|---|---|---|---|
| 1 | Real-Time Embedded Systems and Components | Sam Siewert | Cengage Learning India Edition | 2007 |
| 2 | Embedded/Real Time Systems, Concepts, Design and Programming, Black Book | Dr. K.V.K.K Prasad | Dream Tech Press | New edition, 2010 |

**Reference Books**

| | | | | |
|---|---|---|---|---|
| 1 | Real Time System | James W S Liu | Pearson Education | 2008 |
| 2 | Programming for Embedded Systems | Dream Tech Software Team | John Wiley, India Pvt. Ltd. | 2008 |

**M.TECH VLSI DESIGN & EMBEDDED SYSTEMS (EVE)**
**Choice Based Credit System (CBCS) and Outcome Based Education(OBE)**
**SEMESTER -II**

**System Verilog**

| | | | |
|---|---|---|---|
| Course Code | 20EVE23 | CIE Marks | 40 |
| TeachingHours/Week (L:T:P) | 4:0:0 | SEE Marks | 60 |
| Credits | 04 | Exam Hours | 03 |

**Module-1**

**Verification Guidelines:**
The verification process, basic test bench functionality, directed testing, methodology basics, constrained random stimulus, randomization, functional coverage, test bench components, layered testbench.

**Data Types**:
Built in Data types, fixed and dynamic arrays, Queues, associative arrays, linked lists, array methods, choosing a storage type, creating new types with type def, creating user defined structures, typeconversion, Enumerated types, constants and strings, Expression width.

**Module-2**

**Procedural Statements and Routines**:
Procedural statements, Tasks, Functions and void functions, Task and function overview, Routine arguments, returning from a routine, Local data storage, time values.

**Converting the test bench and design**:
Separating the test bench and design, The interface construct, Stimulus timing, Interface driving and sampling, System Verilog assertions.

**Module-3**

**Randomization**:
Introduction, Randomization in System Verilog, Constraint details, Solution probabilities, Valid constraints, In-line constraints, Random number functions, Common randomization problems, Iterative and array constraints, Random control, Random Number Generators.

**Module-4**

**Threads and Interprocess Communication**:
Working with threads, Disabling threads, Interprocess communication, Events, semaphores, Mailboxes, Building a test bench with threads and Interprocess Communication.

**Module-5**

**Functional Coverage:**
Coverage types, Coverage strategies, Simple coverage example, Anatomy of Cover group and Triggering a Cover group, Data sampling, Cross coverage, Generic Cover groups, Coverage options, Analyzing coverage data, measuring coverage statistics during simulation.

**Course outcomes:**
At the end of the course the student will be able to:

1. Write test benches for moderately complex digital circuits
2. Use System Verilog language
3. Appreciate functional coverage
4. Apply constrained random tests benches using System Verilog
5. Analyze a verification case and apply System Verilog to verify the design

**Question paper pattern:**
The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 60.

- The question paper will have ten full questions carrying equal marks.
- Each full question is for 20 marks.
- There will be two full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub question covering all the topics under a module.
- The students will have to answer five full questions, selecting one full question from each module.

**Students have to conduct the following experiments as a part of CIE marks along with other Activities:**

1. Write a program to demonstrate two-state and four-state data types.
2. Write a program to demonstrate push_front, pop_front, push_back and pop_back with respect to Queues.
3. Declare four variables red, black, white and green through Enumerated type declaration, use the keywords ‘first’ and ‘next’ to step through the variables and display the output.
4. Demonstrate Full adder with ‘Interface’ construct.
5. Write a program to demonstrate the difference between ‘rand’ and ‘randc’.
6. Demonstrate Random Control with randcase and $urandom_range.
7. Demonstrate 4-bit adder with the verification environment.

**M.TECH VLSI DESIGN & EMBEDDED SYSTEMS (EVE)**
**Choice Based Credit System (CBCS) and Outcome Based Education(OBE)**
**SEMESTER -II**

**Advances in VLSI Design**

| | | | |
|---|---|---|---|
| Course Code | 20EVE241 | CIE Marks | 40 |
| TeachingHours/Week (L:T:P) | 4:0:0 | SEE Marks | 60 |
| Credits | 04 | Exam Hours | 03 |

**Module-1**

**Implementation Strategies For Digital ICS**: Introduction, From Custom to Semicustom and Structured Array Design Approaches, Custom Circuit Design, Cell-Based Design Methodology, Standard Cell, Compiled Cells, Macrocells, Megacells and Intellectual Property, Semi-Custom Design Flow, Array-Based Implementation Approaches, Pre-diffused (or Mask-Programmable) Arrays, Pre-wired Arrays, Perspective-The Implementation Platform of the Future.

**Module-2**

**Coping With Interconnect**: Introduction, Capacitive Parasitics, Capacitance and Reliability-Cross Talk, Capacitance and Performance in CMOS, Resistive Parasitics, Resistance and Reliability-Ohmic Voltage Drop, Electromigration, Resistance and Performance-RC Delay, Inductive Parasitics, Inductance and Reliability-Voltage Drop, Inductance and Performance-Transmission Line Effects, Advanced Interconnect Techniques, Reduced-Swing Circuits, Current-Mode Transmission Techniques, Perspective: Networks-on-a-Chip.

**Module-3**

**Timing Issues In Digital Circuits**: Introduction, Timing Classification of Digital Systems, Synchronous Interconnect, Mesochronous interconnect, Plesiochronous Interconnect, Asynchronous Interconnect, Synchronous Design — An In-depth Perspective, Synchronous Timing Basics, Sources of Skew and Jitter, Clock-Distribution Techniques, Latch-Base Clocking, Self-Timed Circuit Design, Self-Timed Logic - An Asynchronous Technique, Completion-Signal Generation, Self-Timed Signaling, Practical Examples of Self-Timed Logic, Synchronizers and Arbiters, Synchronizers-Concept and Implementation, Arbiters, Clock Synthesis and Synchronization Using a Phase-Locked Loop, Basic Concept, Building Blocks of a PLL.

**Module-4**

**Designing Memory and Array Structures**: Introduction, Memory Classification, Memory Architectures and Building Blocks, The Memory Core, Read-Only Memories, Nonvolatile Read-Write Memories, Read-Write Memories (RAM), Contents-Addressable or Associative Memory (CAM), Memory Peripheral Circuitry, The Address Decoders, Sense Amplifiers, Voltage References,Drivers/Buffers, Timing and Control.

**Module-5**

**Designing Memory and Array Structures**: Memory Reliability and Yield, Signal-to-Noise Ratio, Memory yield, Power Dissipation in Memories, Sources of Power Dissipation in Memories, Partitioning of the memory, Addressing the Active Power Dissipation, Data retention dissipation, Case Studies in Memory Design: The Programmable Logic Array (PLA), A 4Mbit SRAM, A 1 Gbit NAND Flash Memory, Perspective: Semiconductor Memory Trends and Evolutions.

**Course outcomes:**

At the end of the course the student will be able to:

1. Apply design automation for complex circuits using the different implementation methodology like custom versus semi-custom, hardwired versus fixed, regular array versus ad-hoc.
2. Use the approaches to minimize the impact of interconnect parasitics on performance, power dissipation and circuit reliability
3. Impose the ordering of the switching events to meet the desired timing constraints using synchronous, clocked approach.
4. Infer the reliability of the memory
5. Understand the role of peripheral circuitry such as the decoders, sense amplifiers, drivers and control circuitry in the design of reliable and fast memories.

**Question paper pattern:**

The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 60.

- The question paper will have ten full questions carrying equal marks.
- Each full question is for 20 marks.
- There will be two full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub question covering all the topics under a module.
- The students will have to answer five full questions, selecting one full question from each module.

**Textbook/ Textbooks**

| Sl No | Title of the book | Name of the Author/s | Publisher Name | Edition and year |
|---|---|---|---|---|
| 1 | Digital Integrated Circuits-A Design Perspective | Jan M Rabey, AnanthaChandrakasan, Borivoje | PHI | 2nd Edition |

**M.TECH VLSI DESIGN & EMBEDDED SYSTEMS (EVE)**
**Choice Based Credit System (CBCS) and Outcome Based Education(OBE)**
**SEMESTER -II**

**Nanoelectronics**

| | | | |
|---|---|---|---|
| Course Code | 20EVE242 | CIE Marks | 40 |
| TeachingHours/Week (L:T:P) | 4:0:0 | SEE Marks | 60 |
| Credits | 04 | Exam Hours | 03 |

**Module-1**

**Introduction**: Overview of nanoscience and engineering. Development milestones in microfabrication and electronic industry. Moores' law and continued miniaturization, Classification of Nanostructures,
Electronic properties of atoms and solids: Isolated atom, Bonding between atoms, Giant molecular solids, Free electron models and energy bands, crystalline solids, Periodicity of crystal lattices,Electronic conduction, effects of nanometer length scale, Fabrication methods: Top down processes, Bottom up processes methods for templating the growth of nanomaterials, ordering of nanosystems (Text 1).

**Module-2**

**Characterization**: Classification, Microscopic techniques, Field ion microscopy, scanning probe techniques, diffraction techniques: bulk and surface diffraction techniques, spectroscopy techniques: photon, radiofrequency, electron, surface analysis and dept profiling: electron, mass, Ion beam, Reflectrometry, Techniques for property measurement: mechanical, electron, magnetic, thermal properties (Text1)

**Module-3**

**Inorganic semiconductor nanostructures**: overview of semiconductor physics. Quantum confinement in semiconductor nanostructures: quantum wells, quantum wires, quantum dots, super-lattices, band offsets, electronic density of states (Text1).
**Carbon Nanostructures**: Carbon molecules, Carbon Clusters, Carbon Nanotubes, application of Carbon Nanotubes (Text 2).

**Module-4**

**Fabrication techniques**: requirements of ideal semiconductor, epitaxial growth of quantum wells, lithography and etching, cleaved-edge over growth, growth of vicinal substrates, strain induced dots and wires, electrostatically induced dots and wires, Quantum well width fluctuations, thermally annealed quantum wells, semiconductor nanocrystals, colloidal quantum dots, self-assembly techniques.
**Physical processes**: modulation doping, quantum hall effect, resonant tunneling, charging effects, ballistic carrier transport, Inter band absorption, intra band absorption, Light emission processes, phonon bottleneck, quantum confined stark effect, nonlinear effects, coherence and dephasing, characterization of semiconductor nanostructures: optical electrical and structural (Text1).

**Module-5**

**Methods of measuring properties**: atomic, crystallography, microscopy, spectroscopy (Text 2).
**Applications**: Injection lasers, quantum cascade lasers, single-photon sources, biological tagging, optical memories, coulomb blockade devices, photonic structures, QWIPs, NEMS, MEMS (Text1).

**Course outcomes:**
At the end of the course the student will be able to:
1. Know the principles behind Nanoscience engineering and Nanoelectronics.
2. Apply the knowledge to prepare and characterize nanomaterials.
3. Know the effect of particles size on mechanical, thermal, optical and electrical properties of nanomaterials.
4. Design the process flow required to fabricate state of the art transistor technology.
5. Analyze the requirements for new materials and device structure in the future technologies.

**Question paper pattern:**
The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 60.
- The question paper will have ten full questions carrying equal marks.
- Each full question is for 20 marks.
- There will be two full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub question covering all the topics under a module.
- The students will have to answer five full questions, selecting one full question from each module.

**Textbook/ Textbooks**

| Sl No | Title of the book | Name of the Author/s | Publisher Name | Edition and year |
|---|---|---|---|---|
| 1 | Nanoscale Science and Technology | Ed Robert Kelsall, Ian Hamley, Mark Geoghegan | John Wiley | 2007 |
| 2 | Introduction to Nanotechnology | Charles P Poole, Jr, Frank J Owens | John Wiley | Copyright 2006, Reprint 2011. |

**M.TECH VLSI DESIGN & EMBEDDED SYSTEMS (EVE)**

**Choice Based Credit System (CBCS) and Outcome Based Education(OBE)**
**SEMESTER -II**

**Static Timing Analysis**

| | | | |
|---|---|---|---|
| Course Code | 20EVE243 | CIE Marks | 40 |
| TeachingHours/Week (L:T:P) | 4:0:0 | SEE Marks | 60 |
| Credits | 04 | Exam Hours | 03 |

**Module-1**

**Introduction**: Nanometer Designs, What is Static Timing Analysis? Why Static Timing Analysis?, Crosstalk and Noise,Design Flow, CMOS Digital Designs, FPGA Designs,Asynchronous Designs, STA at Different Design Phases,Limitations of Static Timing Analysis, Power Considerations,Reliability Considerations

**STA Concepts**: CMOS Logic Design, Basic MOS Structure, CMOSLogic Gate, Standard Cells, Modeling of CMOS Cells, SwitchingWaveform, Propagation Delay, Slew of a Waveform, Skew betweenSignals, Timing Arcs and Unateness, Min and Max Timing Paths,Clock Domains, Operating Conditions

**Module-2**

**Standard Cell Library**: Pin Capacitance, Timing Modeling, Linear Timing Model, Non-Linear Delay Model, Example of Non-Linear,Delay Model Lookup, Threshold Specifications and Slew Derating

Timing Models - Combinational Cells, Delay and Slew Models, Positive or Negative Unate, General Combinational Block, TimingModels - Sequential Cells, Synchronous Checks: Setup and Hold,Example of Setup and Hold Checks, Negative Values in Setup andHold Checks, Asynchronous Checks, Recovery and RemovalChecks

Pulse Width Checks, Example of Recovery, Removal and PulseWidth Checks, Propagation Delay,State-Dependent Models XOR,XNOR and Sequential Cells, Interface Timing Model for a BlackBox, Advanced Timing Modeling, Receiver Pin Capacitance,Specifying Capacitance at the Pin Level, Specifying Capacitance atthe Timing Arc Level, Output Current, Models for Crosstalk NoiseAnalysis, DC Current, Output Voltage, Propagated Noise, NoiseModels for Two-Stage Cells, Noise Models for Multi-stage andSequential Cells, Other Noise Models, Power DissipationModeling, Active Power, Double Counting Clock Pin Power,Leakage Power, Other Attributes in Cell Library, Area Specification, Function Specification, SDF Condition,Characterization and Operating Conditions, What is the ProcessVariable, Derating using K-factors, Library Units.

**Module-3**

**Interconnect Parasitics**: RLC for Interconnect, Wireload Models, Interconnect Trees, Specifying Wireload Models, Representation ofExtracted Parasitics, Detailed Standard Parasitic Format,Reduced Standard Parasitic Format, Standard Parasitic ExchangeFormat, Representing Coupling Capacitances, HierarchicalMethodology, Block Replicated in Layout, Reducing Parasitics forCritical Nets, Reducing Interconnect Resistance, Increasing WireSpacing, Parasitics for Correlated Nets.

**Delay Calculation**: Overview, Delay Calculation Basics, DelayCalculation with Interconnect, Pre-layout Timing, Post-layoutTiming, Cell Delay using Effective Capacitance, InterconnectDelay, Elmore Delay, Higher Order Interconnect DelayEstimation, Full Chip Delay Calculation, Slew Merging, DifferentSlew Thresholds, Different Voltage Domains, Path DelayCalculation, Combinational Path Delay, Path to a Flip-flop, Inputto Flip-flop Path, Flip-flop to Flip-flop Path, Multiple Paths, SlackCalculation.

**Module-4**

**Configuring the STA Environment**: What is the STAEnvironment?

Specifying Clocks, Clock Uncertainty, Clock Latency, GeneratedClocks, Example of Master Clock at Clock Gating Cell Output,Generated Clock using Edge and Edge_shift Options, GeneratedClock using Invert Option, Clock Latency for Generated Clocks,Typical Clock Generation Scenario, Constraining Input Paths,Constraining Output Paths, Example A, Example B, Example C,Timing Path Groups, Modeling of External Attributes, ModelingDrive Strengths, Modeling Capacitive Load, Design Rule Checks,Virtual Clocks, Refining the Timing Analysis, Specifying InactiveSignals, Breaking Timing Arcs in Cells, Point-to-PointSpecification, Path Segmentation

**Module-5**

**Timing Verification**: Setup Timing Check, Flip-flop to Flip-flop Path, Input to Flip-flop Path, Input Path with Actual Clock, Flipflopto Output Path, Input to Output Path, Frequency Histogram,Hold Timing Check, Flip-flop to Flip-flop Path, Hold SlackCalculation, Input to Flip-flop Path, Flip-flop to Output Path,Flip-flop to Output Path with Actual Clock, Input to Output Path,Multicycle Paths, Crossing Clock Domains, False Paths, Half-Cycle Paths, Removal Timing Check, Recovery Timing Check,Timing across Clock Domains, Slow to Fast Clock Domains, Fastto Slow Clock Domains, Half-cycle Path - Case 1, Half-cycle Path -Case 2, Fast to Slow Clock Domain, Slow to Fast Clock Domain,Multiple Clocks, Integer Multiples, Non-Integer Multiples, PhaseShifted.

**M.TECH VLSI DESIGN & EMBEDDED SYSTEMS (EVE)**
**Choice Based Credit System (CBCS) and Outcome Based Education(OBE)**
**SEMESTER -II**

**Reconfigurable Computing**

| | | | |
|---|---|---|---|
| Course Code | 20EVE244 | CIE Marks | 40 |
| TeachingHours/Week (L:T:P) | 4:0:0 | SEE Marks | 60 |
| Credits | 04 | Exam Hours | 03 |

**Module-1**

**Introduction**: History, Reconfigurable vs Processor based system, RC Architecture.
**Reconfigurable Logic Devices**: Field Programmable Gate Array, Coarse Grained ReconfigurableArrays.
**Reconfigurable Computing System**: Parallel Processing on Reconfigurable Computers, A survey ofReconfigurable Computing System. (Text 1)

**Module-2**

**Languages and Compilation**: Design Cycle, Languages, HDL, High Level Compilation, Low level Design flow, Debugging Reconfigurable Computing Applications. (Text 1)

**Module-3**

**Implementation**: Integration, FPGA Design flow, Logic Synthesis.
**High Level Synthesis for Reconfigurable Devices:** Modelling, Temporal Partitioning Algorithms. (Text 2)

**Module-4**

**Partial Reconfiguration Design**: Partial Reconfiguration Design, Bitstream Manipulation with JBits, The modular Design flow, The Early Access Design Flow, Creating Partially Reconfigurable Designs, Partial Reconfiguration using Hansel-C Designs, Platform Design. (Text 2)

**Module-5**

**Signal Processing Applications**: Reconfigurable computing for DSP, DSP application building blocks, Examples: Beamforming, Software Radio, Image and video processing, Local Neighbourhood functions, Convolution. (Text 1)
**System on a Programmable Chip**: Introduction to SoPC, Adaptive Multiprocessing on Chip.(Text 2)

**Course outcomes:**
At the end of the course the student will be able to:

1. Understand the fundamental principles and practices in reconfigurable architecture.
2. Simulate and synthesize the reconfigurable computing architectures.
3. Understand the FPGA design principles, and logic synthesis
4. Integrate hardware and software technologies for reconfiguration computing focusing on partial reconfiguration design.
5. Design digital systems for a variety of applications on signal processing and system on chip configurations.

**Question paper pattern:**
The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 60.

- The question paper will have ten full questions carrying equal marks.
- Each full question is for 20 marks.
- There will be two full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub question covering all the topics under a module.
- The students will have to answer five full questions, selecting one full question from each module.

**Textbook/ Textbooks**

| Sl No | Title of the book | Name of the Author/s | Publisher Name | Edition and year |
|---|---|---|---|---|
| 1 | Reconfigurable Computing: Accelerating Computation with Field-Programmable Gate Arrays | M. Gokhale and P. Graham | Springer, ISBN: 978-0-387-26105-8 | 2005 |
| 2 | Introduction to Reconfigurable Computing: Architectures, Algorithms and Applications | C. Bobda | Springer, ISBN: 978-1-4020-6088-5 | 2007 |
| **Reference Books** | | | | |
| 1 | Practical FPGA Programming in C | D. Pellerin and S. Thibault | Prentice-Hall | 2005 |
| 2 | FPGA Based System Design | W. Wolf | Prentice-Hall | 2004 |
| 3 | Rapid System Prototyping with FPGAs: Accelerating the Design Process | R. Cofer and B. Harding | Newnes | 2005 |

**M.TECH VLSI DESIGN & EMBEDDED SYSTEMS (EVE)**
**Choice Based Credit System (CBCS) and Outcome Based Education(OBE)**
**SEMESTER -II**

**Low Power VLSI Design**

| | | | |
|---|---|---|---|
| Course Code | 20EVE251 | CIE Marks | 40 |
| TeachingHours/Week (L:T:P) | 4:0:0 | SEE Marks | 60 |
| Credits | 04 | Exam Hours | 03 |

**Module-1**

**Introduction**: Need for low power VLSI chips, charging and discharging capacitance, short circuit current in CMOS leakage current, static current, basic principles of low power design, low power figure of merits.
**Simulation power analysis**: SPICE circuit simulation, discrete transistor modeling and analysis, gate level logic simulation, architecture level analysis, data correlation analysis in DSP systems, Monte Carlo simulation. (Text 1)

**Module-2**

**Probabilistic power analysis**: Random logic signals, probability & frequency, probabilistic power analysis techniques, signal entropy.
**Circuit**: Transistor and gate sizing, equivalent pin ordering, network restructuring and reorganization, special latches and flip flops, low power digital cell library, adjustable device threshold voltage. (Text 1)

**Module-3**

**Logic:** Gate reorganization, signal gating, logic encoding, state machine encoding, pre-computation logic (Text 1).
**Low power Clock Distribution:** Power dissipation in clock distribution, single driver Vs distributed buffers, Zero skew Vs tolerable skew, chip & package co design of clock network (Text 2).

**Module-4**

**Low power Architecture & Systems**: Power & performance management, switching activity reduction, parallel architecture with voltage reduction, flow graph transformation (Text 1).
**Low power arithmetic components**: Introduction, circuit design style, adders, multipliers, division (Text 2).

**Module-5**

**Low power memory design**: Introduction, sources and reductions of power dissipation in memory subsystem, sources of power dissipation in DRAM and SRAM (Text 2).
**Algorithm & Architectural Level Methodologies**: Introduction, design flow, Algorithmic level analysis & optimization, Architectural level estimation & synthesis (Text 2).
**Advanced Techniques**: Adiabatic computation, pass transistor, Asynchronous circuits (Text 1).

**Course outcomes:**
At the end of the course the student will be able to:
1. Identify the sources of power dissipation in CMOS circuits.
2. Perform power analysis using simulation-based approaches and probabilistic analysis.
3. Use optimization and trade-off techniques that involve power dissipation of digital circuits.
4. Make the power design a reality by making power dimension an integral part of the design process.
5. Use practical low power design techniques and their analysis at various levels of design abstraction and analyse how these are being captured in the latest design automation environments.

**Question paper pattern:**
The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 60.
- The question paper will have ten full questions carrying equal marks.
- Each full question is for 20 marks.
- There will be two full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub question covering all the topics under a module.
- The students will have to answer five full questions, selecting one full question from each module.

**Textbook/ Textbooks**

| Sl No | Title of the book | Name of the Author/s | Publisher Name | Edition and year |
|---|---|---|---|---|
| 1 | Practical Low Power Digital VLSI Design | Gary K. Yeap | Kluwer Academic | 1998 |
| 2 | Low Power Design Methodologies | Jan M.Rabaey, MassoudPedram | Kluwer Academic | 2010 |
| **Reference Books** | | | | |
| 1 | Low-Power CMOS VLSI Circuit Design | Kaushik Roy, Sharat Prasad | Wiley | 2000 |
| 2 | Low power digital CMOS design | A.P.Chandrasekaran and R.W.Broadersen | Kluwer Academic | 1995 |
| 3 | Low power VLSI CMOS circuit design | A Bellamour and M I Elmasri | Kluwer Academic | 1995 |

| M.TECH VLSI DESIGN & EMBEDDED SYSTEMS (EVE)<br>Choice Based Credit System (CBCS) and Outcome Based Education(OBE)<br>SEMESTER -II | | | |
|---|---|---|---|
| **SoC Design** | | | |
| Course Code | 20EVE252 | CIE Marks | 40 |
| TeachingHours/Week (L:T:P) | 4:0:0 | SEE Marks | 60 |
| Credits | 04 | Exam Hours | 03 |

**Module-1**

**ARM Organization and Implementation**: 3-stage pipeline ARM organization, 5-stage pipeline ARM organization, ARM instruction execution, ARM implementation, The ARM coprocessor interface.

**The ARM Instruction Set**: Introduction, Exceptions, Conditional execution, Branch and Branch withLink (B, BL), Branch, Branch with Link and eXchange (BX, BLX), Software Interrupt (SWI), Dataprocessing instructions, Multiply instructions, Count leading zeros (CLZ - architecture v5T only), Single word and unsigned byte data transfer instruction, Half-word and signed byte data transfer instructions, Multiple register transfer instructions, Swap memory and register instructions (SWP), Status register to general register transfer instructions, General register to status register transfer instructions, Coprocessor instructions, Coprocessor data operations, Coprocessor data transfers,Coprocessor register transfers, Breakpoint instruction (BRK - architecture v5T only), Unused instruction space, Memory faults, ARM architecture variants.

**Module-2**

**Architectural Support for High-Level Languages**: Abstraction insoftware design, Data types, Floating-point data types, The ARM floating-point architecture, Expressions, Conditional statements,Loops, Functions and procedures, Use of memory, Run-timeenvironment.

**Architectural Support for System Development**: The ARMmemory interface, The Advanced Microcontroller Bus Architecture(AMBA), The ARM reference peripheral specification, Hardware system prototyping tools, The ARMulator, The JTAG boundaryscan test architecture, The ARM debug architecture, EmbeddedTrace, Signal processing support.

**Module-3**

**ARM Processor Cores**: ARM7TDMI, ARM8, ARM9TDMI, ARM10TDMI, Discussion, Example and exercises.

**Memory Hierarchy**: Memory size and speed, On-chip memory, Caches, Cache design - an example, Memory management, Examples and exercises.

**Module-4**

**Architectural Support for Operating Systems**: An introduction to operating systems, The ARM system control coprocessor, CP15 protection unit registers, ARM protection unit, CP15 MMU registers, ARM MMU architecture, Synchronization, Context switching, Input/ Output, Example and exercises.

**ARM CPU Cores**: The ARM710T, ARM720T and ARM740T, The ARM810, The Strong ARM SA-110, The ARM920T and ARM940T, The ARM946E-S and ARM966E-S, The ARM1020E, Discussion, Example and exercises.

**Module-5**

**Embedded ARM Applications**: The VLSI Ruby II Advanced Communication Processor, The VLSI ISDN Subscriber Processor, The One C™VWS22100 GSM chip, The Ericsson-VLSI BluetoothBaseband Controller, The ARM7500 and ARM7500FE, The ARM7100 364, The SA-1100 368, Examples and exercises.

**The AMULET Asynchronous ARM Processors**: Self-timed design 375, AMULET1 377,AMULET2 381, AMULET2e 384, AMULET3 387, The DRACO telecommunications controller 390, A self-timed future? 396, Example and exercises.

**Course outcomes:**

At the end of the course the student will be able to:

1. Apply the 3- and 5-stage pipeline ARM processor cores and analyse the implementation issues.
2. Use the concepts and methodologies employed in designing a System- on-chip (SoC) based around a microprocessor core and in designing the microprocessor core itself.
3. Understand how SoCs and microprocessors are designed and used, and why a modern processor is designed the way that it is.
4. Use integrated ARM CPU cores (including StrongARM) that incorporate full support for memory management.
5. Analyze the requirements of a modern operating system and use the ARM architecture to address the same.

**Question paper pattern:**

The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 60.

- The question paper will have ten full questions carrying equal marks.
- Each full question is for 20 marks.

**M.TECH VLSI DESIGN & EMBEDDED SYSTEMS (EVE)**
**Choice Based Credit System (CBCS) and Outcome Based Education(OBE)**
**SEMESTER -II**

## MICRO ELECTRO MECHANICAL SYSTEMS

| | | | |
|---|---|---|---|
| Course Code | 20ELD253 | CIE Marks | 40 |
| TeachingHours/Week (L:T:P) | 4:0:0 | SEE Marks | 60 |
| Credits | 04 | Exam Hours | 03 |

**Module-1**

**Overview of MEMS and Microsystems**: MEMS and Microsystem, Typical MEMS and Microsystems Products, Evolution of Microfabrication, Microsystems and Microelectronics, Multidisciplinary Nature of Microsystems, Miniaturization. Applications and Markets.

**Module-2**

**Working Principles of Microsystems**: Introduction, Microsensors, Microactuation, MEMS withMicroactuators, Microaccelerometers, Microfluidics.

**Engineering Science for Microsystems Design and Fabrication**: Introduction, Atomic Structure of Matters, Ions and Ionization, Molecular Theory of Matter and Inter-molecular Forces, Doping ofSemiconductors, The Diffusion Process, Plasma Physics, Electrochemistry.

**Module-3**

**Engineering Mechanics for Microsystems Design**: Introduction, Static Bending of Thin Plates, Mechanical Vibration, Thermomechanics, Fracture Mechanics, Thin Film Mechanics, Overview on Finite Element Stress Analysis.

**Module-4**

**Scaling Laws in Miniaturization**:
Introduction, Scaling in Geometry, Scaling in Rigid-BodyDynamics, Scaling in Electrostatic Forces, Scaling of Electromagnetic Forces, Scaling in Electricity, Scaling in Fluid Mechanics, Scaling in Heat Transfer.

**Module-5**

**Overview of Micro-manufacturing**: Introduction, Bulk Micro-manufacturing, Surface Micromachining, The LIGA Process, Summary on Micromanufacturing.
**Microsystem Design**: Introduction, Design Considerations, Process Design, Mechanical Design, Using Finite Element Method.

**Course outcomes:**
At the end of the course the student will be able to:
1. Understand the technologies related to Micro Electro Mechanical Systems.
2. Relate to the scaling laws in miniaturization.
3. Analyse the MEMS devices and develop suitable mathematical models
4. Understand the various application areas for MEMS devices
5. Describe the design and fabrication processes involved with MEMS devices.

**Question paper pattern:**
The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 60.
- The question paper will have ten full questions carrying equal marks.
- Each full question is for 20 marks.
- There will be two full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub question covering all the topics under a module.
- The students will have to answer five full questions, selecting one full question from each module.

**Textbook/ Textbooks**

| Sl No | Title of the book | Name of the Author/s | Publisher Name | Edition and year |
|---|---|---|---|---|
| 1 | MEMS and Micro systems: Design, Manufacture and Nanoscale Engineering | Tai-Ran Hsu | John Wiley & Sons ISBN: 978-0470-08301-7 | 2nd Edition, 2008 |

**Reference Books**

| | | | | |
|---|---|---|---|---|
| 1 | Micro and Nano Fabrication: Tools and Processes | Hans H. Gatzen, Volker Saile, Jurg Leuthold | Springer | 2015 |
| 2 | Micro Electro Mechanical Systems (MEMS) | Dilip KumarBhattacharya, Brajesh Kumar Kaushik | Cengage Learning. | |

**M.TECH VLSI DESIGN & EMBEDDED SYSTEMS (EVE)**

**Choice Based Credit System (CBCS) and Outcome Based Education(OBE)**
**SEMESTER -II**

**HIGH FREQUENCY GaN ELECTRONIC DEVICES**

| | | | |
|---|---|---|---|
| Course Code | 20EVE254 | CIE Marks | 40 |
| TeachingHours/Week (L:T:P) | 4:0:0 | SEE Marks | 60 |
| Credits | 04 | Exam Hours | 03 |

**Module-1**

**Introduction and Overview**:
**High Power High Frequency Transistors**: A Material's Perspective: Introduction, Johnson's Figure of Merit, Output Power Figure of Merit 2, Achieving Mobile Carriers for Wide Band Gap Semiconductors, Low Field Mobility Considerations, Channel Temperature Considerations, Heterojunction Advantages (Chapter 2).

**Module-2**

**Isotope Engineering of GaN for Boosting Transistor Speeds**: Introduction, Current Saturation, The Effect of Non-equilibrium LO Phonons is Twofold, Derivation of the Electron-LO Phonon Interaction Hamiltonian, Evaluating the Probability of Scattering into the LO Phonon Mode q, Evaluation of the Phonon Population in Each Mode, Momentum Relaxation Time, Calculating Velocity vs. Field Dependence, Analysis, "Creative Disorder", Summary of the Theoretical Analysis, Experimental Feasibility of Introducing Isotopic Disorder in GaN HEMTs (Chapter 3).
**Linearity Aspects of High Power Amplification in GaN Transistors**: "Creative Disorder", Summary of the Theoretical Analysis, Experimental Feasibility of Introducing Isotopic Disorder in GaN HEMTs, Overview of Non-linearity and Its Impacts, Trade-Offs Against Other Metrics, Origins of Non-linearity in GaN HEMTs, Transconductance, Capacitance, Self-heating, Trapping, Large-Signal Modelling, Special Concerns for GaN, Available Models, Physically Derived Models, Circuit Models, Device-Level Design for Linearity, Linearizing the Transconductance Profile, BRIDGE FET Technology, Field Plate Technology, Circuit-Level Techniques for Linearity (Chapter 4).

**Module-3**

**III-Nitride Tunneling Hot Electron Transfer Amplifier (THETA)**:
Overview of the Chapter Analysis of Hot Electron Transport and Monte Carlo Simulation, Electron Transport Scattering Mechanisms, Monte Carlo Simulation Small Signal Models for High-Frequency Performance ,Effect of Base Thickness and Doping on β, gm, Delay Component, ft, and fmax, Effect of Emitter-Base Current Density on Delay Component, ft, and fmax , Unipolar Transport in III-Nitride Alloys, Polarization-Engineered Vertical Barriers, Leakage in Vertical AlGaN/GaN Heterojunctions, Polarization-Engineered Base-Collector Barriers, Design, Growth, Fabrication, and Characterization of THETA ,Generation I: Common-Emitter Current Gain , Ga Polar THETA with Current Gain >1, N Polar THETA Hot Electron Transport in Vertical AlGaN/GaN Heterostructures, Negative Differential Resistance in III-Nitride THETA, Generation II: Current Gain > 10 in III-Nitride HETs , Emitter-Base Barrier Engineering, Current Gain Above 10 in III-Nitride HETs, Effect of Barrier Thickness on Current Gain (Chapter 5).

**Module-4**

**Plasma-Wave Propagation in GaN and Its Applications**:
Electron PlasmaWaves: Physical Origin, Drude Conductivity and Distributed Models for HEMTs, Hydrodynamic Transport Equations and Non-linear Effects, Electron PlasmaWaves in GaN Experimental Demonstration, Direct Electrical Probing, Quasi-Optical Excitation, Prospective Applications, RTD-Gated HEMT (Chapter 6).

**Numerical Simulation of Distributed Electromagnetic and Plasma Wave Effect Devices**: Hydrodynamic Modeling of the 2DEG Channel ,Electrodynamic Equations (or Maxwell's Equation), Finite Difference Time Domain (FDTD) Solution, Time-Space Discretization of HD Equations, Time-Space Discretization of Maxwell's Equation 4 Verification Using Analytical Models and Experimental Data , Model Validation Via Analytical Method , Model Validation Via Prior Measurements 5 HEMT-Based Terahertz Emitters Using PlasmaWave Instability , Modeling of HEMT-Based Terahertz Emitters, Full-Wave Hydrodynamic Modeling of Terahertz Emissions from an Short Channel HEMT [24], Dyakonov-Shur Instability, Instability Mechanism , Instability in Ungated InGaAs HEMT, Effects of Velocity Saturation and Reduced Mobility, RTD-Assisted Amplification of Plasmons in HEMTs, Full-Wave Modeling of RTD-Gated HEMT: Validation and Results, Comparison of Numerical and Analytical Solutions, Plasmon Propagation in RTD-Gated GaN/AlGaN Heterojunctions, Experimental Work for Confirmation of Plasma Modes in 2DEG Sample, Capacitively-Coupled HEMT Device, Fabrication and Measurements (Chapter 7).

| M.TECH VLSI DESIGN & EMBEDDED SYSTEMS (EVE)<br>Choice Based Credit System (CBCS) and Outcome Based Education(OBE)<br>SEMESTER -II | | | |
|---|---|---|---|
| VLSI & ES Lab-2 | | | |
| Course Code | 20EVEL26 | CIE Marks | 40 |
| TeachingHours/Week (L:T:P) | 0:0:4 | SEE Marks | 60 |
| Credits | 02 | Exam Hours | 03 |

| Sl. NO | Experiments |
|---|---|
| | **PART A: VLSI Design.**<br>**Experiments to be conducted using suitable CAD tool** |
| 1 | Design an Inverter with given specifications*, completing the design flow mentioned below:<br>a. Draw the schematic and verify the following<br>i) DC Analysis<br>ii) Transient Analysis<br>b. Draw the Layout and verify the DRC, ERC<br>c. Check for XX<br>d. Extract RC and back annotate the same and verify the Design<br>e. Verify & Optimize for Time, Power and Area to the given constraint*** |
| 2 | Design the following circuits with given specifications*, completing the design flow mentioned below:<br>a. Draw the schematic and verify the following<br>i) DC Analysis<br>ii) AC Analysis<br>iii) Transient Analysis<br>b. Draw the Layout and verify the DRC, ERC, LVS<br>c. Check for XX<br>d. Extract RC and back annotate the same and verify the Design<br>i) Single Stage differential amplifier<br>ii) Common source amplifier<br>iii) Design an op-amp with given specification* using differential amplifier Common source amplifier in library**<br>iv) Design a 4 bit R-2R based DAC for the given specification** |
| 3 | Design an Integrator using OPAMP (First Order) |
| 4 | Design a Differentiator using OPAMP (First Order) |
| 5 | Design and characterize a basic Sigma delta ADC from the available designs. |
| | (Any other experiments may be added in supportive of the course)<br>*Appropriate specification should be given.<br>** Applicable Library should be added & information should be given to the Designer.<br>*** An appropriate constraint should be given |
| | **PART B: RTOS programs using C language in LINUX OS.** |
| 1 | Develop programs to (a) create child process and display its id and<br>(b) Execute child process function using switch structure |
| 2 | Develop and test program for a multithreaded application, where communication is through a buffer for the conversion of lowercase text to uppercase text, using semaphore concept. |
| 3 | Develop and test program for a multithreaded application, where communication is through shared memory for the conversion of lowercase text to uppercase text. |
| 4 | Develop program for inter-thread communication using message queue.<br>Data is to be input from the keyboard for the chosen application. |

**M.TECH VLSI DESIGN & EMBEDDED SYSTEMS (EVE)**
**Choice Based Credit System (CBCS) and Outcome Based Education(OBE)**
**SEMESTER -II**

**TECHNICAL SEMINAR**

| | | | |
|---|---|---|---|
| Course Code | 20EVE27 | CIE Marks | 100 |
| Number of contact Hours/week (L:T:P) | 0:0:2 | SEE Marks | -- |
| Credits | 02 | Exam Hours | -- |

**Course objectives:**

The objective of the seminar is to inculcate self-learning, face audience confidently, enhance communication skill, involve in group discussion and present and exchange ideas.

Each student, under the guidance of a Faculty, is required to

- Choose, preferably through peer reviewed journals, a recent topic of his/her interest relevant to the Course of Specialization.
- Carryout literature survey, organize the Course topics in a systematic order.
- Prepare the report with own sentences.
- Type the matter to acquaint with the use of Micro-soft equation and drawing tools or any such facilities.
- Present the seminar topic orally and/or through power point slides.
- Answer the queries and involve in debate/discussion.
- Submit two copies of the typed report with a list of references.

The participants shall take part in discussion to foster friendly and stimulating environment in which the students are motivated to reach high standards and become self-confident.

The CIE marks for the seminar shall be awarded (based on the relevance of the topic, presentation skill, participation in the question and answer session and quality of report) by the committee constituted for the purpose by the Head of the Department. The committee shall consist of three faculties from the department with the senior most acting as the Chairperson.

**Marks distribution for CIE of the course 20XXX27 seminar:**

Seminar Report: 50 marks
Presentation skill:25 marks
Question and Answer:25 marks

**M.TECH VLSI DESIGN & EMBEDDED SYSTEMS (EVE)**
**Choice Based Credit System (CBCS) and Outcome Based Education(OBE)**
**SEMESTER -III**

**CAD of DIGITAL SYSTEMS**

| | | | |
|---|---|---|---|
| Course Code | 20EVE31 | CIE Marks | 40 |
| TeachingHours/Week (L:T:P) | 4:0:0 | SEE Marks | 60 |
| Credits | 04 | Exam Hours | 03 |

**Module-1**

**Introduction to Design Methodologies**: The VLSI Design Problem, The Design Domains, Design Actions, Design Methods and Technologies.
**VLSI Design Automation tools**: Algorithmic and System Design, Structural and Logic Design, Transistor-level Design, Layout Design, Verification Methods, Design Management Tools.
**Algorithmic graph theory and computational complexity**: Terminology, Data Structures for the Representation of Graphs, Computational Complexity, Examples of Graph Algorithms.
**Tractable and intractable problems**: Decision Problems, Complexity Classes, NP-completeness and NP-hardness, Consequences.

**Module-2**

**General purpose methods for combinational optimization**: Backtracking and Branch-and-bound, Dynamic Programming, Integer Linear Programming, Local Search, Simulated Annealing, Tabu Search, Genetic Algorithms, A Few Final Remarks on General-purpose Methods.
**Layout compaction**: Design Rules, Symbolic Layout, Problem Formulation, Algorithms for Constraint-graph Compaction, Other Issues.

**Module-3**

**Placement and partitioning**: Circuit Representation, Wire-length Estimation, Types of Placement Problem, Placement Algorithm, Partitioning.
**Floor planning**: Floor planning Concepts, Shape Functions and Floorplan Sizing.

**Module-4**

**Routing**: Types of Local Routing Problems, Area Routing, Channel Routing, Introduction to Global Routing, Algorithms for Global Routing.
**Simulation**: General Remarks on VlSl Simulation, Gate-level Modeling and Simulation, Switch-level Modeling and Simulation.

**Module-5**

**Logic Synthesis and Verification**: Introduction to Combinational Logic Synthesis, Binary-decision Diagrams, Two-level Logic Synthesis
**High level synthesis**: Hardware Models for High Level Synthesis, Internal Representation of the Input Algorithm, Allocation, Assignment and Scheduling, Some Scheduling Algorithm, Some Aspects of the Assignment Problem, High-level Transformations.

**Course outcomes:**
At the end of the course the student will be able to:
1. Understand the various design methodologies.
2. Solve graph theoretic problems.
3. Evaluate the computational complexity of an algorithm.
4. Write algorithms for VLSI Automation.
5. Simulate and synthesize digital circuits using VLSI automation tools.

**Question paper pattern:**
The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 60.
- The question paper will have ten full questions carrying equal marks.
- Each full question is for 20 marks.
- There will be two full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub question covering all the topics under a module.
- The students will have to answer five full questions, selecting one full question from each module.

**Students have to conduct the following experiments as a part of CIE marks along with other Activities:**

Implement the following in C/C++/NS3
1. Dijkstar's algorithm to find the shortest routing path.
2. Depth first search (DFS) and breadth first search (BFS) graph traversal algorithm.
3. Prim's algorithm to construct Minimum Spanning Tree.
4. Backtracking algorithm for space optimization.
5. Dynamic Programming and Linear Programming.

**M.TECH VLSI DESIGN & EMBEDDED SYSTEMS (EVE)**
**Choice Based Credit System (CBCS) and Outcome Based Education(OBE)**

**SEMESTER -III**

**Machine Learning in VLSI CAD**

| | | | |
|---|---|---|---|
| Course Code | 20EVE321 | CIE Marks | 40 |
| TeachingHours/Week (L:T:P) | 3:0:0 | SEE Marks | 60 |
| Credits | 03 | Exam Hours | 03 |

**Module-1**

**A Preliminary Taxonomy for Machine Learning in VLSI CAD**
Machine learning taxonomy, VLSI CAD Abstraction levels (Text Book:1 – 1.1, 1.2)
**Machine Learning for Compact Lithographic Process Models**
Introduction, Lithographic Patterning Process, Representation of Lithographic Patterning Process – Mask, Imaging, Resist & Etch Transfer Function (Text Book:1 – 2.1, 2.2).

**Module-2**

**Machine Learning of Compact Lithographic Process Models (Cont.,)**
Compact process model machine learning problem statement, CPM Task, CPM Training Experience, Performance metrics, Supervised learning of a CPM (Text. Book:1 – 2.3)
**Neural Network Compact Patterning Models**
Neural Network Mask Transfer Function, Neural Network Image Transfer Function, Neural Network Resist Transfer Function, Neural Network Etch Transfer Function (Text. Book:1 – 2.4).

**Module-3**

**Machine Learning for Mask Synthesis**
Introduction, Machine Learning guided OPC, MLP Construction, ML-EPC, EPC Algorithm (TextBook:1 – 3.1, 3.2, 3.2.2.2, 3.3.2, 3.3.2.4).
**Machine Learning in Physical Verification**
Introduction, Machine Learning in Physical Verification – layout feature extraction & encoding, models for hotspot detection.
(Text.Book:1 – 4.1, 4.2)

**Module-4**

**Machine Learning in Mask Synthesis and Physical Design:**
Machine Learning inMask Synthesis – mask synthesis flow, Machine Learning for sub-resolution assist features, Machine Learning for optical proximity correction.
Machine Learning inPhysical Design - for datapath placement, routability driven placement, clock optimization, lithography friendly routing (Text Book: 1 – 4.3, 4.4).
**Machine Learning for Manufacturing**
Gaussian Process-Based Wafer-Level Correlation Modeling and Its Applications
(Text Book: 1 – 5.1).

**Module-5**

**Machine Learning for Yield and Reliability:**
High-volume manufacturing yield estimation – Histogram with random sampling, Histogram with GP-ST-PS, Kernel density estimation. (Text Book: 1 – 5.2.11).
Machine learning based aging analysis (Text Book: 1 – 9.1).
Learning from limited data in VLSI CAD, Iterative feature search (Text Book: 1 – 13.1, 13.2).
Comparative study of Assertion mining algorithms in GoldMine (Text Book: 1 – 20.1).

**Course outcomes:**
At the end of the course the student will be able to:

1. Use machine learning technologies in VLSI CAD to further automate the design, verification and implementation of the most advanced chips.
2. Relate to the usage of machine learning algorithms for Compact Lithographic Process Models.
3. Apply Machine Learning in Mask Synthesis and Physical Verification to bear on CAD problems such as hot-spot detection, efficient test generation, post-silicon measurement minimization.
4. Predict the Yield and Reliability of VLSI chips using machine learning methods.
5. Comprehend the appropriate application of the various supervised, unsupervised and statistical learning in the various layers of chip design hierarchy.

**M.TECH VLSI DESIGN & EMBEDDED SYSTEMS (EVE)**
**Choice Based Credit System (CBCS) and Outcome Based Education(OBE)**
**SEMESTER -III**

**CMOS RF Circuit Design**

| | | | |
|---|---|---|---|
| Course Code | 20EVE322 | CIE Marks | 40 |
| TeachingHours/Week (L:T:P) | 3:0:0 | SEE Marks | 60 |
| Credits | 03 | Exam Hours | 03 |

**Module-1**

**Introduction to RF Design, Wireless Technology and Basic Concepts**: A wireless world, RF design is challenging, The big picture. General considerations, Effects of Nonlinearity, Noise, Sensitivity and dynamic range, Passive impedance transformation. Scattering parameters, Analysis of nonlinear dynamic systems, conversion of gains and distortion

**Module-2**

**Communication Concepts**: General concepts, analog modulation, digital modulation, spectral re-growth, coherent and non-coherent detection, Mobile RF communications, Multiple access techniques, Wireless standards, Appendix 1: Differential phase shift keying.

**Module-3**

**Transceiver Architecture**: General considerations, Receiver architecture, Transmitter architectures, Direct conversion and two-step transmitters, RF testing for heterodyne, Homodyne, Image reject, Direct IF and sub sampled receivers.

**Module-4**

**Low Noise Amplifiers and Mixers**: General considerations, Problem of input matching, LNAtopologies: common-source stage with inductive load, common-source stage with resistive feedback.
Mixers-General considerations, passive down conversion mixers, Various mixers- working and implementation.

**Module-5**

**VCO and PLLs**- Oscillators- Basic topologies VCO and definition of phase noise, Noise power and trade off. Resonator VCO designs, Quadrature and single sideband generators. Radio frequency Synthesizers- PLLS, Various RF synthesizer architectures and frequency dividers, Power Amplifier design.

**Course outcomes:**
At the end of the course the student will be able to:

1. Analyse the effect of nonlinearity and noise in RF and microwave design.
2. Exemplify the approaches taken in actual RF products.
3. Minimize the number of off-chip components required to design mixers, Low-Noise Amplifiers, VCO and PLLs.
4. Explain various receivers and transmitter topologies with their merits and drawbacks.
5. Demonstrate how the system requirements define the parameters of the circuits and the impact on the performance

**Question paper pattern:**
The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 60.

- The question paper will have ten full questions carrying equal marks.
- Each full question is for 20 marks.
- There will be two full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub question covering all the topics under a module.
- The students will have to answer five full questions, selecting one full question from each module.

**Textbook/ Textbooks**

| Sl No | Title of the book | Name of the Author/s | Publisher Name | Edition and year |
|---|---|---|---|---|
| 1 | RF Microelectronics | B. Razavi | PHI | second edition |
| **Reference Books** | | | | |
| 1 | CMOS Circuit Design, layout and Simulation | R. Jacob Baker, H.W. Li, D.E. Boyce | PHI | 1998 |
| 2 | Design of CMOS RF Integrated Circuits | Thomas H. Lee | Cambridge University press | 1998 |
| 3 | Mixed Analog and Digital Devices and Technology | Y.P. Tsividis | TMH | 1996 |

**M.TECH VLSI DESIGN & EMBEDDED SYSTEMS (EVE)**
**Choice Based Credit System (CBCS) and Outcome Based Education(OBE)**
**SEMESTER -III**

**Embedded Linux System Design and Development**

| | | | |
|---|---|---|---|
| Course Code | 20EVE323 | CIE Marks | 40 |
| TeachingHours/Week (L:T:P) | 3:0:0 | SEE Marks | 60 |
| Credits | 03 | Exam Hours | 03 |

**Module-1**

**Introduction**: History of Embedded Linux, Why Embedded Linux, Embedded Linux Versus Desktop Linux, Frequently Asked Questions, Embedded Linux Distributions, Porting Roadmap.
**Getting Started:** Architecture of Embedded Linux, Linux Kernel Architecture, User Space, Linux Start-Up Sequence, GNU CrossPlatform Tool chain.

**Module-2**

**Board Support Package**: Inserting BSP in Kernel Build Procedure, Memory Map, Interrupt Management, The PCI Subsystem, Timers, UART, Power Management.

**Module-3**

**Embedded Storage**: Flash Map, MTD—Memory Technology Device, MTD Architecture, Sample MTD Driver for NOR Flash, The Flash-Mapping Drivers, MTD Block and Character Devices,Mtdutils Package, Embedded File Systems, Optimizing Storage Space, Tuning Kernel Memory.

**Module-4**

**Embedded Drivers**: Linux Serial Driver, Ethernet Driver , I2C Subsystem on Linux, USB Gadgets, Watchdog Timer, Kernel Modules.

**Module-5**

**Porting Applications**: Architectural Comparison, Application Porting Roadmap, Programming with Pthreads, Operating System Porting Layer (OSPL), Kernel API Driver.

**Course outcomes:**
At the end of the course the student will be able to:
1. Understand the embedded Linux development environment.
2. Understand and create Linux BSP for a hardware platform.
3. Understand the Linux model for embedded storage and write drivers and applications for the same.
4. Understand various embedded Linux drivers such as serial, I2C, and so on.
5. Port applications to embedded Linux from a traditional RTOS.

**Question paper pattern:**
The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 60.

- The question paper will have ten full questions carrying equal marks.
- Each full question is for 20 marks.
- There will be two full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub question covering all the topics under a module.
- The students will have to answer five full questions, selecting one full question from each module.

**Textbook/ Textbooks**

| Sl No | Title of the book | Name of the Author/s | Publisher Name | Edition and year |
|---|---|---|---|---|
| 1 | Embedded Linux System Design And Development | P.Raghavan, Amol Lad, Sriram Neelakandan | Auerbach Publications, Taylor & Francis Group | 2006 |
| **Reference Books** | | | | |
| 1 | Building Embedded Linux Systems | Karim Yaghmour, Jon Masters, Gilad Ben-Yossef, and Philippe Gerum | O'Reilly publications | 2nd edition |

**M.TECH VLSI DESIGN & EMBEDDED SYSTEMS (EVE)**
**Choice Based Credit System (CBCS) and Outcome Based Education(OBE)**
**SEMESTER -III**

**Advanced Computer Architecture**

| | | | |
|---|---|---|---|
| Course Code | 20EVE324 | CIE Marks | 40 |
| TeachingHours/Week (L:T:P) | 3:0:0 | SEE Marks | 60 |
| Credits | 03 | Exam Hours | 03 |

**Module-1**

**Parallel Computer Models**: The State of Computing, Multiprocessors and multicomputers, Multivector and SIMD computers.
**Program and Network Properties**: Conditions of parallelism, Program Partitioning & Scheduling, Program Flow Mechanisms.

**Module-2**

**Principles of Scalable Performance**: Performance Metrics and Measures, Parallel Processing Applications, Speedup Performance Laws, Scalability Analysis and Approaches.
**Processors & Memory Hierarchy**: Advanced processor technology, Super Scalars & Vector Processors, Memory Hierarchy Technology, Virtual Memory Technology.

**Module-3**

**Bus, Cache and Shared Memory**: Bus Systems, Cache Memory Organizations, Shared Memory Organizations, Sequential & Weak Consistency Model.
**Pipelining & Superscalar Technologies**: Linear Pipeline Processors, Nonlinear Pipeline Processors, Instruction Pipeline Design, Arithmetic Pipeline Design, Superscalar Pipeline Design.

**Module-4**

**Multivector& SIMD Computers**: Vector Processing principles, Multivector Multiprocessors, Compound Vector Processing, SIMD Computer Organization.
**Scalable, Multithreaded and Data Flow Computers**: Latency Hiding Techniques, Principles of Multithreading, Fine Grain Multi Computers, Scalable and Multithreaded Architectures, Data Flow and Hybrid Architectures.

**Module-5**

**Parallel Models, Languages and Compilers**: Parallel Programming Models, Parallel Languages & Compilers, Dependence Analysis and Data Arrays, Code Optimization and Scheduling, Loop Parallelization and Pipelining.
**Parallel Program Development and Environments**: Parallel Programming Environments, Synchronization and Multi Processor Modes, Shared Variable Program Structures.

**Course outcomes:**
At the end of the course the student will be able to:
1. Understand the basic concepts for parallel processing
2. Analyze program partitioning and flow mechanisms
3. Apply pipelining concept for the performance evaluation
4. Learn the advanced processor architectures for suitable applications
5. Understand parallel Programming

**Question paper pattern:**
The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 60.

- The question paper will have ten full questions carrying equal marks.
- Each full question is for 20 marks.
- There will be two full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub question covering all the topics under a module.
- The students will have to answer five full questions, selecting one full question from each module.

**Textbook/ Textbooks**

| Sl No | Title of the book | Name of the Author/s | Publisher Name | Edition and year |
|---|---|---|---|---|
| 1 | Advanced Computer Architecture: Parallelism, Scalability, Programmability | Kai Hwang & Narendra Jotwani | McGraw Hill Education, ISBN: 978-93-392-2092-1 | 3rd Edition, 2016 |
| **Reference Books** | | | | |
| 1 | Computer Architecture, Pipelined and Parallel Processor Design | M.J. Flynn | Narosa Publishing | 2002 |
| 2 | Parallel programming in C with MPI and OpenMP | Michael J Quinn | Tata McGraw Hill | 2013 |
| 3 | An Introduction to Parallel Computing: Design and Analysis of Algorithms | Ananth Grama | Pearson | 2nd Edition, 2004 |

**M.TECH VLSI DESIGN & EMBEDDED SYSTEMS (EVE)**
**Choice Based Credit System (CBCS) and Outcome Based Education(OBE)**
**SEMESTER -III**

**VLSI Design for Signal Processing**

| | | | |
|---|---|---|---|
| Course Code | 20EVE331 | CIE Marks | 40 |
| TeachingHours/Week (L:T:P) | 3:0:0 | SEE Marks | 60 |
| Credits | 03 | Exam Hours | 03 |

**Module-1**

**Introduction to DSP Systems**: Typical DSP Algorithms, DSP Application Demands and Scaled CMOS Technologies, Representations of DSP Algorithms.
**Iteration Bounds**: Data flow graph Representations, loop bound and Iteration bound. Algorithms for Computing Iteration Bound, Iteration Bound of multi rate data flow graphs.

**Module-2**

**Pipelining and Parallel Processing**: pipelining of FIR Digital Filters, parallel processing, Pipelining and parallel processing for low power.
**Retiming**: Definition and Properties, Solving Systems of Inequalities, Retiming Techniques.

**Module-3**

**Unfolding**: An Algorithm for Unfolding, Properties of Unfolding, Critical path, Unfolding and Retiming, Application of Unfolding.
**Folding**: Folding Transformation, Register Minimization Techniques, Register Minimization in Folded Architectures, Folding of Multirate Systems.

**Module-4**

**Systolic Architecture Design**: systolic array design Methodology, FIR systolic array, Selection of Scheduling Vector, Matrix-Matrix Multiplication and 2D systolic Array Design, Systolic Design forspace representation containing Delays.
**Fast convolution**: Cook-Toom Algorithm, Winograd Algorithm, Iterated convolution, cyclic convolution Design of fast convolution Algorithm by Inspection.

**Module-5**

**Pipelined and Parallel Recursive and Adaptive Filter**: Pipeline Interleaving in Digital Filter, first order IIR digital Filter, Higher order IIR digital Filter, parallel processing for IIR filter, Combinedpipelining and parallel processing for IIR Filter, Low power IIR Filter Design Using Pipelining and parallel processing, pipelined adaptive digital filter.

**Course outcomes:**
At the end of the course the student will be able to:
1. Illustrate the use of various DSP algorithms and addresses their representation using block diagrams, signal flow graphs and data-flow graphs
2. Use pipelining and parallel processing in design of high-speed /low-power applications
3. Apply unfolding in the design of parallel architecture
4. Evaluate the use of look-ahead techniques in parallel and pipelined IIR Digital filters.
5. Develop an algorithm or architecture or circuit design for DSP applications

**Question paper pattern:**
The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 60.
- The question paper will have ten full questions carrying equal marks.
- Each full question is for 20 marks.
- There will be two full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub question covering all the topics under a module.
- The students will have to answer five full questions, selecting one full question from each module.

**Textbook/ Textbooks**

| Sl No | Title of the book | Name of the Author/s | Publisher Name | Edition and year |
|---|---|---|---|---|
| 1 | VLSI Digital Signal Processing systems, Design and implementation | Keshab K.Parthi | Wiley | 1999 |
| **Reference Books** | | | | |
| 1 | Analog VLSI Signal and Information Processing | Mohammed Isamail and Terri Fiez | Mc Graw-Hill | 1994 |
| 2 | VLSI and Modern Signal Processing | S.Y. Kung, H.J. White House, T. Kailath | Prentice Hall | 1985 |
| 3 | Design of Analog - Digital VLSI Circuits for Telecommunication and Signal Processing | Jose E. France, Yannis Tsividis | Prentice Hall | 1994 |
| 4 | DSP Integrated Circuits | Lars Wanhammar | Academic Press Series in Engineering | 1st Edition |

**M.TECH VLSI DESIGN & EMBEDDED SYSTEMS (EVE)**
**Choice Based Credit System (CBCS) and Outcome Based Education(OBE)**
**SEMESTER -III**

**Pattern Recognition & Machine Learning**

| | | | |
|---|---|---|---|
| Course Code | 20ESP332 | CIE Marks | 40 |
| TeachingHours/Week (L:T:P) | 3:0:0 | SEE Marks | 60 |
| Credits | 03 | Exam Hours | 03 |

**Module-1**

**Introduction**: Probability Theory, Model Selection, The Curse of Dimensionality, Decision Theory, Information Theory
**Distributions**: Binary and Multinomial Variables, The Gaussian Distribution, The Exponential Family, Nonparametric Methods. (Ch.: 1,2)

**Module-2**

**Supervised Learning**
**Linear Regression Models**: Linear Basis Function Models, The Bias-Variance Decomposition, Bayesian Linear Regression, Bayesian Model Comparison
**Classification & Linear Discriminant Analysis**: Discriminant Functions, Probabilistic Generative Models, Probabilistic Discriminative Mode (Ch.:3,4).

**Module-3**

**Supervised Learning**
**Kernels**: Dual Representations, Constructing Kernels, Radial Basis Function Network, Gaussian Processes
**Support Vector Machines**: Maximum Margin Classifiers, Relevance Vector Machines
**Neural Networks**: Feed-forward Network, Network Training, Error Backpropagation (Ch:5,6,7).

**Module-4**

**Unsupervised Learning:**
**Mixture Models**: K-means Clustering, Mixtures of Gaussians, Maximum likelihood, EM for Gaussian mixtures, Alternative View of EM.
**Dimensionality Reduction**: Principal Component Analysis, Factor/Component Analysis, Probabilistic PCA, Kernel PCA, Nonlinear Latent Variable Models (Ch.: 9,12).

**Module-5**

**Probabilistic Graphical Models**: Bayesian Networks, Conditional Independence, Markov Random Fields, Inference in Graphical Models, Markov Model, Hidden Markov Models (Ch.:8,13)

**Course outcomes:**
At the end of the course the student will be able to:
1. Identify areas where Pattern Recognition and Machine Learning can offer a solution.
2. Describe the strength and limitations of some techniques used in computational Machine Learning for classification, regression and density estimation problems.
3. Describe and model data.
4. Solve problems in Regression and Classification.
5. Discuss main and modern concepts for model selection and parameter estimation in recognition, decision making and statistical learning problems.

**Question paper pattern:**
The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 60.
- The question paper will have ten full questions carrying equal marks.
- Each full question is for 20 marks.
- There will be two full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub question covering all the topics under a module.
- The students will have to answer five full questions, selecting one full question from each module.

**Textbook/ Textbooks**

| Sl No | Title of the book | Name of the Author/s | Publisher Name | Edition and year |
|---|---|---|---|---|
| 1 | Pattern Recognition and Machine Learning | Christopher Bishop | Springer | 2006 |

**M.TECH VLSI DESIGN & EMBEDDED SYSTEMS (EVE)**
**Choice Based Credit System (CBCS) and Outcome Based Education(OBE)**
**SEMESTER -III**

**Internet of Things**

| | | | |
|---|---|---|---|
| Course Code | 20ECS333 | CIE Marks | 40 |
| TeachingHours/Week (L:T:P) | 3:0:0 | SEE Marks | 60 |
| Credits | 03 | Exam Hours | 03 |

**Module-1**

**What is IoT ?**
Genesis, Digitization, Impact, Connected Roadways, Buildings, Challenges
**IoT Network Architecture and Design**
Drivers behind new network Architectures, Comparing IoT Architectures, M2M architecture, IoT world forum standard, IoT Reference Model, Simplified IoT Architecture.

**Module-2**

**IoT Network Architecture and Design**
Core IoT Functional Stack, Layer1(Sensors and Actuators), Layer 2(Communications Sublayer), Access network sublayer, Gateways and backhaul sublayer, Network transport sublayer,IoT Network management.
Layer 3(Applications and Analytics) – Analytics vs Control, Data vs Network Analytics, IoT Data Management and Compute Stack

**Module-3**

**Engineering IoT Networks**
Things in IoT – Sensors, Actuators, MEMS and smart objects.
Sensor networks, WSN, Communication protocols for WSN
Communications Criteria, Range, Frequency bands, power consumption, Topology, Constrained Devices, Constrained Node Networks
IoT Access Technologies, IEEE 802.15.4
Competitive Technologies – Overview only of IEEE 802.15.4g, 4e, IEEE 1901.2a
Standard Alliances – LTE Cat0, LTE-M, NB-IoT

**Module-4**

**Engineering IoT Networks**
IP as IoT network layer, Key Advantages, Adoption, Optimization, Constrained Nodes, Constrained Networks, IP versions, Optimizing IP for IoT.
Application Protocols for IoT – Transport Layer, Application Transport layer, Background only of SCADA, Generic web based protocols, IoT Application Layer
Data and Analytics for IoT – Introduction, Structured and Unstructured data, IoT Data Analytics overview and Challenges.

**Module-5**

**IoT in Industry (Three Use cases)**
IoT Strategy for Connected manufacturing, Architecture for Connected Factory
Utilities – Power utility, IT/OT divide, Grid blocks reference model, Reference Architecture, Primary substation grid block and automation.
Smart and Connected cities –Strategy, Smart city network Architecture, Street layer, city layer, Data center layer, services layer, Smart city security architecture, Smart street lighting.

**Course outcomes:**
At the end of the course the student will be able to:
1. Understand the basic concepts IoT Architecture and devices employed.
2.Analyze the sensor data generated and map it to IoT protocol stack fortransport.
3.Apply communications knowledge to facilitate transport of IoT data overvarious available communications media.
4.Design a use case for a typical application in real life ranging fromsensing devices to analyzing the data available on a server to performtasks on the device.
5. Apply knowledge of Information technology to design of IoT applications (OperationalTechnology).

**Question paper pattern:**
The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 60.

- The question paper will have ten full questions carrying equal marks.
- Each full question is for 20 marks.
- There will be two full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub question covering all the topics under a module.
- The students will have to answer five full questions, selecting one full question from each module.

**M.TECH VLSI DESIGN & EMBEDDED SYSTEMS (EVE)**
**Choice Based Credit System (CBCS) and Outcome Based Education(OBE)**
**SEMESTER -III**

**Long Term Reliability of VLSI Systems**

| | | | |
|---|---|---|---|
| Course Code | 20EVE334 | CIE Marks | 40 |
| TeachingHours/Week (L:T:P) | 3:0:0 | SEE Marks | 60 |
| Credits | 03 | Exam Hours | 03 |

**Module-1**

**Electromigration Reliability**
Why Electromigration Reliability?,Why system-level EM Reliability Management? Physics- based EM Modeling, Electromigration Fundamentals, Stress based EM Modeling and stress diffusion equations, Modeling for transient EM effects and Initial stress conditions, post voiding stress and void volume evolution, compact physics based EM model for a single wire, other relevant EM models and analysis methods. (Text Book:1 – 1.1, 1.2, 2.1 up to 2.6, 2.9).

**Module-2**

**Fast EM Stress Evolution Analysis**
Introduction, The LTI ordinary differential equations for EM stress evolution, The presented Krylov fast EM stress analysis, Numerical results and discussions (Text. Book:1 – 3.1 up to 3.4).

**Module-3**

**EM Assessment for Power Grid Networks**
New power grid reliability analysis method, cross-layout temperature and thermal stress characterization, impact of across-layout temperature and thermal stress on EM. (Text.Book:1 – 7.1, 7.2, 7.4, 7.5).

**Module-4**

**Transistor Aging Effects and Reliability:**
Introduction, Transistor reliability in advanced technology nodes, Transistor Aging, BTI- Bias Temperature Instability, HCI – Hot Carrier Injection, Coupling models for BTI and HCI degradations, RTN – Random Telegraph Noise, TDDB – Time Dependent Dielectric Breakdown. (Text Book: 1 – 13.1, 13.2).

**Module-5**

**Aging Effects in Sequential Elements:**
Introduction, Background: flip flop timing analysis, process variation model, voltage droop model, Robustness analysis, reliability-aware flip-flop design (Text Book: 1 – 16.1 up to 16.4).

**Course outcomes:**
At the end of the course the student will be able to:
1. Comprehend the recent research in the area of interconnect and device reliability.
2. Determine the impact of device-level reliability on system performance, built upon physics-based models.
3. Understand the physics-based EM modeling.
4. Understand the underlying phenomena of BTI, HCI, TDDB leading to device-level reliability degradation.
5. Relate to considerations at the circuit-level with both combinational and sequential elements.

**Question paper pattern:**
The SEE question paper will be set for 100 marks and the marks scored will be proportionately reduced to 60.
- The question paper will have ten full questions carrying equal marks.
- Each full question is for 20 marks.
- There will be two full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub question covering all the topics under a module.
- The students will have to answer five full questions, selecting one full question from each module.

**Textbook**

| Sl No | Title of the book | Name of the Author/s | Publisher Name | Edition and year |
|---|---|---|---|---|
| 1 | Long-Term Reliability of Nanometer VLSI Systems | Sheldon X. D. Tan, Mehdi BaradaranTahoori, Taeyoung Kim, SamanKiamehr, Zeyu | Springer International Publishing | 1st Edition, 2019 ISBN: 978-3-030-26171-9 |