SCHEME OF TEACHING AND EXAMINATION
M.Tech in VLSI DESIGN AND EMBEDDED SYSTEMS

I SEMESTER

Sl. No	Subject Code	Title	Teaching Hours /Week		Examination				Credit
			Theory	Practical/Field Work/ Assignment	Duration	I.A. Marks	Theory/ Practical Marks	Total Marks	
1	16ELD11	Advanced Engineering Mathematics	4	-	3	20	80	100	4
2	16EVE12	Digital VLSI Design	4	-	3	20	80	100	4
3	16EVE13	Advanced Embedded System	4	-	3	20	80	100	4
4	16EVE14	Low Power VLSI Design	4	-	3	20	80	100	4
5	16EXX15X	Elective-1	3	-	3	20	80	100	3
6	16EVEL16	VLSI and ES Lab -1		3	3	20	80	100	2
7	16EVE17	Seminar on advanced topics from refereed journals	-	3	-	100	-	100	1
TOTAL			**19**	**6**	**18**	**220**	**480**	**700**	**22**

Elective -1	
16 EVE151	Digital System Design Using Verilog
16 EVE152	Nanoelectronics
16 EVE153	ASIC Design
16 ELD154	Advanced Computer Architecture

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II SEMESTER

Sl. No	Subject Code	Title	Teaching Hours /Week		Examination				Credit
			Theory	Practical/Field Work/ Assignment	Duration	I.A. Marks	Theory/ Practical Marks	Total Marks	
1	16EVE21	Design of Analog and Mixed mode VLSI Circuits	4	-	3	20	80	100	4
2	16EVE22	VLSI Testing	4	-	3	20	80	100	4
3	16EVE23	Advances in VLSI Design	4	-	3	20	80	100	4
4	16EVE24	Real Time Operating System	4	-	3	20	80	100	4
5	16EXX25X	Elective –2	3	-	3	20	80	100	3
6	16EVEL26	VLSI and ES Lab -2		3	3	20	80	100	2
7	16EVE27	Seminar on Advanced topics from refereed journals	-	3	-	100	-	100	1
TOTAL			**19**	**6**	**18**	**220**	**480**	**700**	**22**

Elective -2	
16EVE251	System Verilog
16EVE252	VLSI Design for Signal processing
16ELD253	Micro Electro Mechanical Systems
16EVE254	SoC Design

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III SEMESTER: Internship

Sl. No	Subject Code	Title	Teaching Hours /Week		Examination				Credit
			Theory	Practical/Field Work/ Assignment	Duration	I.A. Marks	Theory/ Practical Marks	Total Marks	
1	16EVE31	Seminar / Presentation on Internship (After 8 weeks from the date of commencement)	-	-	-	25	-	25	20
2	16EVE32	Report on Internship	-	-	-	25	-	25	
3	16EVE33	Evaluation and Viva-Voce of Internship	-	-	-	-	50	50	
4	16EVE34	Evaluation of Project phase -1	-	-	-	50	-	50	1
TOTAL			**-**	**-**	**-**	**100**	**50**	**150**	**21**

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IV SEMESTER

Sl. No	Subject Code	Title	Teaching Hours /Week		Examination				Credit
			Theory	Practical/Field Work/ Assignment	Duration	I.A. Marks	Theory/ Practical Marks	Total Marks	
1	16ELD41	Synthesis and Optimization of Digital Circuits	4	-	3	20	80	100	4
2	16EXX42X	Elective-3	3	-	3	20	80	100	3
3	16EVE43	Evaluation of Project phase -2	-	-	-	50	-	50	3
4	16EVE44	Evaluation of Project and Viva-Voce	-	-	-	-	100+100	200	10
TOTAL			**-**	**-**	**6**	**90**	**360**	**450**	**20**

Elective -3	
16EVE421	CMOS RF Circuit Design
16ECS422	Advances in Image Processing
16EVE423	High Speed VLSI Design
16ELD424	Reconfigurable Computing

Note:

1. Project Phase-1: 6-week duration shall be carried out between 2nd and 3rd Semester vacation. Candidates in consultation with the guide shall carry out literature survey/ visit industries to finalize the topic of Project.

2. Project Phase-2: 16-week duration during 4th semester**.** Evaluation shall be done by the committee constituted comprising of HoD as Chairman, Guide and Senior faculty of the department.

3. **Project Evaluation**: Evaluation shall be taken up at the end of 4thsemester. Project work evaluation and Viva-Voce examination shall be conducted.

a. Internal Examiner shall carry out the evaluation for 100 marks.

b. External Examiner shall carry out the evaluation for 100 marks.

c .The average of marks allotted by the internal and external examiner shall be the final marks of the project evaluation.

d. Viva-Voce examination of Project work shall be conducted jointly by Internal and External examiner for 100 marks.

ADVANCED ENGINEERING MATHEMATICS [As per Choice Based Credit System (CBCS) scheme] SEMESTER – I			
Subject Code	16ELD11	IA Marks	20
Number of Lecture Hours/Week	04	Exam Marks	80
Total Number of Lecture Hours	50 (10 Hours per Module)	Exam Hours	03
CREDITS – 04			

Course objectives: This course will enable students to:

- Acquaint with principles of linear algebra, calculus of variations, probability theory and random process.
- Apply the knowledge of linear algebra, calculus of variations, probability theory and random process in the applications of electronics and communication engineering sciences.

Modules	**Revised Bloom's Taxonomy (RBT) Level**
Module -1	
Linear Algebra-I Introduction to vector spaces and sub-spaces, definitions, illustrative examples and simple problems. Linearly independent and dependent vectors-definition and problems. Basis vectors, dimension of a vector space. Linear transformations- definition, properties and problems. Rank-Nullity theorem(without proof). Matrix form of linear transformations-Illustrative examples.**(Text 1 & Ref. 1)**	**L1,L2**
Module -2	
Linear Algebra-II Computation of Eigen values and Eigen vectors of real symmetric matrices-Given's method. Orthogonal vectors and orthogonal bases. Gram-Schmidt orthogonalization process. QR decomposition, singular value decomposition, least square approximations.**(Text 1 & Ref. 1)**	**L1,L2**
Module -3	
Calculus of Variations Concept of functional-Eulers equation. functional dependent on first and higher order derivatives, functional on several dependent variables. Isoperimetric problems-variation problems with moving boundaries.**(Text 2 & Ref. 2)**	**L1,L2**
Module -4	

Probability Theory Review of basic probability theory. Definitions of random variables and probability distributions, probability mass and density functions, expectation, moments, central moments, characteristic functions, probability generating and moment generating functions-illustrations. Binomial, Poisson, Exponential, Gaussian and Rayleigh distributions-examples.**(Text 3 & Ref. 3)**	**L1,L2**
Module -5	
Joint probability distributions Definition and properties of CDF, PDF, PMF, conditional distributions. Expectation, covariance and correlation. Independent random variables. Statement of central limit theorem-Illustrative examples. Random process- Classification, stationary and ergodic random process. Auto correlation function-properties, Gaussian random process.**(Text 3 & Ref. 3)**	**L1,L2**

Course Outcomes: After studying this course, students will be able to:

- Understand vector spaces, basis, linear transformations and the process of obtaining matrix of linear transformations arising in magnification and rotation of images.
- Apply the techniques of QR and singular value decomposition for data compression, least square approximation in solving inconsistent linear systems.
- Utilize the concepts of functionals and their variations in the applications of communication systems, decision theory, synthesis and optimization of digital circuits.
- Learn the idea of random variables (discrete/continuous) and probability distributions in analyzing the probability models arising in control systems and system communications.
- Apply the idea of joint probability distributions and the role of parameter-dependent random variables in random process.

Question paper pattern:

- The question paper will have 10 full questions carrying equal marks.
- Each full question consists of 16 marks with a maximum of four sub questions.
- There will be 2 full questions from each module covering all the topics of the module
- The students will have to answer 5 full questions, selecting one full question from each module.

Text Books:

1. David C.Lay, Steven R.Lay and J.J.McDonald: Linear Algebra and its Applications, 5th Edition, Pearson Education Ltd., 2015.
2. E. Kreyszig, "Advanced Engineering Mathematics", 10th edition, Wiley, 2015.
3. Scott L.Miller, Donald G. Childers: "Probability and Random Process with application to Signal Processing", Elsevier Academic Press, 2nd Edition,2013.

Reference books:

1. Richard Bronson: "Schaum's Outlines of Theory and Problems of Matrix Operations", McGraw-Hill, 1988.
2. Elsgolts, L.: "Differential Equations and Calculus of Variations", MIR Publications, 3rd Edition, 1977.
3. T.Veerarajan: "Probability, Statistics and Random Process", 3rd Edition, Tata McGraw Hill Co.,2008.

Web links:

1. http://nptel.ac.in/courses.php?disciplineId=111
2. http://www.class-central.com/subject/math(MOOCs)
3. http://ocw.mit.edu/courses/mathematics/
4. www.wolfram.com

DIGITAL VLSI DESIGN

[As per Choice Based Credit System (CBCS) scheme]

SEMESTER –I

Subject Code	16EVE12	IA Marks	20
Number	04	Exam Marks	80
Total Number of	50 (10 Hours per Module)	Exam Hours	03

CREDITS – 04

Course objectives: This course will enable students to:

- Explain VLSI Design Methodologies
- Learn Static and Dynamic operation principles, analysis and design of inverter circuit.
- Infer state of the art Semiconductors Memory circuits.
- Outline the comprehensive coverage of Methodologies and Design practice that are used to reduce the Power Dissipation of large scale digital circuits.
- Illustrate VLSI and ASIC design.

Modules	**Revised Bloom's Taxonomy (RBT) Level**
Module -1	
MOS Transistor: The Metal Oxide Semiconductor (MOS) Structure, The MOS System under External Bias, Structure and Operation of MOS Transistor, MOSFET Current-Voltage Characteristics, MOSFET Scaling and Small-Geometry Effects. **MOS Inverters-Static Characteristics**: Introduction, Resistive-Load Inverter, Inverters with n_Type MOSFET Load.	**L1, L2**
Module -2	
MOS Inverters-Static Characteristics: CMOS Inverter. **MOS Inverters**: Switching Characteristics and Interconnect Effects: Introduction, Delay-Time Definition, Calculation of Delay Times, Inverter Design with Delay Constraints, Estimation of Interconnect Parasitics, Calculation of Interconnect Delay, Switching Power Dissipation of CMOS Inverters.	**L2, L3**
Module -3	

Semiconductor Memories: Introduction, Dynamic Random Access Memory (DRAM), Static Random Access Memory (SRAM), Nonvolatile Memory, Flash Memory, Ferroelectric Random Access Memory (FRAM).	**L1, L2, L3**
Module -4	
Dynamic Logic Circuits: Introduction, Basic Principles of Pass Transistor Circuits, Voltage Bootstrapping, Synchronous Dynamic Circuit Techniques, Dynamic CMOS Circuit Techniques, High Performance Dynamic CMOS Circuits. **BiCMOS Logic Circuits**: Introduction, Bipolar Junction Transistor (BJT): Structure and Operation, Dynamic Behavior of BJTs, Basic BiCMOS Circuits: Static Behavior, Switching Delay in BiCMOS Logic Circuits, BiCMOS Applications.	**L1,L2, L3**
Module -5	
Chip Input and Output (I/O) Circuits: Introduction, ESD Protection, Input Circuits, Output Circuits and L(di/dt) Noise, On-Chip Clock Generation and Distribution, Latch-Up and Its Prevention. **Design for Manufacturability**: Introduction, Process Variations, Basic Concepts and Definitions, Design of Experiments and Performance Modeling.	**L2, L3**

Course outcomes:

After studying this course, students will be able to:

1. Analyse issues of On-chip interconnect Modelling and Interconnect delay calculation.
2. Analyse the Switching Characteristics in Digital Integrated Circuits.
3. Use the Dynamic Logic circuits in state-of-the-art VLSI chips.
4. Study critical issues such as ESD protection, Clock distribution, Clock buffering, and Latch phenomenon
5. Use Bipolar and Bi-CMOS circuits in very high speed design.

Question Paper Pattern

- The question paper will have 10 full questions carrying equal marks.
- Each full question consists of 16 marks with a maximum of four sub questions.
- There will be 2 full questions from each module covering all the topics of the module
- The students will have to answer 5 full questions, selecting one full question from each module.

Text Book:

Sung Mo Kang & Yosuf Leblebici, “CMOS Digital Integrated Circuits: Analysis and Design”, Tata McGraw-Hill, Third Edition.

Reference Books:

1. Neil Weste and K. Eshragian, “Principles of CMOS VLSI Design: A System Perspective”, Second Edition, Pearson Education (Asia) Pvt. Ltd. 2000.
2. Wayne, Wolf, “Modern VLSI Design: System on Silicon” Prentice Hall PTR/Pearson Education, Second Edition, 1998.
3. Douglas A Pucknell & Kamran Eshragian, “Basic VLSI Design” PHI 3rd Edition (original Edition – 1994).

ADVANCED EMBEDDED SYSTEM [As per Choice Based Credit System (CBCS) scheme] SEMESTER – I			
Subject Code	16EVE13	IA Marks	20
Number of Lecture Hours/Week	04	Exam Marks	80
Total Number of Lecture Hours	50 (10 Hours per Module)	Exam Hours	03
CREDITS – 04			

Course objectives: This course will enable students to:

- Understand the basic hardware components and their selection method based on the characteristics and attributes of an embedded system.
- Describe the hardware software co-design and firmware design approaches
- Explain the architectural features of ARM CORTEX M3, a 32 bit microcontroller including memory map, interrupts and exceptions.
- Program ARM CORTEX M3 using the various instructions, for different applications.

Modules	**Revised Bloom's Taxonomy (RBT) Level**
Module -1	
Embedded System: Embedded vs General computing system, classification, application and purpose of ES. Core of an Embedded System, Memory, Sensors, Actuators, LED, Opto coupler, Communication Interface, Reset circuits, RTC, WDT, Characteristics and Quality Attributes of Embedded Systems (Text 1: Selected Topics from Ch -1, 2, 3).	**L1, L2, L3**
Module -2	
Hardware Software Co-Design, embedded firmware design approaches, computational models, embedded firmware development languages, Integration and testing of Embedded Hardware and firmware, Components in embedded system development environment (IDE), Files generated during compilation, simulators, emulators and debugging (Text 1: Selected Topics From Ch-7, 9, 12, 13).	**L1, L2, L3**

Module -3	
ARM-32 bit Microcontroller: Thumb-2 technology and applications of ARM, Architecture of ARM Cortex M3, Various Units in the architecture, General Purpose Registers, Special Registers, exceptions, interrupts, stack operation, reset sequence (Text 2: Ch 1, 2, 3)	**L1, L2, L3**
Module -4	
Instruction Sets: Assembly basics, Instruction list and description, useful instructions, Memory Systems, Memory maps, Cortex M3 implementation overview, pipeline and bus interface (Text 2: Ch-4, 5, 6)	**L1, L2, L3**
Module -5	
Exceptions, Nested Vector interrupt controller design, Systick Timer, Cortex-M3 Programming using assembly and C language, CMSIS (Text 2: Ch-7, 8, 10)	**L1, L2, L3**

Course Outcomes: After studying this course, students will be able to:

- Understand the basic hardware components and their selection method based on the characteristics and attributes of an embedded system.
- Explain the hardware software co-design and firmware design approaches.
- Acquire the knowledge of the architectural features of ARM CORTEX M3, a 32 bit microcontroller including memory map, interrupts and exceptions.
- Apply the knowledge gained for Programming ARM CORTEX M3 for different applications.

Question paper pattern:

- The question paper will have 10 full questions carrying equal marks.
- Each full question consists of 16 marks with a maximum of four sub questions.
- There will be 2 full questions from each module covering all the topics of the module
- The students will have to answer 5 full questions, selecting one full question from each module.

Text Books:

1. K. V. Shibu, "Introduction to embedded systems", TMH education Pvt. Ltd. 2009.
2. Joseph Yiu, “The Definitive Guide to the ARM Cortex-M3”, 2nd edn, Newnes, (Elsevier), 2010.

Reference Book:

James K. Peckol, "Embedded systems- A contemporary design tool", John Wiley, 2008.

LOW POWER VLSI DESIGN [As per Choice Based Credit System (CBCS) scheme] SEMESTER –I			
Subject Code	16EVE14	IA Marks	20
Number of Lecture	04	Exam Marks	80
Total Number of Lecture Hours	50 (10 Hours per Module)	Exam Hours	03
CREDITS – 04			

Course objectives: This course will enable students to:

- Know the basics and advanced techniques in low power design which is a hot topic in today's market where the power plays a major role.
- Describe the various power reduction and the power estimation methods.
- Explain power dissipation at all layers of design hierarchy from technology, circuit, logic, architecture and system
- Apply State-of-the art approaches to power estimation and reduction.
- Practice the low power techniques using current generation design style and process technology

Modules	**Revised Bloom's Taxonom**
Module -1	
Introduction: Need for low power VLSI chips, charging and discharging capacitance, short circuit current in CMOS leakage current, static current, basic principles of low power design, low power figure of merits. **Simulation power analysis**: SPICE circuit simulation, discrete transistor modeling and analysis, gate level logic simulation, architecture level analysis, data correlation analysis in DSP systems, Monte Carlo simulation. (Text 1)	**L1, L2**
Module -2	
Probabilistic power analysis: Random logic signals, probability & frequency, probabilistic power analysis techniques, signal entropy. **Circuit**: Transistor and gate sizing, equivalent pin ordering, network restructuring and reorganization, special latches and flip flops, low power digital cell library, adjustable device threshold voltage. (Text 1)	**L1, L2, L3**
Module -3	
Logic: Gate reorganization, signal gating, logic encoding, state machine encoding, pre-computation logic (Text 1). **Low power Clock Distribution:** Power dissipation in clock distribution, single driver Vs distributed buffers, Zero skew Vs tolerable skew, chip & package co design of clock network (Text 2).	**L1, L2, L3**
Module -4	

Low power Architecture & Systems: Power & performance management, switching activity reduction, parallel architecture with voltage reduction, flow graph transformation (Text 1). **Low power arithmetic components:** Introduction, circuit design style, adders, multipliers, division (Text 2).	**L1- L4**
Module -5	
Low power memory design: Introduction, sources and reductions of power dissipation in memory subsystem, sources of power dissipation in DRAM and SRAM (Text 2). **Algorithm & Architectural Level Methodologies:** Introduction, design flow, Algorithmic level analysis & optimization, Architectural level estimation & synthesis (Text 2). **Advanced Techniques:** Adiabatic computation, pass transistor, Asynchronous circuits (Text 1).	**L1-L4**

Course outcomes: After studying this course, students will be able to:

- Identify the sources of power dissipation in CMOS circuits.
- Perform power analysis using simulation based approaches and probabilistic analysis.
- Use optimization and trade-off techniques that involve power dissipation of digital circuits.
- Make the power design a reality by making power dimension an integral part of the design process
- Use practical low power design techniques and their analysis at various levels of design abstraction and analyse how these are being captured in the latest design automation environments.

Question paper pattern:

- The question paper will have 10 full questions carrying equal marks.
- Each full question consists of 16 marks with a maximum of four sub questions.
- There will be 2 full questions from each module covering all the topics of the module
- The students will have to answer 5 full questions, selecting one full question from each module.

Text Books:

1. Gary K. Yeap, "Practical Low Power Digital VLSI Design", Kluwer Academic, 1998.
2. Jan M.Rabaey, Massoud Pedram, "Low Power Design Methodologies", Kluwer Academic, 2010.

Reference Books:

1. Kaushik Roy, Sharat Prasad, "Low-Power CMOS VLSI Circuit Design" Wiley, 2000
2. A.P.Chandrasekaran and R.W.Broadersen, "Low power digital CMOS design", Kluwer Academic,1995.
3. A Bellamour and M I Elmasri, " Low power VLSI CMOS circuit design", Kluwer Academic,1995.

DIGITAL SYSTEM DESIGN USING VERILOG

[As per Choice Based Credit System (CBCS) scheme]

SEMESTER – I

Subject Code	16EVE151	IA Marks	20
Number of Lecture Hours/Week	03	Exam Marks	80
Total Number of Lecture Hours	40 (08 Hours per Module)	Exam Hours	03

CREDITS – 03

Course objectives: This course will enable students to:

- Understand the concepts of Verilog Language
- Design the digital systems as an activity in a larger systems design context.
- Study the design and operation of semiconductor memories frequently used in application specific digital system.
- Inspect how effectively IC's are embedded in package and assembled in PCB's for different application
- Design and diagnosis of processors and I/O controllers they can be used in embedded systems

Modules	**Revised Bloom's Taxonomy (RBT) level**
Module -1	
Introduction and Methodology: Digital Systems and Embedded Systems, Binary representation and Circuit Elements, Real-World Circuits, Models, Design Methodology.	**L1, L2**
Module -2	
Number Basics: Unsigned and Signed Integers, Fixed and Floating-point Numbers. **Sequential Basics**: Storage elements, Counters, Sequential Data paths and Control, Clocked Synchronous Timing Methodology.	**L1, L2**
Module -3	
Memories: Concepts, Memory Types, Error Detection and Correction. **Implementation Fabrics**: ICs, PLDs, Packaging and Circuit Boards, Interconnection and Signal Integrity.	**L1, L2**
Module -4	
Processor Basics: Embedded Computer Organization, Instruction and Data, Interfacing with memory. **I/O interfacing**: I/O devices, I/O controllers, Parallel Buses, Serial Transmission, I/O software.	**L2, L3**
Module -5	

Accelerators: Concepts, case study, Verification of accelerators. **Design Methodology**: Design flow, Design optimization, Design for test.	**L2, L3**

Course Outcomes: After studying this course, students will be able to:

- Design embedded systems, using small microcontrollers, larger CPUs/DSPs, or hard or soft processor cores.
- Design the combinational circuits using discrete gates and programmable logic devices.
- Describe Verilog model for sequential circuits and test pattern generation
- Explore the different types of semiconductor memories and their usage for specific chip design
- Synthesis different types of processor and I/O controllers that are used in embedded system design

Question paper pattern:

- The question paper will have 10 full questions carrying equal marks.
- Each full question consists of 16 marks with a maximum of four sub questions.
- There will be 2 full questions from each module covering all the topics of the module
- The students will have to answer 5 full questions, selecting one full question from each module.

Text Book:

Peter J. Ashenden, "Digital Design: An Embedded Systems Approach Using VERILOG", Elesvier, 2010.

Reference Book:

Verilog HDL: A Guide to Digital Design and Synthesis, Second Edition by Samir Palnitkar.

NANOELECTRONICS [As per Choice Based Credit System (CBCS) scheme]			
Subject Code	16EVE152	IA Marks	20
Number of Lecture Hours/Week	03	Exam Marks	80
Total Number of Lecture Hours	40 (08 Hours per Module)	Exam Hours	03
CREDITS – 03			

Course objectives: This course will enable students to:

- Enhance basic engineering science and technological knowledge of nanoelect ronics.
- Explain basics of top-down and bottom-up fabrication process, devices and systems.
- Describe technologies involved in modern day electronic devices.
- Appreciate the complexities in scaling down the electronic devices in the future.

Modules	**Revised Bloom's Taxonomy (RBT) Level**
Module -1	
Introduction: Overview of nanoscience and engineering. Development milestones in microfabrication and electronic industry. Moores' law and continued miniaturization, Classification of Nanostructures, Electronic properties of atoms and solids: Isolated atom, Bonding between atoms, Giant molecular solids, Free electron models and energy bands, crystalline solids, Periodicity of crystal lattices, Electronic conduction, effects of nanometer length scale, Fabrication methods: Top down processes, Bottom up processes methods for templating the growth of nanomaterials, ordering of nanosystems (Text 1).	**L1, L2**
Module -2	
Characterization: Classification, Microscopic techniques, Field ion microscopy, scanning probe techniques, diffraction techniques: bulk and surface diffraction techniques (Text1).	**L1,L2,L3**
Module -3	

Characterization: spectroscopy techniques: photon, radiofrequency, electron, surface analysis and dept profiling: electron, mass, Ion beam, Reflectrometry, Techniques for property measurement: mechanical, electron, magnetic, thermal properties. **Inorganic semiconductor nanostructures:** overview of semiconductor physics. Quantum confinement in semiconductor nanostructures: quantum wells, quantum wires, quantum dots, super-lattices, band offsets, electronic density of states (Text1).	**L1-L3**
Module -4	
Fabrication techniques: requirements of ideal semiconductor, epitaxial growth of quantum wells, lithography and etching, cleaved-edge over growth, growth of vicinal substrates, strain induced dots and wires, electrostatically induced dots and wires, Quantum well width fluctuations, thermally annealed quantum wells, semiconductor nanocrystals, collidal quantum dots, self-assembly techniques. **Physical processes:** modulation doping, quantum hall effect, resonant tunneling, charging effects, ballistic carrier transport, Inter band absorption, intra band absorption, Light emission processes, phonon bottleneck, quantum confined stark effect, nonlinear effects, coherence and dephasing, characterization of semiconductor nanostructures: optical electrical and structural (Text1).	**L1-L3**
Module -5	
Methods of measuring properties: atomic, crystollography, microscopy, spectroscopy (Text 2). **Applications**: Injection lasers, quantum cascade lasers, single-photon sources, biological tagging, optical memories, coulomb blockade devices, photonic structures, QWIP's, NEMS, MEMS (Text 1).	**L1-L3**

Course outcomes: After studying this course, students will be able to:

- Know the principles behind Nanoscience engineering and Nanoelectronics.
- Apply the knowledge to prepare and characterize nanomaterials.
- Know the effect of particles size on mechanical, thermal, optical and electrical properties of nanomaterials.
- Design the process flow required to fabricate state of the art transistor technol ogy.
- Analyze the requirements for new materials and device structure in the future technologies.

Question paper pattern:

- The question paper will have 10 full questions carrying equal marks.
- Each full question consists of 16 marks with a maximum of four sub questions.
- There will be 2 full questions from each module covering all the topics of the module
- The students will have to answer 5 full questions, selecting one full question from each module.

Text Books:

1. Ed Robert Kelsall, Ian Hamley, Mark Geoghegan, “Nanoscale Science and Technology”, John Wiley, 2007.
2. Charles P Poole, Jr, Frank J Owens, “Introduction to Nanotechnology”, John Wiley, Copyright 2006, Reprint 2011.

Reference Book:

Ed William A Goddard III, Donald W Brenner, Sergey E. Lyshevski, Gerald J Iafrate, “Hand Book of Nanoscience Engineering and Technology”, CRC press, 2003.

ASIC DESIGN

[As per Choice Based Credit System (CBCS) scheme]

SEMESTER – I

Subject Code	16EVE153	IA Marks	20
Number of Lecture Hours/Week	03	Exam Marks	80
Total Number of Lecture Hours	40	Exam Hours	03

CREDITS – 03

Course objectives: This course will enable students to:

- Explain ASIC methodologies and programmable logic cells to implement a function on IC.
- Analyse back-end physical design flow, including partitioning, floor-planning, placement, and routing.
- Gain sufficient theoretical knowledge for carrying out FPGA and ASIC designs.
- Design CAD algorithms and explain how these concepts interact in ASIC design.

Modules	**Revised Bloom's Taxonomy (RBT)Level**
Module -1	
Introduction to ASICs, Full custom, Semi-custom and Programmable ASICs, ASIC Design flow, ASIC cell libraries. **CMOS Logic:** Datapath Logic Cells**:** Data Path Elements, Adders: Carry skip, Carry bypass, Carry save, Carry select, Conditional sum, Multiplier (Booth encoding), Data path Operators, I/O cells.	**L1,L2**
Module -2	
ASIC Library Design: Logical effort: Predicting Delay, Logical area and logical efficiency, Logical paths, Multi stage cells, Optimum delay and number of stages. **Programmable ASIC Logic Cells:** MUX as Boolean function generators, Actel ACT: ACT 1, ACT 2 and ACT 3 Logic Modules, Xilinx LCA: XC3000 CLB, Altera FLEX and MAX.	**L1-L3**
Module -3	
Programmable ASIC I/O Cells: Xilinx and Altera I/O Block. **Low-level design entry:** Schematic entry: Hierarchical design, Netlist screener. **ASIC Construction:** Physical Design, CAD Tools. **Partitioning:** Goals and objectives, Constructive Partitioning, Iterative Partitioning Improvement, KL, FM and Look Ahead algorithms.	**L1-L4**
Module -4	
Floor planning and placement: Goals and objectives, Floor planning tools, Channel definition, I/O and Power planning and Clock planning. Placement**:** Goals and Objectives, Min-cut Placement algorithm, Iterative Placement Improvement, Physical Design Flow.	**L1-L3**

Module -5

Routing: Global Routing: Goals and objectives, Global Routing Methods, Back-annotation. Detailed Routing: Goals and objectives, Measurement of Channel Density, Left-Edge and Area-Routing Algorithms. Special Routing, Circuit extraction and DRC.	**L1-L3**

Course outcomes:

After studying this course, students will be able to:

- Describe the concepts of ASIC design methodology, data path elements, logical effort and FPGA architectures.
- Analyze the design of FPGAs and ASICs suitable for specific tasks, perform design entry and explain the physical design flow.
- Design data path elements for ASIC cell libraries and compute optimum path delay.
- Create floor plan including partition and routing with the use of CAD algorithms.

Question paper pattern:

- The question paper will have 10 full questions carrying equal marks.
- Each full question consists of 16 marks with a maximum of four sub questions.
- There will be 2 full questions from each module covering all the topics of the module
- The students will have to answer 5 full questions, selecting one full question from each module.

Text Book:

Michael John Sebastian Smith, "Application - Specific Integrated Circuits" Addison-Wesley Professional; 2005.

Reference Books:

1. Neil H.E. Weste, David Harris, and Ayan Banerjee, "CMOS VLSI Design: A Circuits and Systems Perspective", 3rd edition, Addison Wesley/ Pearson education, 2011.
2. Vikram Arkalgud Chandrasetty, "VLSI Design: A Practical Guide for FPGA and ASIC Implementations", Springer, 2011, ISBN: 978-1-4614-1119-2.
3. Rakesh Chadha**,** Bhasker J., "An ASIC Low Power Primer", Springer, ISBN: 978-1-4614-4270-7.

ADVANCED COMPUTER ARCHITECTURE

[As per Choice Based Credit System (CBCS) scheme]

SEMESTER – I

Subject Code	16ELD154	IA Marks	20
Number of Lecture Hours/Week	03	Exam Marks	80
Total Number of Lecture Hours	40	Exam Hours	03

CREDITS – 03

Course objectives: This course will enable students to:

- Understand the basic concepts for parallel processing
- Analyze program partitioning and flow mechanisms
- Apply pipelining concept for the performance evaluation
- Learn the advanced processor architectures for suitable applications

Modules	**Revised Bloom's Taxonomy (RBT) Level**
Module -1	
Parallel Computer Models: Classification of parallel computers, Multiprocessors and multicomputers, Multivector and SIMD computers. Program and Network Properties, Conditions of parallelism, Data and resource Dependences, Hardware and software parallelism. **(Text 1)**	**L2, L3, L4**
Module -2	
Program partitioning and scheduling, Grain Size and latency, Program flow mechanisms, Control flow versus data flow, Data flow Architecture, Demand driven mechanisms, Comparisons of flow mechanisms, Principles of Scalable Performance, Performance Metrics and Measures, Parallel Processing Applications, Speedup Performance Laws, Scalability Analysis and Approaches. **(Text 1)**	**L2, L3, L4**
Module -3	
Advanced Processors: Advanced processor technology, Instruction-set Architectures, CISC Scalar Processors, RISC Scalar Processors, Superscalar Processors, VLIW Architectures, Pipelining, Linear pipeline processor, nonlinear pipeline processor, Instruction pipeline design. **(Text 1)**	**L1, L2, L3**
Module -4	
Mechanisms for instruction pipelining, Dynamic instruction scheduling, Branch Handling techniques, branch prediction, Arithmetic Pipeline Design, Computer arithmetic principles, Static Arithmetic pipeline, Multifunctional arithmetic pipelines. **(Text 1)**	**L2, L3, L4**
Module -5	

Multithread and Dataflow Architecture: Principles of Multithreading, Scalable and Multithreaded Architecture, Dataflow Architecture, Symmetric shared memory architecture, distributed shared memory architecture. **(Text 1 & 2)**	**L1, L2, L3**

Course outcomes: At the end of this course, the students will be able to:

- Understand the basic concepts for parallel processing
- Analyze program partitioning and flow mechanisms
- Apply pipelining concept for the performance evaluation
- Learn the advanced processor architectures for suitable applications

Question paper pattern:

- The question paper will have 10 full questions carrying equal marks.
- Each full question consists of 16 marks with a maximum of four sub questions.
- There will be 2 full questions from each module covering all the topics of the module
- The students will have to answer 5 full questions, selecting one full question from each module.

Text Books:

1. Kai Hwang, "Advanced computer architecture", TMH. 2007.
2. Kai Hwang and Zu, "Scalable Parallel Computers Architecture", MGH, 2008.

Reference Books:

1. M.J. Flynn, "Computer Architecture, Pipelined and Parallel Processor Design", Narosa Publishing, 2002.
2. D.A.Patterson, J.L.Hennessy, "Computer Architecture: A quantitative approach", Morgan Kauffmann feb,2002.

VLSI and ES LAB - 1

[As per Choice Based Credit System (CBCS) scheme]

SEMESTER – I

Laboratory Code	16EVEL16	IA Marks	20
Number of Lecture Hours/Week	01Hr Tutorial (Instructions) + 02 Hours Laboratory	Exam Marks	80
		Exam Hours	03

CREDITS – 02

Course objectives: This course will enable students to:

- Learn Verilog Code Programming for the design of digital circuits
- Use FPGA/CPLD board and Logic Analyzer or Chipscope to verify the results
- Learn Assembly language programming for different applications using ARM-Cortex M3 Kit and Keil uVision- 4 tool.
- Learn C language programming for different applications using ARM- Cortex M3 Kit and Keil uVision-4 tool.

Laboratory Experiments:	**Revised Bloom's Taxonomy**
1) **Digital Design Experiments**: Using Verilog code and any Compiler. Download code to FPGA/CPLD board and verify the output using Logic Analyzer or Chipscope a) Design and verify an 8 to 3 programmable priority encoder b) Design and verify 3-bit Arbitrary Counter and repeat the given sequence c) Design and Verify BCD adder and subtractor d) Design and verify a sequential block to generate a sequence (say 11101) using appropriate FSM. e) Design and verify 8 bit Ripple carry adder and Carry skip adder. f) Design and verify a Linear feedback shift register based on a given polynomial expression g) Design and verify the following 8 bit multipliers. Also report on area delay trade-off i) Serial Multiplier ii) Parallel Multiplier h) Design and verify a parameterized FIFO i) Design and verify register file which has 32-entry 3-ports having explicit address decoder. The ports are dedicated for read and write and will take one clock cycle for read or write operation	**L2,L3,L4**

2) **ARM Cortex M3 Programs**: (Programming to be done using Keil uVision 4 and download the program on to a M3 evaluation board such as NXP LPC1768 or ATMEL ATSAM3U) a) Write an Assembly language program to calculate the sum and display the result for the addition of first ten numbers. SUM = 10+9+8+.....+1 b) Write a Assembly language program to link multiple object files and link them together c) Write an Assembly language program to store data in RAM d) Write a C program to Output the "Hello World" message using UART e) Write a C program to Design a Stopwatch using interrupts	**L2,L3,L4**

Course outcomes: On the completion of this laboratory course, the students will be able to:

- Develop Verilog Code for the design of digital circuits
- Use FPGA/CPLD board and Logic Analyzer or Chipscope to verify the results
- Develop Assembly language programs for different applications using ARM-Cortex M3 Kit and Keil uVision-4 tool.
- Develop C language programs for different applications using ARM-Cortex M3 Kit and Keil uVision-4 tool

Conduct of Practical Examination:

- All laboratory experiments are to be included for practical examination.
- For examination, two questions using different tool to be set.
- Students are allowed to pick one experiment from the lot.
- Strictly follow the instructions as printed on the cover page of answer script for breakup of marks.
- Change of experiment is allowed only once and Marks allotted to the procedure part to be made zero.

M.Tech-VLSI & ES-2016-SECOND SEMESTER SYLLABUS

Design of Analog and Mixed Mode VLSI Circuits [As per Choice Based credit System (CBCS) Scheme SEMESTER – II			
Subject Code	16EVE21	IA Marks	20
Number of Lecture Hours/Week	04	Exam marks	80
Total Number of Lecture Hours	50 (10 Hours per Module)	Exam Hours	03
CREDITS – 04			

Course Objectives: This course will enable students to:

- Describe basic physics and operation of MOS devices.
- Exemplify single-stage and differential amplifiers and current mirrors
- Describe operational amplifiers
- Learn the design of phase-locked-loops
- Know the role of Data converters in an ever-increasing digital world.

Modules	**RBT Level**
Module 1	
Basic MOS Device Physics: General considerations, MOS I/V Characteristics, second order effects, MOS device models. **Single stage Amplifier:** Basic Concepts, Common Source stage.(Text 1)	L1, L2
Module 2	
Single stage Amplifier: Source follower, common-gate stage, Cascode Stage, choice of device models. **Differential Amplifiers:** Single ended and differential operation, Basic differential pair, Common mode response, Differential pair with MOS loads, Gilbert cell. (Text 1)	L1,L2
Module 3	
Passive and Active Current Mirrors: Basic current mirrors, Cascode Current mirrors, Active Current mirrors. **Operational Amplifiers (part-1):** General Considerations**,** One Stage OP-Amp, Two Stage OP-Amp, Gain boosting. (Text 1)	L1,L2,L3
Module 4	
Operational Amplifiers (part-2): Common Mode Feedback, Slew rate, Power Supply Rejection. **Phase Locked Loops:** Simple PLL, Charge pump PLLs, Non-ideal effects in PLLs, Delay-Locked Loops, Applications. (Text 1)	L1,L2,L3
Module 5	
Data Converter Architectures: DAC & ADC Specifications, Current Steering DAC, Charge Scaling DAC, Cyclic DAC, Pipeline DAC, Flash ADC, Pipeline ADC, Integrating ADC, Successive Approximation ADC. (Text 2)	L1,L2,L3

Course Outcomes: After studying this course, students will be able to:

- Use efficient analytical tools for quantifying the behaviour of basic circuits by inspection.
- Design high-performance, stable operational amplifiers with the trade-offs between speed, precision and power dissipation.
- Design and study the behaviour of phase-locked-loops for the applications.
- Identify the critical parameters that affect the analog and mixed-signal VLSI circuits' performance
- Perform calculations in the digital or discrete time domain, more sophisticated data converters to translate the digital data to and from inherently analog world.

Question paper pattern:

- The question paper will have 10 full questions carrying equal marks.
- Each full question consists of 16 marks with a maximum of four sub questions.
- There will be 2 full questions from each module covering all the topics of the module
- The students will have to answer 5 full questions, selecting one full question from each module.

Text Books:

1. Behzad Razavi, "Design of Analog CMOS Integrated Circuits", TMH, 2007.
2. R. Jacob Baker, "CMOS Circuit Design, Layout, and Simulation", Second Edition, Wiley.

Reference Book:

Phillip E. Allen, Douglas R. Holberg, "CMOS Analog Circuit Design", Second Edition, Oxford University Press.

VLSI Testing

[As per Choice Based credit System (CBCS) Scheme
SEMESTER – II

Subject Code	16EVE22	IA Marks	20
Number of Lecture Hours/Week	04	Exam marks	80
Total Number of Lecture Hours	50 (10 Hours per Module)	Exam Hours	03

CREDITS – 04

Course Objectives: This course will enable students to:

- Learn various types of faults and fault modeling
- Comprehend the need for testing and testable design of digital circuits
- Illustrate methods and algorithms for testing digital combinatorial networks and test pattern generation
- Exemplify methods for testing sequential circuits and memory testing
- Inferring testing methods using Boundary scan, Built-in self test and other advanced topics in digital circuit design.

Modules	**RBT Level**
Module 1	
Faults in digital circuits: Failures and Faults, Modeling of faults, Temporary Faults. (Text 1) **Logic Simulation:** Applications, Problems in simulation based design verification, types of simulation, The unknown logic values, compiled simulation, event-driven simulation, Delay models, Element evaluation, Hazard detection, Gate-level event-driven Simulation. (Text 2)	L1,L2
Module 2	
Test generation for Combinational Logic circuits: Fault Diagnosis of digital circuits, Test generation techniques for combinational circuits, Detection of multiple faults in Combinational logic circuits. (Text 1) **Testable Combinational logic circuit design:** The Read-Muller expansion technique, Three level OR-AND-OR design, Automatic synthesis of testable logic.(Text 1)	L1,L2,L3
Module 3	
Testable Combinational logic circuit design: Testable design of multilevel combinational circuits, Synthesis of random pattern testable combinational circuits, Path delay fault testable combinational logic design, Testable PLA design. (Text 1) **Test generation for Sequential circuits:** Testing of sequential circuits as Iterative combinational circuits, state table verification, Test generation based on Circuit Structure, Functional Fault models, test Generation based on Functional Fault models. (Text 1)	L1,L2,L3
Module 4	
Design of testable sequential circuits: Controllability and observability, Ad-Hoc design rules for improving testability, design of	L1,L2,L3

diagnosable sequential circuits, the scan-path technique for testable sequential circuit design, Level Sensitive Scan Design(LSSD), Random Access Scan Technique, Partial scan, testable sequential circuit design using Nonscan Techniques, Cross check, Boundary Scan. (Text 1)	
Module 5	
Built-In Self Test: Test pattern generation for BIST, Output response analysis, Circular BIST, BIST Architectures. (Text 1) **Testable Memory Design:** RAM Fault Models, Test algorithms for RAMs, Detection of pattern-sensitive faults, BIST techniques for RAM chips, Test generation and BIST for embedded RAMs. (Text1)	L1,L2,L3

Course Outcomes: After studying this course, students will be able to:

- Analyze the need for fault modeling and testing of digital circuits
- Generate fault lists for digital circuits and compress the tests for efficiency
- Create tests for digital memories and analyze failures in them
- Apply boundary scan technique to validate the performance of digital circuits
- Design built-in self tests for complex digital circuits

Question paper pattern:

- The question paper will have 10 questions carrying equal marks.
- Each full question consists of 16 marks with a maximum of four sub questions.
- There will be 2 full questions from each module covering all the topics of the module
- The students will have to answer 5 full questions, selecting one full question from each module.

Text Books:

1. Lala Parag K., Digital Circuit Testing and Testability, New York, Academic Press, 1997.
2. Abramovici M, Breuer M A and Friedman A D, “Digital Systems Testing and Testable Design”, Wiley, 1994.

Reference Books:

1. Vishwani D Agarwal, “Essential of Electronic Testing for Digital, Memory and Mixed Signal Circuits”, Springer, 2002.
2. Wang, Wu and Wen, “VLSI Test Principles and Architectures”, Morgan Kaufmann, 2006.

Advances in VLSI Design

[As per Choice Based credit System (CBCS) Scheme

SEMESTER – II

Subject Code	16EVE23	IA Marks	20
Number of Lecture Hours/Week	04	Exam marks	80
Total Number of Lecture Hours	50 (10 Hours per Module)	Exam Hours	03

CREDITS – 04

Course Objectives: This course will enable the students to:

- Learn circuit-oriented approach towards digital design
- Illustrate the impact of interconnect wiring on the functionality and performance of a digital gate.
- Infer different approaches to digital timing and clocking circuits
- Understand the impact of clock skew on the behaviour of digital synchronous circuits
- Explain the role of peripheral circuitry such as the decoders, sense amplifiers, drivers and control circuitry in the design of reliable and fast memories

Modules	**RBT Level**
Module 1	
Implementation Strategies For Digital ICS: Introduction, From Custom to Semicustom and Structured Array Design Approaches, Custom Circuit Design, Cell-Based Design Methodology, Standard Cell, Compiled Cells, Macrocells, Megacells and Intellectual Property, Semi-Custom Design Flow, Array-Based Implementation Approaches, Pre-diffused (or Mask-Programmable) Arrays, Pre-wired Arrays, Perspective-The Implementation Platform of the Future.	L1,L2,L3
Module 2	
Coping With Interconnect: Introduction, Capacitive Parasitics, Capacitance and Reliability-Cross Talk, Capacitance and Performance in CMOS, Resistive Parasitics, Resistance and Reliability-Ohmic Voltage Drop, Electromigration, Resistance and Performance-RC Delay, Inductive Parasitics, Inductance and Reliability-Voltage Drop, Inductance and Performance-Transmission Line Effects, Advanced Interconnect Techniques, Reduced-Swing Circuits, Current-Mode Transmission Techniques, Perspective: Networks-on-a-Chip.	L1,L2,L3
Module 3	
Timing Issues In Digital Circuits: Introduction, Timing Classification of Digital Systems, Synchronous Interconnect, Mesochronous interconnect, Plesiochronous Interconnect, Asynchronous Interconnect, Synchronous Design — An In-depth Perspective, Synchronous Timing Basics, Sources of Skew and Jitter, Clock-Distribution Techniques, Latch-Based Clocking, Self-Timed Circuit Design, Self-Timed Logic - An Asynchronous	L1,L2,L3

Technique, Completion-Signal Generation, Self-Timed Signaling, Practical Examples of Self-Timed Logic, Synchronizers and Arbiters, Synchronizers-Concept and Implementation, Arbiters, Clock Synthesis and Synchronization Using a Phase-Locked Loop, Basic Concept, Building Blocks of a PLL.	
Module 4	
Designing Memory and Array Structures: Introduction, Memory Classification, Memory Architectures and Building Blocks, The Memory Core, Read-Only Memories, Nonvolatile Read-Write Memories, Read-Write Memories (RAM), Contents-Addressable or Associative Memory (CAM), Memory Peripheral Circuitry, The Address Decoders, Sense Amplifiers, Voltage References, Drivers/Buffers, Timing and Control.	L1,L2,L3
Module 5	
Designing Memory and Array Structures: Memory Reliability and Yield, Signal-to-Noise Ratio, Memory yield, Power Dissipation in Memories, Sources of Power Dissipation in Memories, Partitioning of the memory, Addressing the Active Power Dissipation, Data-retention dissipation, Case Studies in Memory Design: The Programmable Logic Array (PLA), A 4 Mbit SRAM, A 1 Gbit NAND Flash Memory, Perspective: Semiconductor Memory Trends and Evolutions.	L1,L2,L3

Course Outcomes: After studying this course, students will be able to:

- Apply design automation for complex circuits using the different implementation methodology like custom versus semi-custom, hardwired versus fixed, regular array versus ad-hoc.
- Use the approaches to minimize the impact of interconnect parasitics on performance, power dissipation and circuit reliability
- Impose the ordering of the switching events to meet the desired timing constraints using synchronous, clocked approach.
- Infer the reliability of the memory

Question paper pattern:

- The question paper will have 10 full questions carrying equal marks.
- Each full question consists of 16 marks with a maximum of four sub questions.
- There will be 2 full questions from each module covering all the topics of the module
- The students will have to answer 5 full questions, selecting one full question from each module.

Text Book:

Jan M Rabey, Anantha Chandrakasan, Borivoje Nikolic, “Digital Integrated Circuits-A Design Perspective”, PHI, 2nd Edition.

Reference Books:

1. M. Smith, “Application Specific Integrated circuits”, Addison Wesley, 1997
2. H. Veendrick, “MOS IC’s: From Basics to ASICs, Wiley-VCH, 1992.
3. Anantha P. Chandrakasan , Robert W. Brodersen, “Low Power Digital CMOS Design”, Kluwer Academic Publisher, 1995.

Real Time Operating System

[As per Choice Based credit System (CBCS) Scheme

SEMESTER – II

Subject Code	16EVE24	IA Marks	20
Number of Lecture Hours/Week	04	Exam marks	80
Total Number of Lecture Hours	50 (10 Hours per Module)	Exam Hours	03

CREDITS – 04

Course Objectives: This course will enable the students to:

- Introduce the fundamental concepts of Real Time Operating Systems and the real time embedded system
- Apply concepts relating to operating systems such as Scheduling techniques, Thread Safe Reentrant Functions, Dynamic priority policies.
- Describe concepts related to Multi resource services like blocking, Deadlock, live lock & soft real-time services.
- Discuss Memory management concepts, Embedded system components, Debugging components and file system components.
- Study programs for multithreaded applications using suitable data structures.

Modules	**RBT Level**
Module 1	
Real-Time Systems and Resources: Brief history of Real Time Systems, A brief history of Embedded Systems. System Resources, Resource Analysis, Real-Time Service Utility, Scheduler concepts, Real-Time OS, State transition diagram and tables, Thread Safe Reentrant Functions. (Text 1: Selected sections from Chap. 1, 2)	L1,L2,L3
Module 2	
Processing with Real Time Scheduling: Scheduler Concepts, Preemptive Fixed Priority Scheduling Policies with timing diagrams and problems and issues, Feasibility, Rate Monotonic least upper bound, Necessary and Sufficient feasibility, Deadline –Monotonic Policy, Dynamic priority policies, Alternative to RM policy. (Text 1: Chap. 2,3,7)	L1,L2,L3
Module 3	
Memory and I/O: Worst case execution time, Intermediate I/O, Shared Memory, ECC Memory, Flash file systems. Multi-resource Services, Blocking, Deadlock and live lock, Critical sections to protect shared resources, Missed deadline, QoS, Reliability and Availability, Similarities and differences, Reliable software, Available software. (Text 1: Selected topics from Chap. 4,5,6,7,11)	L1,L2,L3
Module 4	
Firmware Components: The 3 firmware components, RTOS system software mechanisms, Software application components. Debugging	L1,L2,L3

Components, Exceptions, assert, Checking return codes, Single-step debugging, kernel scheduler traces, Test access ports, Trace Ports, External test equipment. (Text 1: Selected topics from Chap. 8,9)	
Module 5	
Process and Threads: Process and thread creations, Simple Programs, Programs related to semaphores, message queue, shared buffer applications involving inter task/thread communication using multiple threads. (Text 2: Chap. 11)	L1,L2,L3

Course Outcomes: After studying this course, students will be able to:

- Develop programs for real time services, firmware and RTOS, using the fundamentals of Real Time Embedded System, real time service utilities, debugging methodologies and optimization techniques.
- Select the appropriate system resources (CPU, I/O, Memory, Cache, ECC Memory, Microcontroller/FPGA/ASIC to improve the system performance.
- Apply priority based static and dynamic real time scheduling techniques for the given specifications.
- Analyze deadlock conditions, shared memory problem, critical section problem, missed deadlines, availability, reliability and QoS.
- Develop programs for multithreaded applications using suitable techniques and data structure

Question paper pattern:

- The question paper will have 10 full questions carrying equal marks.
- Each full question consists of 16 marks with a maximum of four sub questions.
- There will be 2 full questions from each module covering all the topics of the module
- The students will have to answer 5 full questions, selecting one full question from each module.

Text Books:

1. Sam Siewert, "Real-Time Embedded Systems and Components", Cengage Learning India Edition, 2007.
2. Dr. K.V.K.K Prasad, Embedded/Real Time Systems, Concepts, Design and Programming, Black Book, Dream Tech Press, New edition, 2010.

Reference Books:

1. James W S Liu, "Real Time System", Pearson education, 2008.
2. Dream Tech Software Team, "Programming for Embedded Systems", John Wiley, India Pvt. Ltd., 2008.

System Verilog [As per Choice Based credit System (CBCS) Scheme SEMESTER – II			
Subject Code	16EVE251	IA Marks	20
Number of Lecture Hours/Week	03	Exam marks	80
Total Number of Lecture Hours	40 (8 Hours per Module)	Exam Hours	03
CREDITS – 03			

Course Objectives: This course will enable students to:

- Understand digital system verification using object oriented methods
- Learn the System Verilog language for digital system verification.
- Create/build test benches for the basic design/methodology.
- Use constrained random tests for verification
- Understand concepts of functional coverage

Modules	**RBT Level**
Module 1	
Verification Guidelines: The verification process, basic test bench functionality, directed testing, methodology basics, constrained random stimulus, randomization, functional coverage, test bench components. **Data Types:** Built in Data types, fixed and dynamic arrays, Queues, associative arrays, linked lists, array methods, choosing a storage type, creating new types with type def, creating user defined structures, type conversion, Enumerated types, constants and strings, Expression width.	L1, L2
Module 2	
Procedural Statements and Routines: Procedural statements, Tasks, Functions and void functions, Task and function overview, Routine arguments, returning from a routine, Local data storage, time values. **Converting the test bench and design:** Separating the test bench and design, The interface construct, Stimulus timing, Interface driving and sampling, System Verilog assertions.	L1,L2,L3
Module 3	
Randomization: Introduction, Randomization in System Verilog, Constraint details, Solution probabilities, Valid constraints, In-line constraints, Random number functions, Common randomization problems, Iterative and array constraints, Random control.	L1,L2,L3
Module 4	
Threads and Interprocess Communication: Working with threads, Disabling threads, Interprocess	L1,L2,L3

communication, Events, semaphores, Mailboxes, Building a test bench with threads and Interprocess Communication.	
Module 5	
Functional Coverage: Coverage types, Coverage strategies, Simple coverage example, Anatomy of Cover group and Triggering a Cover group, Data sampling, Cross coverage, Generic Cover groups, Coverage options, Analyzing coverage data, measuring coverage statistics during simulation.	L1,L2,L3

Course Outcomes: After studying this course, students will be able to:

- Write test benches for moderately complex digital circuits
- Use System Verilog language
- Appreciate functional coverage
- Apply constrained random tests benches using System Verilog
- Analyze a verification case and apply System Verilog to verify the design

Question paper pattern:

- The question paper will have 10 full questions carrying equal marks.
- Each full question consists of 16 marks with a maximum of four sub questions.
- There will be 2 full questions from each module covering all the topics of the module
- The students will have to answer 5 full questions, selecting one full question from each module.

Text Book:

Chris Spear, 'System Verilog for Verification – A guide to learning the Test bench language features', Springer Publications, 2nd Edition, 2010.

Reference Book:

Stuart Sutherland, Simon Davidmann, Peter Flake, "System Verilog for Design-A guide to using system verilog for Hardware design and modeling", Springer Pulications, 2nd Edition, 2006.

VLSI Design for Signal Processing [As per Choice Based credit System (CBCS) Scheme SEMESTER – II			
Subject Code	16EVE252	IA Marks	20
Number of Lecture Hours/Week	03	Exam marks	80
Total Number of Lecture Hours	40 (8 Hours per Module)	Exam Hours	03
CREDITS – 03			

Course Objectives: This course will enable students to:

- Learn several high-level architectural transformations that can be used to design families of architectures for a given algorithm.
- Deal with high-level algorithm transformations such as strength reduction, look-ahead and relaxed look-ahead.

Modules	**RBT Level**
Module 1	
Introduction to DSP Systems: Typical DSP Algorithms, DSP Application Demands and Scaled CMOS Technologies, Representations of DSP Algorithms. **Iteration Bounds:** Data flow graph Representations, loop bound and Iteration bound.	L1, L2
Module 2	
Iteration Bounds: Algorithms for Computing Iteration Bound, Iteration Bound of multi rate data flow graphs. **Pipelining and Parallel Processing:** pipelining of FIR Digital Filters, parallel processing, Pipelining and parallel processing for low power.	L1,L2,L3
Module 3	
Retiming: Definition and Properties, Solving Systems of Inequalities, Retiming Techniques, **Unfolding**: An Algorithm for Unfolding, Properties of Unfolding, Critical path, Unfolding and Retiming, Application of Unfolding. **Systolic Architecture Design:** systolic array design Methodology, FIR systolic array.	L1,L2,L3
Module 4	
Systolic Architecture Design: Selection of Scheduling Vector, Matrix-Matrix Multiplication and 2D systolic Array Design, Systolic Design for space representation containing Delays. **Fast convolution**: Cook-Toom Algorithm, Winograd Algorithm, Iterated convolution, cyclic convolution Design of fast convolution Algorithm by Inspection.	L1,L2,L3
Module 5	
Pipelined and Parallel Recursive and Adaptive Filter: Pipeline Interleaving in Digital Filter, first order IIR digital Filter, Higher order IIR digital Filter, parallel processing for IIR filter, Combined pipelining and parallel processing for IIR Filter, Low power IIR Filter Design Using Pipelining and parallel processing, pipelined adaptive	L1,L2,L3

digital filter.

Course Outcomes: After studying this course, students will be able to:

- Illustrate the use of various DSP algorithms and addresses their representation using block diagrams, signal flow graphs and data-flow graphs
- Use pipelining and parallel processing in design of high-speed /low-power applications
- Apply unfolding in the design of parallel architecture
- Evaluate the use of look-ahead techniques in parallel and pipelined IIR Digital filters.
- Develop an algorithm or architecture or circuit design for DSP applications

Question paper pattern:

- The question paper will have 10 full questions carrying equal marks.
- Each full question consists of 16 marks with a maximum of four sub questions.
- There will be 2 full questions from each module covering all the topics of the module
- The students will have to answer 5 full questions, selecting one full question from each module.

Text Book:

Keshab K.Parthi, "VLSI Digital Signal Processing systems, Design and implementation ", Wiley 1999.

Reference Books:

1. Mohammed Isamail and Terri Fiez, "Analog VLSI Signal and Information Processing ", Mc Graw-Hill,1994.
2. S.Y. Kung, H.J. White House, T. Kailath, " VLSI and Modern Signal Processing ", Prentice Hall, 1985.
3. Jose E. France, Yannis Tsividis, " Design of Analog - Digital VLSI Circuits for Telecommunication and Signal Processing ", Prentice Hall, 1994.
4. Lars Wanhammar, “DSP Integrated Circuits”, Academic Press Series in Engineering, 1st Edition.

Micro Electro Mechanical Systems

[As per Choice Based credit System (CBCS) Scheme

SEMESTER – II

Subject Code	16ELD253	IA Marks	20
Number of Lecture Hours/Week	04	Exam marks	80
Total Number of Lecture Hours	40 (08 Hours per Module)	Exam Hours	03

CREDITS – 03

Course Objectives: This course will enable students to:

- Know an overview of microsystems, their fabrication and application areas.
- Teach working principles of several MEMS devices.
- Develop mathematical and analytical models of MEMS devices
- Know methods to fabricate MEMS devices
- Expose the students to various application areas where MEMS devices can be used.

Modules	**RBT Level**
Module 1	
Overview of MEMS and Microsystems: MEMS and Microsystem, Typical MEMS and Microsystems Products, Evolution of Microfabrication, Microsystems and Microelectronics, Multidisciplinary Nature of Microsystems, Miniaturization. Applications and Markets.	L1, L2
Module 2	
Working Principles of Microsystems: Introduction, Microsensors, Microactuation, MEMS with Microactuators, Microaccelerometers, Microfluidics. **Engineering Science for Microsystems Design and Fabrication:** Introduction, Atomic Structure of Matters, Ions and Ionization, Molecular Theory of Matter and Inter-molecular Forces, Doping of Semiconductors, The Diffusion Process, Plasma Physics, Electrochemistry.	L1, L2
Module 3	
Engineering Mechanics for Microsystems Design: Introduction, Static Bending of Thin Plates, Mechanical Vibration, Thermomechanics, Fracture Mechanics, Thin Film Mechanics, Overview on Finite Element Stress Analysis.	L1,L2,L3
Module 4	
Scaling Laws in Miniaturization: Introduction, Scaling in Geometry, Scaling in Rigid-Body Dynamics, Scaling in Electrostatic Forces, Scaling of Electromagnetic Forces, Scaling in Electricity, Scaling in Fluid Mechanics, Scaling in Heat Transfer.	L1,L2,L3

Module 5	
Overview of Micro-manufacturing: Introduction, Bulk Micro-manufacturing, Surface Micromachining, The LIGA Process, Summary on Micro-manufacturing. **Microsystem Design:** Introduction, Design Considerations, Process Design, Mechanical Design, Using Finite Element Method.	L1,L2,L3

Course Outcomes: After studying this course, students will be able to:

- Appreciate the technologies related to Micro Electro Mechanical Systems.
- Understand design and fabrication processes involved with MEMS devices.
- Analyse the MEMS devices and develop suitable mathematical models
- Know various application areas for MEMS devices

Question paper pattern:

- The question paper will have 10 full questions carrying equal marks.
- Each full question consists of 16 marks with a maximum of four sub questions.
- There will be 2 full questions from each module covering all the topics of the module
- The students will have to answer 5 full questions, selecting one full question from each module.

Text Book:

Tai-Ran Hsu, MEMS and Micro systems: Design, Manufacture and Nanoscale Engineering, 2nd Ed, Wiley.

Reference Books:

1. Hans H. Gatzen, Volker Saile, Jurg Leuthold, Micro and Nano Fabrication: Tools and Processes, Springer, 2015.
2. Dilip Kumar Bhattacharya, Brajesh Kumar Kaushik, Micro electromechanical Systems (MEMS), Cenage Learning.

SoC Design

[As per Choice Based credit System (CBCS) Scheme
SEMESTER – II

Subject Code	16EVE254	IA Marks	20
Number of Lecture Hours/Week	03	Exam marks	80
Total Number of Lecture Hours	40 (8 Hours per Module)	Exam Hours	03

CREDITS – 03

Course Objectives: This course will enable students to:

- Describe the ARM processor architecture and user-level assembly language programming
- Appreciate what a high-level language (in this case, C) really needs and how those needs are met by the ARM instruction set.
- raises the issues involved in debugging systems which use embedded processor cores and in the production testing of board-level systems.
- Learn the concept of memory hierarchy, discussing the principles of memory management and caches.

Modules	**RBT Level**
Module 1	
ARM Organization and Implementation:3-stage pipeline ARM organization, 5-stage pipeline ARM organization, ARM instruction execution, ARM implementation, The ARM coprocessor interface. **The ARM Instruction Set :**Introduction, Exceptions, Conditional execution, Branch and Branch with Link (B, BL),Branch, Branch with Link and eXchange (BX, BLX),Software Interrupt (SWI),Data processing instructions, Multiply instructions, Count leading zeros (CLZ - architecture v5T only), Single word and unsigned byte data transfer instruction, Half-word and signed byte data transfer instructions ,Multiple register transfer instructions, Swap memory and register instructions (SWP), Status register to general register transfer instructions , General register to status register transfer instructions, Coprocessor instructions, Coprocessor data operations, Coprocessor data transfers, Coprocessor register transfers, Breakpoint instruction (BRK - architecture v5T only), Unused instruction space, Memory faults, ARM architecture variants.	L1,L2
Module 2	
Architectural Support for High-Level Languages: Abstraction in software design, Data types, Floating-point data types, The ARM floating-point architecture, Expressions, Conditional statements, Loops, Functions and procedures, Use of memory, Run-time environment. **Architectural Support for System Development:** The ARM memory interface, The Advanced Microcontroller Bus Architecture (AMBA), The ARM reference peripheral specification, Hardware system prototyping tools, The ARMulator, The JTAG boundary scan test architecture, The ARM debug architecture, Embedded Trace,	L1,L2

Signal processing support.	
Module 3	
ARM Processor Cores: ARM7TDMI, ARM8,ARM9TDMI, ARM10TDMI ,Discussion ,Example and exercises. **Memory Hierarchy:** Memory size and speed, On-chip memory, Caches, Cache design - an example, Memory management, Examples and exercises.	L1,L2
Module 4	
Architectural Support for Operating Systems: An introduction to operating systems, The ARM system control coprocessor, CP15 protection unit registers, ARM protection unit,CP15 MMU registers, ARM MMU architecture, Synchronization, Context switching, Input/ Output, Example and exercises. **ARM CPU Cores:** The ARM710T, ARM720T and ARM740T, The ARM810,The Strong ARM SA-110,The ARM920T and ARM940T,The ARM946E-S and ARM966E-S,The ARM1020E,Discussion,Example and exercises.	L1,L2
Module 5	
Embedded ARM Applications: The VLSI Ruby II Advanced Communication Processor, The VLSI ISDN Subscriber Processor, The One C™ VWS22100 GSM chip, The Ericsson-VLSI Bluetooth Baseband Controller, The ARM7500 and ARM7500FE, The ARM7100 364,The SA-1100 368,Examples and exercises. **The AMULET Asynchronous ARM Processors:** Self-timed design 375,AMULET1 377,AMULET2 381,AMULET2e 384,AMULET3 387,The DRACO telecommunications controller 390, A self-timed future? 396,Example and exercises.	L1,L2,L3

Course Outcomes: After studying this course, students will be able to:

- Apply the 3- and 5-stage pipeline ARM processor cores and analyse the implementation issues.
- Use the concepts and methodologies employed in designing a System-on-chip (SoC) based around a microprocessor core and in designing the microprocessor core itself.
- Understand how SoCs and microprocessors are designed and used, and why a modern processor is designed the way that it is.
- Use integrated ARM CPU cores (including StrongARM) that incorporate full support for memory management.
- Analyze the requirements of a modern operating system and use the ARM architecture to address the same.

Question paper pattern:

- The question paper will have 10 full questions carrying equal marks.
- Each full question consists of 16 marks with a maximum of four sub questions.
- There will be 2 full questions from each module covering all the topics of the module
- The students will have to answer 5 full questions, selecting one full question from each module.

Text Book:

Steve Furber, “ARM System-On-Chip Architecture”, Addison Wesley, 2nd edition.

References Books:

1. Joseph Yiu, “The Definitive Guide to the ARM Cortex-M3”, 2nd edn, Newnes, (Elsevier), 2010.
2. Sudeep Pasricha and Nikil Dutt, "On-Chip Communication Architectures: System on Chip Interconnect”, Morgan Kaufmann, Publishers © 2008.
3. Michael Keating, Pierre Bricaud, “Reuse Methodology Manual for System on Chip designs”, Kluwer Accademic Publishers, 2nd edition, 2008.

VLSI and ES Lab-2

[As per Choice Based Credit System (CBCS) scheme]

SEMESTER – II

Laboratory Code	16EVEL26	IA Marks	20
Number of Lecture Hours/Week	03	Exam marks	80
Total Number of Lecture Hours	01Hr Tutorial (Instructions) + 02 Hours Laboratory	Exam Hours	03

CREDITS – 02

Course objectives: This laboratory course enables students to:

- Learn the CAD tool and the flow of the Full Custom IC design cycle.
- Learn running DRC, LVS and Parasitic Extraction of the various designs.
- Create various components like inverter, differential amplifier and use the same in the design of operational amplifier, R-2R based DAC and ADC.
- Understand the suitability of different techniques of IPC and task switching in a multithreaded application.
- Study and implement different types of data structures required to implement inter task communication.
- Implement Inter task communication using an appropriate data structure.

Part – A: Experiments to be done using CADENCE/SYNOPSIS/MENTOR GRAPHICS/TANNER Tool	**RBT Level**
1. Design an **Inverter** with given specifications*, completing the design flow mentioned below: a. Draw the schematic and verify the following i) DC Analysis ii) Transient Analysis b. Draw the Layout and verify the DRC, ERC c. Check for XX d. Extract RC and back annotate the same and verify the Design e. Verify & Optimize for Time, Power and Area to the given constraint*** (Following specification may be used to design an Inverter in gpdk 180nm technology with minimum area: i. Maximum output rise time=100ps ii. Maximum output fall time=100ps iii. $P_{avg} \leq 15\mu w$ iv. Load capacitance= 50fF v. Input rise time=200ps vi. Input fall time=200ps Choose maximum frequency based on the power)	L3
Design the following circuits with given specifications*, completing the design flow mentioned below: a. Draw the schematic and verify the following i) DC Analysis ii) AC Analysis iii) Transient Analysis	L3

b. Draw the Layout and verify the DRC, ERC, LVS c. Check for XX d. Extract RC and back annotate the same and verify the Design. 2. i) A Single Stage differential amplifier ii) Common source amplifier 3. Design an op-amp with given specification* using given differential amplifier Common source amplifier in library** 4. Design a 4 bit R-2R based DAC for the given specification**	
5. Design an Integrator and Differentiator using OPAMP (First Order)	
6. Design and characterize a basic Sigma delta ADC from the available designs.	
7. Design a simple NAND/NOR gate using any one of the tools given above. (Any other experiments may be added in supportive of the course) * Appropriate specification should be given. ** Applicable Library should be added & information should be given to the Designer. *** An appropriate constraint should be given	
Part – B: Experiments to be done using Linux	
1. Develop and test programs to (a) create child process and display it's id and (b) Execute child process function using switch structure	
2. Develop and test program for a multithreaded application, where communication is through a buffer for the conversion of lowercase text to uppercase text, using semaphore concept.	
3. Develop and test program for a multithreaded application, where communication is through shared memory for the conversion of lowercase text to uppercase text.	
4. Develop program for inter-thread communication using message queue. Data is to be input from the keyboard for the chosen application.	
5. Create 'n' number of child threads. Each thread prints the message "I'm in thread number …" and sleeps for 50 ms and then quits. The main thread waits for complete execution of all the child threads and then quits. Compile and execute in Linux.	
6. Implement the multi-thread application satisfying the following : i. Two child threads are created with normal priority. ii. Thread 1 receives and prints its priority and sleeps for 50ms and then quits. iii. Thread 2 prints the priority of the thread 1 and rises its priority to above normal and retrieves the new priority of thread 1, prints it and then quits. iv. The main thread waits for the child thread to complete its job and	L3

quits.

7. Implement the usage of anonymous pipe with 512 bytes for data sharing between parent and child processes using handle inheritance mechanism

Course outcomes: This laboratory course enable the students to:

- Design Analog, digital and mixed mode circuits
- Learn the various issues in Mixed signal designs basically data converters.
- Acquire hands-on skills of using CAD tools in VLSI design.
- Appreciate the design process in VLSI through a mini-project on the design of a CMOS sub-system.
- Select a suitable task switching technique in a multithreaded application.
- Implement different techniques of message passing and Inter task communication.
- Implement different data structures such as pipes, queues and buffers in multithreaded programming.

Conduct of Practical Examination:

- All laboratory experiments are to be included for practical examination.
- For examination, one experiment from Part-A and One experiment from Part-B is to be set.
- Strictly follow the instructions as printed on the cover page of answer script for breakup of marks.
- Change of experiment is allowed only once and Marks allotted to the Procedure part to be made zero.

Reference Book: (for some of the Part-B programs)

Dreamtech Software Team, "Programming for Embedded Systems", John Wiley, India Pvt. Ltd., 2008.

M.Tech-VLSI & ES-2016-FOURTH SEMESTER SYLLABUS

Synthesis and Optimization of Digital Circuits [As per Choice Based credit System (CBCS) Scheme SEMESTER – IV			
Subject Code	16ELD41	IA Marks	20
Number of Lecture Hours/Week	04	Exam marks	80
Total Number of Lecture Hours	50 (10 Hours per Module)	Exam Hours	03
CREDITS – 04			

Course Objectives: This course will enable students:

- Understand the need for optimization and dimensions of optimization for digital circuits.
- Understand basic optimization techniques used in circuits design
- Understand advanced tools and techniques in digital systems design including Hardware Modeling and Compilation Techniques.
- Explain details of Logic-Level synthesis and optimization techniques for combinational and sequential circuits.
- Explain the concept of scheduling and resource binding for optimization.

Modules	**RBT Level**
Module 1	
Introduction to Synthesis and optimization: Design of Microelectronics circuits, Computer aided Synthesis and Optimization. **Hardware Modeling**: HDLs for Synthesis, Abstract models, Compilation and Behavioral Optimization. (Text1: Topics from Chap. 1,3)	L1, L2, L3
Module 2	
Graph theory for CAD for VLSI: Graphs, Combinatorial Optimization, Graph Optimization problems and Algorithms, Boolean Algebra and Applications. **Architectural Synthesis and Optimization:** Fundamental Architectural Synthesis problems, Area and Performance Estimation, Strategies for Architectural Optimization, Data path Synthesis, Control Path Synthesis.(Text1: Topics From Chap. 2,4)	L1, L2, L3
Module 3	
Two level Combinational Logic Optimization: Introduction, Logic Optimizations, Operations on Two level Logic Covers, Algorithms for Logic Minimization, Symbolic Minimization and Encoding Problems. **Multiple Level Combinational Logic Optimization**: Introduction, Models and Transformations for Combinational Networks, The Algebraic Model, The Boolean Model. (Text1: Chap. 7, 8)	L1, L2, L3
Module 4	
Sequential Logic Optimization: Introduction, Sequential Logic Optimization using State based Models, Sequential Logic Optimization using Network Models, Implicit FSM Traversal Methods, Testability concerns for	L1, L2, L3

Synchronous Circuits. (Text 1: Chap. 9)	
Module 5	
Scheduling Algorithms: Introduction, A Model for Scheduling problems, Scheduling with Resource Constraints, Scheduling without Resource Constraints, Scheduling Algorithms for Extended Sequencing Models, Scheduling Pipelined Circuits. **Resource Sharing and Binding:** Sharing and Binding for Resource dominated circuits, Sharing and Binding for General Circuits, Concurrent Binding and Scheduling, Resource sharing and Binding for Non – Scheduled Sequencing Graphs. (Text1: Chap. 5,6)	L1, L2, L3

Course Outcomes: After studying this course, students will be able to:

- Understand the process of synthesis and optimization in a top down approach for digital circuits models using HDLs.
- Understand the terminologies of graph theory and its algorithms to optimize a Boolean equation.
- Apply different two level and multilevel optimization algorithms for combinational circuits
- Apply the different sequential circuit optimization methods using state models and network models.
- Apply different scheduling algorithms with resource binding and without resource binding for pipelined sequential circuits and extended sequencing models.

Question paper pattern:

- The question paper will have 10 full questions carrying equal marks.
- Each full question consists of 16 marks with a maximum of four sub questions.
- There will be 2 full questions from each module covering all the topics of the module
- The students will have to answer 5 full questions, selecting one full question from each module.

Text Book:

Giovanni De Micheli, "Synthesis and Optimization of Digital Circuits", Tata McGraw-Hill, 2003.

Reference Book:

Edwars M.D., Automatic Logic synthesis Techniques for Digital Systems, Macmillan New Electronic Series, 1992.

CMOS RF Circuit Design

[As per Choice Based credit System (CBCS) Scheme
SEMESTER – IV

Subject Code	16EVE421	IA Marks	20
Number of Lecture Hours/Week	03	Exam marks	80
Total Number of Lecture Hours	40 (8 Hours per Module)	Exam Hours	03

CREDITS – 03

Course Objectives: This course will enable students to:

- Learn basic concepts in RF and microwave design emphasising the effects of nonlinearity and noise.
- Appreciate communication system, multiple access and wireless standards necessary for RF circuit design.
- Deal with transceiver architecture, various receiver and transmitter designs, their merits and demerits
- Understand the design of RF building blocks such as Low Noise Amplifiers and Mixers

Modules	**RBT Level**
Module 1	
Introduction to RF Design and Wireless Technology: **Basic concepts in RF design(I):** General considerations, Effects of Nonlinearity, Noise, Sensitivity and dynamic range	L1,L2,L3
Module 2	
Basic concepts in RF design (II): Passive impedance transformation, scattering parameters, analysis of nonlinear dynamic systems	L1,L2,L3
Module 3	
Communication Concepts: General concepts, analog modulation, digital modulation, spectral re-growth, Mobile RF communications, Multiple access techniques, Wireless standards	L1,L2,L3
Module 4	
Transceiver Architecture (I): General considerations, Receiver architecture,	L1,L2,L3
Module 5	
Transceiver Architecture (II): Transmitter architectures **Low Noise Amplifiers:** LNA topologies: common-source stage with inductive load, common-source stage with resistive feedback. **Mixers:** General considerations, passive down conversion mixers.	L1,L2,L3

Course Outcomes: After studying this course, students will be able to:

1. Analyse the effect of nonlinearity and noise in RF and microwave design.
2. Exemplify the approaches taken in actual RF products.
3. Minimize the number of off-chip components required to design mixers and Low-Noise Amplifiers.
4. Explain various receivers and transmitter topologies with their merits and

drawbacks.

5. Demonstrate how the system requirements define the parameters of the circuits and how the performance of each circuit impacts that of the overall transceiver.

Question paper pattern:

- The question paper will have 10 full questions carrying equal marks.
- Each full question consists of 16 marks with a maximum of four sub questions.
- There will be 2 full questions from each module covering all the topics of the module
- The students will have to answer 5 full questions, selecting one full question from each module.

Text Book:

B. Razavi, "**RF Microelectronics**", PHI, second edition.

Reference Books:

1. R. Jacob Baker, H.W. Li, D.E. Boyce "**CMOS Circuit Design, layout and Simulation**", PHI 1998.
2. Thomas H. Lee "**Design of CMOS RF Integrated Circuits**" Cambridge University press 1998.
3. Y.P. Tsividis, "**Mixed Analog and Digital Devices and Technology**", TMH 1996

Advances in Image Processing

[As per Choice Based credit System (CBCS) Scheme

SEMESTER – IV

Subject Code	16ECS422	IA Marks	20
Number of Lecture Hours/Week	03	Exam marks	80
Total Number of Lecture Hours	40 (8 Hours per Module)	Exam Hours	03

CREDITS – 03

Course Objectives: This course will enable students to:

- Acquire fundamental knowledge in understanding the representation of the digital image and its properties
- Equip with some pre-processing techniques required to enhance the image for further analysis purpose.
- Select the region of interest in the image using segmentation techniques.
- Represent the image based on its shape and edge information.
- Describe the objects present in the image based on its properties and structure.

Modules	**RBT Level**
Module 1	
The image, its representations and properties: Image representations a few concepts, Image digitization, Digital image properties, Color images.	L1
Module 2	
Image Pre-processing: Pixel brightness transformations, geometric transformations, local pre-processing.	L1, L2
Module 3	
Segmentation: Thresholding; Edge-based segmentation – Edge image thresholding, Edge relaxation, Border tracing, Hough transforms; Region – based segmentation – Region merging, Region splitting, Splitting and merging, Watershed segmentation, Region growing post-processing.	L1, L2, L3
Module 4	
Shape representation and description: Region identification; Contour-based shape representation and description – Chain codes, Simple geometric border representation, Fourier transforms of boundaries, Boundary description using segment sequences, B-spline representation; Region-based shape representation and description – Simple scalar region descriptors, Moments, Convex hull.	L1, L2, L3
Module 5	
Mathematical Morphology: Basic morphological concepts, Four morphological principles, Binary dilation and erosion, Skeletons and object marking, Morphological segmentations and watersheds.	L1, L2, L3

Course Outcomes: After studying this course, students will be able to:

- Understand the representation of the digital image and its properties
- Apply pre-processing techniques required to enhance the image for its further analysis.

- Use segmentation techniques to select the region of interest in the image for analysis
- Represent the image based on its shape and edge information.
- Describe the objects present in the image based on its properties and structure.
- Use morphological operations to simplify images, and quantify and preserve the main shape characteristics of the objects.

Question paper pattern:

- The question paper will have 10 full questions carrying equal marks.
- Each full question consists of 16 marks with a maximum of four sub questions.
- There will be 2 full questions from each module covering all the topics of the module
- The students will have to answer 5 full questions, selecting one full question from each module.

Text Books:

1. Milan Sonka, Vaclav Hlavac, Roger Boyle, "Image Processing, Analysis, and Machine Vision", Cengage Learning, 2013, ISBN: 978-81-315-1883-0

Reference Books:

1. Geoff Doughertry, Digital Image Processing for Medical Applications, Cambridge university Press, 2010
2. S.Jayaraman, S Esakkirajan, T.Veerakumar, Digital Image Processing, Tata McGraw Hill, 2011

High Speed VLSI Design

[As per Choice Based credit System (CBCS) Scheme

SEMESTER – IV

Subject Code	16EVE423	IA Marks	20
Number of Lecture Hours/Week	03	Exam marks	80
Total Number of Lecture Hours	40 (8 Hours per Module)	Exam Hours	03

CREDITS – 03

Course Objectives: This course will enable students to:

- Learn sources of process – driven performance variation in quarter-micron CMOS and apply the rules of thumb.
- Comprehend non-clocked static circuit families, used to implement combinatorial logic.
- Interpret the design styles used for clocked and non-clocked systems.
- Explore the design parameters such as on-chip device length tolerance, supply rail inconsistency and temperature variations.

Modules	**RBT Level**
Module 1	
Process Variability: Introduction**,** Front-end -of-line variability considerations, charge loss mechanisms, back-end-of- line variability considerations.	L1, L2
Module 2	
Non-Clocked logic styles: Introduction, static CMOS structures, DC VS logic, Non-clocked pass-gate families. **Clocked logic styles**: Introduction, single-rail domino logic styles. Dual-rail domino structures, latched domino structures, clocked-pass gate logic.	L1, L2,L3
Module 3	
Circuit Design margin and design variability: Introduction, process induced variation, design induced variations, and application induced variations', Noise. **Latching Strategies:** Introduction, basic latch design, latching single ended logic, latching differential logic, race-free latched for pre-charge logic.	L1, L2,L3
Module 4	
Interface Techniques: Introduction, signaling standard, chip-chip communication networks, ESD protection, Driver design techniques, receiver design techniques.	L1, L2,L3
Module 5	
Clocking styles: Introduction, clock jitter and skew, clock	L1, L2,L3

generation and clock distribution.

Course Outcomes: After studying this course, students will be able to:

1. Accomplish their goal in achieving the trade offs in performance, power, area, reliability and cost by the selection of design styles.
2. Analyse strengths and weakness of non-clocked static circuit families in terms of characteristics.
3. Differentiate the styles used for clocked and non-clocked circuit families.
4. Interpret the performance considerations to enable high speed communication; by choosing the input and output convention compatible with signal levels required for the design.

Question paper pattern:

- The question paper will have 10 full questions carrying equal marks.
- Each full question consists of 16 marks with a maximum of four sub questions.
- There will be 2 full questions from each module covering all the topics of the module
- The students will have to answer 5 full questions, selecting one full question from each module.

Text Book:

Kerry Bernstein & et. Al., "**High Speed CMOS Design Styles"**, Kluwer, 1999.

Reference Books:

1. Howard Johnson & Martin Graham, **"High Speed Digital Design"** A Handbook of Black Magic, Prentice Hall PTR, 1993.
2. William S. Dally & John W. Poulton, **"Digital Systems Engineering"**, Cambridge University Press, 1998.
3. Masakazu Shoji, **"High Speed Digital Circuits"**, Addison Wesley Publishing Company, 1996.

Reconfigurable Computing

[As per Choice Based credit System (CBCS) Scheme
SEMESTER – IV

Subject Code	16ELD424	IA Marks	20
Number of Lecture Hours/Week	03	Exam marks	80
Total Number of Lecture Hours	40 (8 Hours per Module)	Exam Hours	03

CREDITS – 03

Course Objectives: The aim of this course is to enable the students to

- Acquire fundamental knowledge and understanding of principles and practice in reconfigurable architecture.
- Understand the FPGA design principles, and logic synthesis.
- Integrate hardware and software technologies for reconfiguration computing focusing on partial reconfiguration design.
- Focus on different domains of applications on reconfigurable computing.

Modules	**RBT Level**
Module 1	
Introduction : History, Reconfigurable Vs Processor based system, RC Architecture. **Reconfigurable Logic Devices**: Field Programmable Gate Array, Coarse Grained Reconfigurable Arrays. **Reconfigurable Computing System**: Parallel Processing on Reconfigurable Computers, A survey of Reconfigurable Computing System. (Text 1)	LI, L2
Module 2	
Languages and Compilation: Design Cycle, Languages, HDL, High Level Compilation, Low level Design flow, Debugging Reconfigurable Computing Applications. (Text 1)	L1,L2
Module 3	
Implementation: Integration, FPGA Design flow, Logic Synthesis. **High Level Synthesis for Reconfigurable Devices:** Modelling, Temporal Partitioning Algorithms. (Text 2)	L1, L2, L3
Module 4	
Partial Reconfiguration Design: Partial Reconfiguration Design, Bitstream Manipulation with JBits, The modular Design flow, The Early Access Design Flow, Creating Partially Reconfigurable Designs, Partial Reconfiguration using Hansel-C Designs, Platform Design. (Text 2)	L1,L2
Module 5	
Signal Processing Applications: Reconfigurable computing for DSP, DSP application building blocks, Examples: Beamforming, Software Radio, Image and video processing, Local Neighbourhood functions, Convolution. (Text 1) **System on a Programmable Chip:** Introduction to SoPC, Adaptive Multiprocessing on Chip. (Text 2)	L1, L2, L3

Course Outcomes:: After studying this course, students will be able to:

- Simulate and synthesize the reconfigurable computing architectures.
- Use the reconfigurable architectures for the design of a digital system.

- Design of digital systems for a variety of applications on signal processing and system on chip configurations.

Question paper pattern:

- The question paper will have 10 full questions carrying equal marks.
- Each full question consists of 16 marks with a maximum of four sub questions.
- There will be 2 full questions from each module covering all the topics of the module
- The students will have to answer 5 full questions, selecting one full question from each module.

Text Books:

1. M. Gokhale and P. Graham, "Reconfigurable Computing: Accelerating Computation with Field-Programmable Gate Arrays", Springer, 2005.

2. C. Bobda, "Introduction to Reconfigurable Computing: Architectures, Algorithms and Applications", Springer, 2007.

Reference Books:

1. D. Pellerin and S. Thibault, "Practical FPGA Programming in C", Prentice-Hall, 2005.

2. W. Wolf, "FPGA Based System Design", Prentice-Hall, 2004.

3. R. Cofer and B. Harding, "Rapid System Prototyping with FPGAs: Accelerating the Design Process", Newnes, 2005.

VISVESVARAYA TECHNOLOGICAL UNIVERSITY, BELAGAVI
Scheme of Teaching and Examination: 2018-19
M.Tech in VLSI Design & Embedded Systems (EVE)
Choice Based Credit System (CBCS)

I SEMESTER

Sl. No	Course	Course Code	Course Title	Teaching Hours /Week		Examination				Credits
				Theory	Practical/ Field work/ Assignment	Duration in hours	CIE Marks	SEE Marks	Total Marks	
1	PCC	18ELD11	Advanced Engineering Mathematics	04	--	03	40	60	100	4
2	PCC	18EVE12	ASIC Design	04	--	03	40	60	100	4
3	PCC	18EVE13	Advanced Embedded System	04	--	03	40	60	100	4
4	PCC	18EVE14	VLSI Testing	04	--	03	40	60	100	4
5	PCC	18EVE15	Digital VLSI Design	04	--	03	40	60	100	4
6	PCC	18EVEL16	VLSI & ES Lab-1	-	04	03	40	60	100	2
7	PCC	18RMI17	Research Methodology and IPR	02	--	03	40	60	100	2
			TOTAL	**22**	**04**	**21**	**280**	**420**	**700**	**24**

Note:- PCC: Professional Core Course

Internship: All the students shall undergo mandatory internship of 6 weeks during the vacation of I and II semesters and /or II and III semesters. University examination will be conducted during III semester and prescribed credit shall be included in the III semester. Internship shall be considered as a head of passing and shall be considered for the award of degree. Those, who do not take-up/complete the internship shall be declared as failed and have to complete during subsequent University examination after satisfying the internship requirements.

VISVESVARAYA TECHNOLOGICAL UNIVERSITY, BELAGAVI
Scheme of Teaching and Examination: 2018-19
M.Tech in VLSI Design & Embedded Systems (EVE)
Choice Based Credit System (CBCS)

II SEMESTER

Sl. No	Course	Course Code	Course Title	Teaching Hours /Week		Examination				Credits
				Theory	Practical/ Field work/ Assignment	Duration in hours	CIE Marks	SEE Marks	Total Marks	
1	PCC	18EVE21	Design of Analog and Mixed mode VLSI Circuits	04	--	03	40	60	100	4
2	PCC	18EVE22	Real Time Operating System	04	--	03	40	60	100	4
3	PCC	18EVE23	System Verilog	04	--	03	40	60	100	4
4	PEC	18XXX24X	Professional Elective 1	04	--	03	40	60	100	4
5	PEC	18XXX25X	Professional Elective 2	04	--	03	40	60	100	4
6	PCC	18EVEL26	VLSI & ES Lab-2	--	04	03	40	60	100	2
7	PCC	18EVE27	Technical Seminar	--	02	--	100	--	100	2
TOTAL				**20**	**06**	**18**	**340**	**360**	**700**	**24**

Note:- PCC: Professional Core Course, PEC: Professional Elective Course

Professional Elective 1		Professional Elective 2	
Course Code Under 18XXX24X	**Course Title**	**Course Code Under 18XXX25X**	**Course Title**
18EVE241	Advances in VLSI Design	18EVE251	Low Power VLSI Design
18EVE242	Nanoelectronics	18EVE252	SoC Design
18EVE243	Static Timing Analysis	18ELD253	Micro Electro Mechanical Systems

Note:

1. Technical Seminar: CIE marks shall be awarded by a committee comprising of HoD as Chairman, Guide/co-guide in any and a senior faculty of the department. Participation in seminar by all postgraduate students of the same and other semesters of the programme shall be mandatory.

The CIE marks awarded for Technical Seminar, shall be based on the evaluation of Seminar Report, Presentation skill and Question and Answer session in the ratio 50:25:25.

2. Internship: All the students shall undergo mandatory internship of 6 weeks during the vacation of I and II semesters and /or II and III semesters. A University examination will be conducted during III semester and prescribed credit shall be included in the III semester. Internship shall be considered as head of passing and shall be considered for the award of degree. Those, who do not take-up/complete the internship shall be declared as failed and have to complete during subsequent University examination after satisfying the internship requirements.

VISVESVARAYA TECHNOLOGICAL UNIVERSITY, BELAGAVI
Scheme of Teaching and Examination: 2018-19
M.Tech in VLSI Design & Embedded Systems (EVE)
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III SEMESTER

Sl. No	Course	Course Code	Course Title	Teaching Hours /Week		Examination				Credits
				Theory	Practical/ Field work/ Assignment	Duration in hours	CIE Marks	SEE Marks	Total Marks	
1	PCC	18EVE31	CAD of Digital Systems	04	--	03	40	60	100	4
2	PEC	18XXX32X	Professional Elective 3	04	--	03	40	60	100	4
3	PEC	18XXX33X	Professional Elective 4	04	--	03	40	60	100	4
4	Proj	18EVE34	Evaluation of Project Phase -1	--	02	--	100	--	100	2
5	INT	18EVE35	Internship	(Completed during the intervening vacation of I and II semesters and /or II and III semesters.)		03	40	60	100	6
TOTAL				**12**	**02**	**12**	**260**	**240**	**500**	**20**

Note:- PCC: Professional Core Course, PEC: Professional Elective Course, Proj: Project, INT: Internship

Professional Elective 3		Professional Elective 4	
Course Code Under 18XXX32X	**Course Title**	**Course Code Under 18XXX33X**	**Course Title**
18ECS321	Advances in Image Processing	18EVE331	VLSI for Signal Processing
18EVE322	CMOS RF Circuit Design	18ESP332	Pattern Recognition & Machine Learning
18EVE323	Embedded Linux System Design And Development	18ECS333	Internet of Things

Note:

1. Project Phase-1: Students in consultation with the guide/co-guide if any, shall pursue literature survey and complete the preliminary requirements of selected Project work. Each student shall prepare relevant introductory project document, and present a seminar.

CIE marks shall be awarded by a committee comprising of HoD as Chairman, Guide and a senior faculty of the department. The CIE marks awarded for project work phase -1, shall be based on the evaluation of Project Report, Project Presentation skill and Question and Answer session in the ratio 50:25:25.

SEE (University examination) shall be as per the University norms.

2. Internship: Those, who have not pursued /completed the internship shall be declared as failed and have to complete during subsequent University examinations after satisfy the internship requirements.

Internship SEE (University examination) shall be as per the University norms.

VISVESVARAYA TECHNOLOGICAL UNIVERSITY, BELAGAVI
Scheme of Teaching and Examination: 2018-19
M.Tech in VLSI Design & Embedded Systems (EVE)
Choice Based Credit System (CBCS)

IV SEMESTER

Sl. No	Course	Course Code	Course Title	Teaching Hours /Week		Examination				Credits
				Theory	Practical/ Field work/ Assignment	Duration in hours	CIE Marks	SEE Marks Viva voce	Total Marks	
1	Proj	18EVE41	Project Work Phase -2	--	04	03	40	60	100	20
			TOTAL	--	**04**	**03**	**40**	**60**	**100**	**20**

Note: Proj: Project.

Note:

1. Project Phase-2:

CIE marks shall be awarded by a committee comprising of HoD as Chairman, Guide/co-guide, if any and a Senior faculty of the department. The CIE marks awarded for Project Work Phase -2, shall be based on the evaluation of Project Report subjected to plagiarism check, Project Presentation skill and Question and Answer session in the ratio 50:25:25.

SEE shall be at the end of IV semester. Project work evaluation and Viva-Voce examination (SEE), after satisfying the plagiarism check, shall be as per the University norms.

M.Tech-VLSI & ES-2018- FIRST SEMESTER SYLLABUS

ADVANCED ENGINEERING MATHEMATICS **[As per Choice Based Credit System (CBCS) Scheme]** **SEMESTER – I**			
Course Code	**18ELD11**	**CIE**	**40**
Number of Lecture Hours/Week	**04**	**SEE Marks**	**60**
Total Number of Lecture Hours	**50 (10 Hours per Module)**	**Exam Hours**	**03**

CREDITS – 04

Course objectives: This course will enable students to:

- To learn principles of advanced engineering mathematics through linear algebra and calculus of variations.
- To understand probability theory and random process that serve as an essential tool for applications of electronics and communication engineering sciences

Modules	**(RBT) Level**
Module -1	
Linear Algebra-I Introduction to vector spaces and sub-spaces, definitions, illustrative example. Linearly independent and dependent vectors- Basis-definition and problems. Linear transformations-definitions. Matrix form of linear transformations-Illustrative examples (Text Book:1).	**L1,L2**
Module -2	
Linear Algebra-II Computation of eigen values and eigen vectors of real symmetric matrices-Given's method. Orthogonal vectors and orthogonal bases. Gram-Schmidt orthogonalization process (Text. Book:1).	**L1,L2**
Module -3	
Calculus of Variations : - Concept of functional- Eulers equation**.** Functional dependent on first and higher order derivatives, Functional on several dependent variables. Isoperimetric problems-variation problems with moving boundaries. (Text.Book:2)	**L1,L2**
Module -4	
Probability Theory:-Review of basic probability theory. Definitions of random variables and probability distributions, probability mass and density functions, expectation, moments, central moments, characteristic functions, probability generating and moment generating functions-illustrations. Poisson, Gaussian and Erlang distributions-examples. (Text Book: 3)	**L1,L2**
Module -5	

Engineering Applications on Random processes:- Classification. Stationary, WSS and ergodic random process. Auto-correlation function-properties, Gaussian random process. (Text Book: 3)	**L1,L2**

Course Outcomes: After studying this course, students will be able to:

1. Understand vector spaces, basis, linear transformations and the process of obtaining matrix of linear transformations arising in magnification and rotation of images.
2. Apply the technique of singular value decomposition for data compression, least square approximation in solving inconsistent linear systems.
3. Utilize the concepts of functional and their variations in the applications of communication systems, decision theory, synthesis and optimization of digital circuits.
4. Learn the idea of random variables (discrete/continuous) and probability distributions in analyzing the probability models arising in control systems and system communications.
5. Analyze random process through parameter-dependent variables in various random processes.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

ASIC DESIGN

[As per Choice Based Credit System (CBCS) scheme]

SEMESTER- I

Subject Code	**18EVE12**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**04**	**SEE Marks**	**60**
Total Number of Lecture Hours	**50 (10 Hours per Module)**	**Exam Hours**	**03**

CREDITS – 04

Course objectives: This course will enable students to:

- Explain ASIC methodologies and programmable logic cells to implement a function on IC.
- Analyse back-end physical design flow, including partitioning, floor-planning, placement, and routing.
- Gain sufficient theoretical knowledge for carrying out FPGA and ASIC designs.
- Design CAD algorithms and explain how these concepts interact in ASIC design.

Modules	**(RBT) Level**
Module -1	
Introduction to ASICs: Full custom, Semi-custom and Programmable ASICs, ASIC Design flow, ASIC cell libraries. **CMOS Logic:** Data path Logic Cells**:** Data Path Elements, Adders: Carry skip, Carry bypass, Carry save, Carry select, Conditional sum, Multiplier (Booth encoding), Data path Operators, I/O cells, Cell Compilers.	**L1,L2**
Module -2	
ASIC Library Design: Logical effort: Predicting Delay, Logical area and logical efficiency, Logical paths, Multi stage cells, Optimum delay and number of stages, library cell design. **Programmable ASIC Logic Cells:** MUX as Boolean function generators, Acted ACT: ACT 1, ACT 2 and ACT 3 Logic Modules, Xilinx LCA: XC3000 CLB, Altera FLEX and MAX, Programmable ASIC I/O Cells: Xilinx and Altera I/O Block.	**L1-L3**
Module -3	
Low-level design entry: Schematic entry: Hierarchical design, The cell library, Names, Schematic Icons & Symbols, Nets, Schematic Entry for ASICs, Connections, vectored instances & buses, Edit in place, attributes, Netlist screener. **ASIC Construction:** Physical Design, CAD Tools System partitioning, Estimating ASIC size. **Partitioning:** Goals and objectives, Constructive Partitioning, Iterative Partitioning Improvement, KL, FM and Look Ahead algorithms.	**L1-L4**
Module -4	

Floor planning and placement: Goals and objectives, Measurement of delay in Floor planning, Floor planning tools, Channel definition, I/O and Power planning and Clock planning. **Placement:** Goals and Objectives, Min-cut Placement algorithm, Iterative Placement Improvement, Time driven placement methods, Physical Design Flow.	**L1-L3**
Module -5	
Routing: Global Routing: Goals and objectives, Global Routing Methods, Global routing between blocks, Back-annotation. Detailed Routing: Goals and objectives, Measurement of Channel Density, Left-Edge Algorithm, Area-Routing Algorithms, Multilevel routing, Timing –Driven detailed routing, Final routing steps, Special Routing, Circuit extraction and DRC.	**L1-L3**

Course outcomes: After studying this course, students will be able to:

1. Describe the concepts of ASIC design methodology, data path elements, logical effort and FPGA architectures.
2. Analyze the design of FPGAs and ASICs suitable for specific tasks, perform design entry and explain the physical design flow.
3. Design data path elements for ASIC cell libraries and compute optimum path delay.
4. Create floor plan including partition and routing with the use of CAD algorithms.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Book:

- Michael John Sebastian Smith, “Application - Specific Integrated Circuits” Addison-Wesley Professional; 2005.

Reference Books:

1. Neil H.E. Weste, David Harris, and Ayan Banerjee, “CMOS VLSI Design: A Circuits and Systems Perspective”, 3rd edition, Addison Wesley/ Pearson education, 2011.
2. Vikram Arkalgud Chandrasetty, “VLSI Design: A Practical Guide for FPGA and ASIC Implementations”, Springer, 2011, ISBN: 978-1-4614-1119-2.
3. Rakesh Chadha**,** Bhasker J., “An ASIC Low Power Primer”, Springer, ISBN: 978-1-4614-4270-7.

ADVANCED EMBEDDED SYSTEM
[As per Choice Based Credit System (CBCS) scheme]
SEMESTER – I

Subject	18EVE13	CIE	40
Number of Lecture Hours/Week	04	SEE Marks	60
Total Number of Lecture Hours	50 (10 Hours per Module)	Exam Hours	03

CREDITS – 04

Course objectives: This course will enable students to:
- Understand the basic hardware components and their selection method based on the characteristics and attributes of an embedded system.
- Describe the hardware software co-design and firmware design approaches
- Explain the architectural features of ARM CORTEX M3, a 32 bit microcontroller including memory map, interrupts and exceptions.
- Program ARM CORTEX M3 using the various instructions, for different applications.

Modules	(RBT) Level
Module -1	
Embedded System: Embedded vs General computing system, classification, application and purpose of ES. Core of an Embedded System, Memory, Sensors, Actuators, LED, Opto coupler, Communication Interface, Reset circuits, RTC, WDT, Characteristics and Quality Attributes of Embedded Systems (Text 1: Selected Topics from Ch -1, 2, 3).	L1, L2, L3
Module -2	
Hardware Software Co-Design, embedded firmware design approaches, computational models, embedded firmware development languages, Integration and testing of Embedded Hardware and firmware, Components in embedded system development environment (IDE), Files generated during compilation, simulators, emulators and debugging (Text 1: Selected Topics From Ch-7, 9, 12, 13).	L1, L2, L3
Module -3	
ARM-32 bit Microcontroller: Thumb-2 technology and applications of ARM, Architecture of ARM Cortex M3, Various Units in the architecture, General Purpose Registers, Special Registers, exceptions, interrupts, stack operation, reset sequence (Text 2: Ch 1, 2, 3)	L1, L2, L3
Module -4	
Instruction Sets: Assembly basics, Instruction list and description, useful instructions, Memory Systems, Memory maps, Cortex M3 implementation overview, pipeline and bus interface (Text 2: Ch-4, 5, 6).	L1, L2, L3
Module -5	

Exceptions, Nested Vector interrupt controller design, Systick Timer, Cortex-M3 Programming using assembly and C language, CMSIS (Text 2: Ch-7, 8, 10).	**L1, L2, L3**

Course Outcomes: After studying this course, students will be able to:

1. Understand the basic hardware components and their selection method based on the characteristics and attributes of an embedded system.
2. Explain the hardware software co-design and firmware design approaches.
3. Acquire the knowledge of the architectural features of ARM CORTEX M3, a 32 bit microcontroller including memory map, interrupts and exceptions.
4. Apply the knowledge gained for Programming ARM CORTEX M3 for different applications.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Books:

1. K. V. Shibu, "Introduction to embedded systems", TMH education Pvt. Ltd. 2009.

2. Joseph Yiu, “The Definitive Guide to the ARM Cortex-M3”, 2nd edn, Newnes, (Elsevier), 2010.

Reference Book:

James K. Peckol, "Embedded systems- A contemporary design tool", John Wiley, 2008.

VLSI TESTING

[As per Choice Based credit System (CBCS) Scheme

SEMESTER – I

Subject Code	**18EVE14**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**04**	**SEE marks**	**60**
Total Number of Lecture Hours	**50 (10 Hours per Module)**	**Exam Hours**	**03**

CREDITS – 04

Course Objectives: This course will enable students to:

- Learn various types of faults and fault modelling.
- Comprehend the need for testing and testable design of digital circuits
- Illustrate methods and algorithms for testing digital combinatorial networks and test pattern generation
- Exemplify methods for testing sequential circuits and memory testing
- Inferring testing methods using Boundary scan, Built-in self test and other advanced topics in digital circuit design.

Modules	**RBT Level**
Module 1	
Faults in digital circuits: Failures and Faults, Modeling of faults, Temporary Faults. (Text 1) **Logic Simulation:** Applications, Problems in simulation based design verification, types of simulation, The unknown logic values, compiled simulation, event-driven simulation, Delay models, Element evaluation, Hazard detection, Gate-level event-driven Simulation. (Text 2)	L1,L2
Module 2	
Test generation for Combinational Logic circuits: Fault Diagnosis of digital circuits, Test generation techniques for combinational circuits, Detection of multiple faults in Combinational logic circuits. (Text 1) **Testable Combinational logic circuit design:** The Read-Muller expansion technique, Three level OR-AND-OR design, Automatic synthesis of testable logic.(Text 1)	L1,L2,L3
Module 3	
Testable Combinational logic circuit design: Testable design of multilevel combinational circuits, Synthesis of random pattern testable combinational circuits, Path delay fault testable combinational logic design, Testable PLA design. (Text 1) **Test generation for Sequential circuits:** Testing of sequential circuits as Iterative combinational circuits, state table verification, Test generation based on Circuit Structure, Functional Fault models, test Generation based on Functional Fault models. (Text 1)	L1,L2,L3
Module 4	
Design of testable sequential circuits: Controllability and observability, Ad-Hoc design rules for improving testability, design of diagnosable sequential circuits, the scan-path technique for testable	L1,L2,L3

sequential circuit design, Level Sensitive Scan Design(LSSD), Random Access Scan Technique, Partial scan, testable sequential circuit design using Nonscan Techniques, Cross check, Boundary Scan. (Text 1)	
Module 5	
Built-In Self Test: Test pattern generation for BIST, Output response analysis, Circular BIST, BIST Architectures. (Text 1) **Testable Memory Design:** RAM Fault Models, Test algorithms for RAMs, Detection of pattern-sensitive faults, BIST techniques for RAM chips, Test generation and BIST for embedded RAMs. (Text1)	L1,L2,L3

Course Outcomes: After studying this course, students will be able to:

1. Analyze the need for fault modeling and testing of digital circuits
2. Generate fault lists for digital circuits and compress the tests for efficiency
3. Create tests for digital memories and analyze failures in them
4. Apply boundary scan technique to validate the performance of digital circuits
5. Design built-in self tests for complex digital circuits

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Books:

1. Lala Parag K., Digital Circuit Testing and Testability, New York, Academic Press, 1997.
2. Abramovici M, Breuer M A and Friedman A D, “Digital Systems Testing and Testable Design”, Wiley, 1994.

Reference Books:

1. Vishwani D Agarwal, “Essential of Electronic Testing for Digital, Memory and Mixed Signal Circuits”, Springer, 2002.
2. Wang, Wu and Wen, “VLSI Test Principles and Architectures”, Morgan Kaufmann, 2006.

DIGITAL VLSI DESIGN
[As per Choice Based Credit System (CBCS) scheme]
SEMESTER –I

Subject Code	**18EVE15**	**CIE Marks**	**40**
Number of Lecture Hours/Week of Lecture Hours/Week	**04**	**SEE Marks**	**60**
Total Number of Lecture Hours Lecture Hours	**50 (10 Hours per Module)**	**Exam Hours**	**03**

CREDITS – 04

Course objectives: This course will enable students to:

- Explain VLSI Design Methodologies
- Learn Static and Dynamic operation principles, analysis and design of inverter circuit.
- Infer state of the art Semiconductors Memory circuits.
- Outline the comprehensive coverage of Methodologies and Design practice that are used to reduce the Power Dissipation of large scale digital circuits.
- Illustrate VLSI and ASIC design

Modules	**(RBT) Level**
Module -1	
MOS Transistor: The Metal Oxide Semiconductor (MOS) Structure, The MOS System under External Bias, Structure and Operation of MOS Transistor, MOSFET Current-Voltage Characteristics, MOSFET Scaling and Small-Geometry Effects. **MOS Inverters-Static Characteristics**: Introduction, Resistive-Load Inverter, Inverters with n_Type MOSFET Load.	**L1, L2**
Module -2	
MOS Inverters-Static Characteristics: CMOS Inverter. **MOS Inverters**: Switching Characteristics and Interconnect Effects: Introduction, Delay-Time Definition, Calculation of Delay Times, Inverter Design with Delay Constraints, Estimation of Interconnect Parasitics, Calculation of Interconnect Delay, Switching Power Dissipation of CMOS Inverters.	**L2, L3**
Module -3	
Semiconductor Memories: Introduction, Dynamic Random Access Memory (DRAM), Static Random Access Memory (SRAM), Nonvolatile Memory, Flash Memory, Ferroelectric Random Access Memory (FRAM).	**L1, L2, L3**
Module -4	

Dynamic Logic Circuits: Introduction, Basic Principles of Pass Transistor Circuits, Voltage Bootstrapping, Synchronous Dynamic Circuit Techniques, Dynamic CMOS Circuit Techniques,High Performance Dynamic CMOS circuits. **BiCMOS Logic Circuits**: Introduction, Bipolar Junction Transistor (BJT): Structure and Operation, Dynamic Behavior of BJTs, Basic BiCMOS Circuits: Static Behavior, Switching Delay in BiCMOS Logic Circuits, BiCMOS Applications.	**L1,L2, L3**
Module -5	
Chip Input and Output (I/O) Circuits: Introduction, ESD Protection, Input Circuits, Output Circuits and L(di/dt) Noise, On-Chip Clock Generation and Distribution, Latch-Up and Its Prevention. **Design for Manufacturability:** Introduction, Process Variations, Basic Concepts and Definitions, Design of Experiments and Performance Modeling.	**L2, L3**

Course outcomes: After studying this course, students will be able to:

1. Analyse issues of On-chip interconnect Modelling and Interconnect delay calculation.
2. Analyse the Switching Characteristics in Digital Integrated Circuits.
3. Use the Dynamic Logic circuits in state-of-the-art VLSI chips.
4. Study critical issues such as ESD protection, Clock distribution, Clock buffering, and Latch phenomenon
5. Use Bipolar and Bi-CMOS circuits in very high speed design.

Question Paper Pattern

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Book:

- Sung Mo Kang & Yosuf Leblebici, “CMOS Digital Integrated Circuits: Analysis and Design”, Tata McGraw-Hill, Third Edition.

Reference Books:

1. Neil Weste and K. Eshragian, “Principles of CMOS VLSI Design: A System Perspective”, Second Edition, Pearson Education (Asia) Pvt. Ltd. 2000.
2. Wayne, Wolf, “Modern VLSI Design: System on Silicon” Prentice Hall PTR/Pearson Education, Second Edition, 1998.
3. Douglas A Pucknell & Kamran Eshragian, “Basic VLSI Design” PHI 3rd Edition (original Edition – 1994).

VLSI & ES Lab-1
[As per Choice Based Credit System (CBCS) scheme]
SEMESTER – I

Laboratory Code	**18EVEL16**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**03**	**SEE marks**	**60**
Total Number of Lecture Hours	**01Hr Tutorial (Instructions)+ 03 Hours Laboratory**	**Exam Hours**	**03**
CREDITS – 02			

Course objectives: This laboratory course enables students to:

- Learn Verilog Code Programming for the design of digital circuits
- Use FPGA/CPLD board and Logic Analyzer or Chipscope to verify the results.
- Learn physical design for the digital circuits
- Learn Assembly language programming for different applications using ARM- Cortex M3 Kit and Keil uVision- 4 tool.
- Learn C language programming for different applications using ARM-Cortex M3 Kit and Keil uVision-4 tool.

Experiments	**RBT Level**
Part – A: VLSI Digital Design Experiments to be done using 1. CADENCE/SYNOPSIS/MENTOR GRAPHICS/TANNER or any other equivalent Tool 2. FPGA/CPLD Boards with Xilinx or any other equivalent	

ASIC-Digital Design Flow I. Write Verilog Code for the following circuits and their Test Bench for verification, observe the wave technological library (constraints to be given). Do the initial timing verification with gate level simulation. 1. An inverter, Buffer, Transmission gate and basic gates 2. Flip flop - RS, D, JK, MS, T 3. 4-bit counter [Synchronous & Asynchronous counter] **Note: For the set of experiments listed above, students can make the following flow as a study:** - Core Constrained flow - Creation of I/O pad frame - Use the created I/O pad frame for Pad constrained design. - CTS flow Only for designs which have clock **FPGA DIGITAL DESIGN** ***VLSI Front End Design programs:*** Programming can be done using any compiler. Down load the programs on FPGA/CPLD boards and use pattern generator (32 channels and logic analyzer)/Chipscope pro apart from verification by simulation 1. Write Verilog code for the design of 8-bit i. Carry Ripple Adder ii. Carry Look Ahead adder iii. Carry Skip Adder 2. Write Verilog Code for 8-bit i. Array Multiplication (Signed and Unsigned) ii. Booth Multiplication (Radix-4) 3. Write Verilog code for 4/8-bit i. Magnitude Comparator ii. LFSR iii. Parity Generator iv. Universal Shift Register 4. Design a Mealy and Moore Sequence Detector using Verilog to detect Sequence. Eg 11101 (with and without overlap) any sequence can be specified.	L3

Part – B: Experiments to be done using ARM Cortex M3	L1, L2, L3
ARM Cortex M3 Programs - Programming to be done using Keil uVision 4 and download the program on to a M3 evaluation board such as NXP LPC1768 or ATMEL ARM a) Write an Assembly language program to calculate the sum and display the result for the addition of first ten numbers. SUM = 10+9+8+.....+1 b) Write an Assembly language program to store data in RAM c) Write a C program to output the "Hello World" message using UART d) Write a C program to operate a buzzer using Cortex M3 e) Write a C program to display the temperature sensed using Cortex M3. f) Write a C program to control stepper motor using Cortex M3.	

Course outcomes: This laboratory course enable the students to:

1. Understand the features of CAD tool in VLSI design.
2. Design and verify the behavior of digital circuits using digital flow
3. Verify the design using a logic analyzer
4. Analyse physical design
5. Develop Assembly language programs for different applications using ARM- Cortex M3 Kit and Keil uVision-4 tool.
6. Develop C language programs for different applications using ARM-Cortex M3 Kit and Keil uVision-4 tool.

Conduct of Practical Examination:

- All laboratory experiments are to be included for practical examination.
- For examination, one experiment from Part-A and One experiment from Part-B is to be set.
- Students are allowed to pick one experiment from the lot.
- Strictly follow the instructions as printed on the cover page of answer script for breakup of marks.
- Change of experiment is allowed only once and Marks allotted to the Procedure part to be made zero.

RESEARCH METHODOLOGY AND IPR

[As per Choice Based Credit System (CBCS) scheme]

SEMESTER –I

Course Code	18RMI17	CIE Marks	40
Number of Lecture Hours/Week	02	Exam Hours	03
Total Number of Lecture Hours	25	SEE Marks	60

Credits - 02

Course objectives:

- To give an overview of the research methodology and explain the technique of defining a research problem
- To explain the functions of the literature review in research.
- To explain carrying out a literature search, its review, developing theoretical and conceptual frameworks and writing a review.
- To explain various research designs and their characteristics.
- To explain the details of sampling designs, and also different methods of data collections.
- To explain the art of interpretation and the art of writing research reports.
- To explain various forms of the intellectual property, its relevance and business impact in the changing global business environment.
- To discuss leading International Instruments concerning Intellectual Property Rights.■

Module-1	**Teaching Hours/ RBT Level**
Research Methodology: Introduction, Meaning of Research, Objectives of Research, Motivation in Research, Types of Research, Research Approaches, Significance of Research, Research Methods versus Methodology, Research and Scientific Method, Importance of Knowing How Research is Done, Research Process, Criteria of Good Research, and Problems Encountered by Researchers in India. ■	**05** **L1, L2**
Module-2	
Defining the Research Problem: Research Problem, Selecting the Problem, Necessity of Defining the Problem, Technique Involved in Defining a Problem, An Illustration. **Reviewing the literature:** Place of the literature review in research, Bringing clarity and focus to your research problem, Improving research methodology, Broadening knowledge base in research area, Enabling contextual findings, How to review the literature, searching the existing literature, reviewing the selected literature, Developing a theoretical framework, Developing a conceptual framework, Writing about the literature reviewed. ■	**05** **L1, L2**
Module-3	

Research Design: Meaning of Research Design, Need for Research Design, Features of a Good Design, Important Concepts Relating to Research Design, Different Research Designs, Basic Principles of Experimental Designs, Important Experimental Designs. **Design of Sample Surveys:** Introduction, Sample Design, Sampling and Non-sampling Errors, Sample Survey versus Census Survey, Types of Sampling Designs. ■	**05** **L1, L2**
Module-4	
Data Collection: Experimental and Surveys, Collection of Primary Data, Collection of Secondary Data, Selection of Appropriate Method for Data Collection, Case Study Method. **Interpretation and Report Writing:** Meaning of Interpretation, Technique of Interpretation, Precaution in Interpretation, Significance of Report Writing, Different Steps in Writing Report, Layout. **Interpretation and Report Writing (continued):** of the Research Report, Types of Reports, Oral Presentation, Mechanics of Writing a Research Report, Precautions for Writing Research Reports. ■	**05** **L1, L2, L3, L4**
Module-5	
Intellectual Property: The Concept, Intellectual Property System in India, Development of TRIPS Complied Regime in India, Patents Act, 1970, Trade Mark Act, 1999,The Designs Act, 2000, The Geographical Indications of Goods (Registration and Protection) Act1999, Copyright Act,1957,The Protection of Plant Varieties and Farmers' Rights Act, 2001,The Semi-Conductor Integrated Circuits Layout Design Act, 2000, Trade Secrets, Utility Models, IPR and Biodiversity, The Convention on Biological Diversity (CBD) 1992, Competing Rationales for Protection of IPRs, Leading International Instruments Concerning IPR, World Intellectual Property Organisation (WIPO),WIPO and WTO, Paris Convention for the Protection of Industrial Property, National Treatment, Right of Priority, Common Rules, Patents, Marks, Industrial Designs, Trade Names, Indications of Source, Unfair Competition, Patent Cooperation Treaty (PCT), Advantages of PCT Filing, Berne Convention for the Protection of Literary and Artistic Works, Basic Principles, Duration of Protection, Trade Related Aspects of Intellectual Property Rights(TRIPS) Agreement, Covered under TRIPS Agreement, Features of the Agreement, Protection of Intellectual Property under TRIPS, Copyright and Related Rights, Trademarks, Geographical indications, Industrial Designs, Patents, Patentable Subject Matter, Rights Conferred, Exceptions, Term of protection, Conditions on Patent Applicants, Process Patents, Other Use without Authorization of the Right Holder, Layout-Designs of Integrated Circuits, Protection of Undisclosed Information, Enforcement of Intellectual Property Rights, UNSECO.■	**05** **L1, L2, L3, L4**

Course outcomes:

At the end of the course the student will be able to:

- Discuss research methodology and the technique of defining a research problem
- Explain the functions of the literature review in research, carrying out a literature search, developing theoretical and conceptual frameworks and writing a review.
- Explain various research designs and their characteristics.
- Explain the art of interpretation and the art of writing research reports
- Discuss various forms of the intellectual property, its relevance and business impact in the changing global business environment and leading International Instruments concerning IPR.■

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

M.Tech-VLSI & ES-2018-SECOND SEMESTER SYLLABUS

DESIGN OF ANALOG AND MIXED MODE VLSI CIRCUITS [**As per Choice Based credit System (CBCS) Scheme** **SEMESTER – II**			
Subject Code	**18EVE21**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**04**	**SEE marks**	**60**
Total Number of Lecture Hours	**50 (10 Hours per Module)**	**Exam Hours**	**03**
CREDITS – 04			

Course Objectives: This course will enable students to:

- Describe basic physics and operation of MOS devices.
- Exemplify single-stage and differential amplifiers and current mirrors
- Describe operational amplifiers
- Learn the design of phase-locked-loops
- Know the role of Data converters in an ever-increasing digital world.

Modules	**RBT Level**
Module 1	
Basic MOS Device Physics: General considerations, MOS I/V Characteristics, second order effects, MOS device models. **Single stage Amplifier:** Basic Concepts, Common Source stage (Text 1)	L1, L2
Module 2	
Single stage Amplifier: Source follower, common-gate stage, Cascode Stage, choice of device models. **Differential Amplifiers:** Single ended and differential operation, Basic differential pair, Common mode response, Differential pair with MOS loads, Gilbert cell (Text 1)	L1,L2
Module 3	
Passive and Active Current Mirrors: Basic current mirrors, Cascode Current mirrors, Active Current mirrors. **Operational Amplifiers (part-1):** General Considerations**,** One Stage OP-Amp, Two Stage OP-Amp, Gain boosting (Text 1)	L1,L2,L3
Module 4	
Operational Amplifiers (part-2): Common Mode Feedback, Slew rate, Power Supply Rejection. **Phase Locked Loops:** Simple PLL, Charge pump PLLs, Non-ideal effects in PLLs, Delay-Locked Loops, Applications (Text 1)	L1,L2,L3
Module 5	
Data Converter Architectures: DAC & ADC Specifications, Current Steering DAC, Charge Scaling DAC, Cyclic DAC, Pipeline DAC, Flash ADC, Pipeline ADC, Integrating ADC, Successive Approximation ADC (Text 2)	L1,L2,L3

Course Outcomes: After studying this course, students will be able to:

1. Use efficient analytical tools for quantifying the behaviour of basic circuits by inspection.
2. Design high-performance, stable operational amplifiers with the trade-offs between speed, precision and power dissipation.
3. Design and study the behaviour of phase-locked-loops for the applications.
4. Identify the critical parameters that affect the analog and mixed-signal VLSI circuits' performance
5. Perform calculations in the digital or discrete time domain, more sophisticated data converters to translate the digital data to and from inherently analog world.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Books:

1. Behzad Razavi, "Design of Analog CMOS Integrated Circuits", TMH, 2007.
2. R. Jacob Baker, "CMOS Circuit Design, Layout, and Simulation", Second Edition, Wiley.

Reference Book:

- Phillip E. Allen, Douglas R. Holberg, "CMOS Analog Circuit Design", Second Edition, Oxford University Press.

REAL TIME OPERATING SYSTEM [As per Choice Based credit System (CBCS) Scheme SEMESTER – II			
Subject Code	**18EVE22**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**04**	**SEE marks**	**60**
Total Number of Lecture Hours	**50 (10 Hours per Module)**	**Exam Hours**	**03**
CREDITS – 04			

Course Objectives: This course will enable the students to:

- Introduce the fundamental concepts of Real Time Operating Systems and the real time embedded system
- Apply concepts relating to operating systems such as Scheduling techniques, Thread Safe Reentrant Functions, Dynamic priority policies.
- Describe concepts related to Multi resource services like blocking, Deadlock, live lock & soft real-time services.
- Discuss Memory management concepts, Embedded system components, Debugging components and file system components.
- Study programs for multithreaded applications using suitable data structures.

Modules	RBT Level
Module 1	
Real-Time Systems and Resources: Brief history of Real Time Systems, A brief history of Embedded Systems. System Resources, Resource Analysis, Real-Time Service Utility, Scheduler concepts, Real-Time OS, State transition diagram and tables, Thread Safe Reentrant Functions. (Text 1: Selected sections from Chap. 1, 2)	L1,L2,L3
Module 2	
Processing with Real Time Scheduling: Scheduler Concepts, Preemptive Fixed Priority Scheduling Policies with timing diagrams and problems and issues, Feasibility, Rate Monotonic least upper bound, Necessary and Sufficient feasibility, Deadline –Monotonic Policy, Dynamic priority policies, Alternative to RM policy. (Text 1: Chap. 2,3,7)	L1,L2,L3
Module 3	
Memory and I/O: Worst case execution time, Intermediate I/O, Shared Memory, ECC Memory, Flash file systems. Multi-resource Services, Blocking, Deadlock and live lock, Critical sections to protect shared resources, Missed deadline, QoS, Reliability and Availability, Similarities and differences, Reliable software, Available software. (Text 1: Selected topics from Chap. 4,5,6,7,11)	L1,L2,L3
Module 4	
Firmware Components: The 3 firmware components, RTOS system software mechanisms, Software application components. Debugging Components, Exceptions, assert, Checking return codes, Single-step debugging, Test access ports, Trace Ports. (Text 1: Selected topics	L1,L2,L3

from Chap. 8,9)	
Module 5	
Process and Threads: Process and thread creations, Programs related to semaphores, message queue, shared buffer applications involving inter task/thread communication (Text 2: Chap. 11)	L1,L2,L3

Course Outcomes: After studying this course, students will be able to:

1. Develop programs for real time services, firmware and RTOS, using the fundamentals of Real Time Embedded System, real time service utilities, debugging methodologies and optimization techniques.
2. Select the appropriate system resources (CPU, I/O, Memory, Cache, ECC Memory, Microcontroller/FPGA/ASIC to improve the system performance.
3. Apply priority based static and dynamic real time scheduling techniques for the given specifications.
4. Analyze deadlock conditions, shared memory problem, critical section problem, missed deadlines, availability, reliability and QoS.
5. Develop programs for multithreaded applications using suitable techniques and data structure

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Books:

1. Sam Siewert, "Real-Time Embedded Systems and Components", Cengage Learning India Edition, 2007.
2. Dr. K.V.K.K Prasad, Embedded/Real Time Systems, Concepts, Design and Programming, Black Book, Dream Tech Press, New edition, 2010.

Reference Books:

1. James W S Liu, "Real Time System", Pearson education, 2008.
2. Dream Tech Software Team, "Programming for Embedded Systems", John Wiley, India Pvt. Ltd., 2008.

SYSTEM VERILOG
[As per Choice Based credit System (CBCS) Scheme]
SEMESTER – II

Subject Code	**18EVE23**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**04**	**SEE marks**	**60**
Total Number of Lecture Hours	**50 (10 Hours per Module)**	**Exam Hours**	**03**

CREDITS – 04

Course Objectives: This course will enable students to:

- Understand digital system verification using object oriented methods
- Learn the System Verilog language for digital system verification.
- Create/build test benches for the basic design/methodology.
- Use constrained random tests for verification
- Understand concepts of functional coverage

Modules	**RBT Level**
Module 1	
Verification Guidelines: The verification process, basic test bench functionality, directed testing, methodology basics, constrained random stimulus, randomization, functional coverage, test bench components, layered testbench. **Data Types:** Built in Data types, fixed and dynamic arrays, Queues, associative arrays, linked lists, array methods, choosing a storage type, creating new types with type def, creating user defined structures, type conversion, Enumerated types, constants and strings, Expression width.	L1, L2
Module 2	
Procedural Statements and Routines: Procedural statements, Tasks, Functions and void functions, Task and function overview, Routine arguments, returning from a routine, Local data storage, time values. **Converting the test bench and design:** Separating the test bench and design, The interface construct, Stimulus timing, Interface driving and sampling, System Verilog assertions.	L1,L2,L3
Module 3	
Randomization: Introduction, Randomization in System Verilog, Constraint details, Solution probabilities, Valid constraints, In-line constraints, Random number functions, Common randomization problems, Iterative and array constraints, Random control, Random Number Generators.	L1,L2,L3
Module 4	
Threads and Interprocess Communication: Working with threads, Disabling threads, Interprocess communication, Events, semaphores, Mailboxes, Building a test bench with threads and Interprocess Communication.	L1,L2,L3

Module 5	
Functional Coverage: Coverage types, Coverage strategies, Simple coverage example, Anatomy of Cover group and Triggering a Cover group, Data sampling, Cross coverage, Generic Cover groups, Coverage options, Analyzing coverage data, measuring coverage statistics during simulation.	L1,L2,L3

Course Outcomes: After studying this course, students will be able to:

1. Write test benches for moderately complex digital circuits
2. Use System Verilog language
3. Appreciate functional coverage
4. Apply constrained random tests benches using System Verilog
5. Analyze a verification case and apply System Verilog to verify the design

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Book:

- Chris Spear, 'System Verilog for Verification – A guide to learning the Test bench language features', Springer Publications, 2nd Edition, 2010.

Reference Book:

- Stuart Sutherland, Simon Davidmann, Peter Flake, "System Verilog for Design-A guide to using system verilog for Hardware design and modeling", Springer Pulications, 2nd Edition, 2006.
- Stuart Sutherland, Simon Davidmann, Peter Flake, System Verilog for Design Second Edition: A Guide to Using System Verilog for Hardware Design and Modeling, Springer Science & Business Media, 15-Sep-2006

ADVANCES IN VLSI DESIGN
[As per Choice Based credit System (CBCS) Scheme]
SEMESTER – II

Subject Code	**18EVE241**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**04**	**SEE marks**	**60**
Total Number of Lecture Hours	**50 (10 Hours per Module)**	**Exam Hours**	**03**

CREDITS – 04

Course Objectives: This course will enable students to:

- Learn circuit-oriented approach towards digital design
- Illustrate the impact of interconnect wiring on the functionality and performance of a digital gate.
- Infer different approaches to digital timing and clocking circuits
- Understand the impact of clock skew on the behaviour of digital synchronous circuits.
- Explain the role of peripheral circuitry such as the decoders, sense amplifiers, drivers and control circuitry in the design of reliable and fast memories .

Modules	**RBT Level**
Module 1	
Implementation Strategies For Digital ICS: Introduction, From Custom to Semicustom and Structured Array Design Approaches, Custom Circuit Design, Cell-Based Design Methodology, Standard Cell, Compiled Cells, Macrocells, Megacells and Intellectual Property, Semi-Custom Design Flow, Array-Based Implementation Approaches, Pre-diffused (or Mask-Programmable) Arrays, Pre-wired Arrays, Perspective-The Implementation Platform of the Future.	L1,L2,L3
Module 2	
Coping With Interconnect: Introduction, Capacitive Parasitics, Capacitance and Reliability-Cross Talk, Capacitance and Performance in CMOS, Resistive Parasitics, Resistance and Reliability-Ohmic Voltage Drop, Electromigration, Resistance and Performance-RC Delay, Inductive Parasitics, Inductance and Reliability-Voltage Drop, Inductance and Performance-Transmission Line Effects, Advanced Interconnect Techniques, Reduced-Swing Circuits, Current-Mode Transmission Techniques, Perspective: Networks-on-a-Chip.	L1,L2,L3
Module 3	
Timing Issues In Digital Circuits: Introduction, Timing Classification of Digital Systems, Synchronous Interconnect, Mesochronous interconnect, Plesiochronous Interconnect, Asynchronous Interconnect, Synchronous Design — An In-depth Perspective, Synchronous Timing Basics, Sources of Skew and Jitter, Clock-Distribution Techniques, Latch-Base Technique,	L1,L2,L3

Completion-Signal Generation, Self-Timed Signaling, Practical Examples of Self-Timed Logic, Synchronizers and Arbiters, Synchronizers-Concept and Implementation, Arbiters, Clock Synthesis and Synchronization Using a Phase-Locked Loop, Basic Concept, Building Blocks of a PLL. d Clocking, Self Timed Circuit Design, Self-Timed Logic - An Asynchronous	
Module 4	
Design of testable sequential circuits: Controllability and observability, Ad-Hoc design rules for improving testability, design of diagnosable sequential circuits, the scan-path technique for testable sequential circuit design, Level Sensitive Scan Design(LSSD), Random Access Scan Technique, Partial scan, testable sequential circuit design using Nonscan Techniques, Cross check, Boundary Scan. (Text 1)	L1,L2,L3
Module 5	
Designing Memory and Array Structures: Memory Reliability and Yield, Signal-to-Noise Ratio, Memory yield, Power Dissipation in Memories, Sources of Power Dissipation in Memories, Partitioning of the memory, Addressing the Active Power Dissipation, Dataretention dissipation, Case Studies in Memory Design: The Programmable Logic Array (PLA), A 4 Mbit SRAM, A 1 Gbit NAND Flash Memory, Perspective: Semiconductor Memory Trends and Evolutions.	L1,L2,L3

Course Outcomes: After studying this course, students will be able to:

1. Apply design automation for complex circuits using the different implementation methodology like custom versus semi-custom, hardwired versus fixed, regular array versus ad-hoc.
2. Use the approaches to minimize the impact of interconnect parasitics on performance, power dissipation and circuit reliability
3. Impose the ordering of the switching events to meet the desired timing constraints using synchronous, clocked approach.
4. Infer the reliability of the memory

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Books:

- Jan M Rabey, Anantha Chandrakasan, Borivoje Nikolic, ―Digital Integrated Circuits-A Design Perspective‖, PHI, 2nd Edition.

Reference Books:

1. M. Smith, —Application Specific Integrated circuits‖, Addison Wesley, 1997 Wang, Wu and Wen, "VLSI Test Principles and Architectures", Morgan Kaufmann, 2006.
2. H. Veendrick, —MOS IC's: From Basics to ASICs, Wiley-VCH, 1992.

NANOELECTRONICS
[As per Choice Based Credit System (CBCS) scheme] SEMESTER – II

Subject Code	18EVE242	CIE	40
Number of Lecture Hours/Week	04	SEE Marks	60
Total Number of Lecture Hours	50 (10 Hours per Module)	Exam Hours	03

CREDITS – 04

Course objectives: This course will enable students to:

- Enhance basic engineering science and technological knowledge of nanoelectronics .
- Explain basics of top-down and bottom-up fabrication process, devices and systems.
- Describe technologies involved in modern day electronic devices.
- Appreciate the complexities in scaling down the electronic devices in the future.

Modules	(RBT) Level
Module -1	
Introduction: Overview of nanoscience and engineering. Development milestones in microfabrication and electronic industry. Moores' law and continued miniaturization, Classification of Nanostructures, Electronic properties of atoms and solids: Isolated atom, Bonding between atoms, Giant molecular solids, Free electron models and energy bands, crystalline solids, Periodicity of crystal lattices, Electronic conduction, effects of nanometer length scale, Fabrication methods: Top down processes, Bottom up processes methods for templating the growth of nanomaterials, ordering of nanosystems (Text 1).	**L1, L2**
Module -2	
Characterization: Classification, Microscopic techniques, Field ion microscopy, scanning probe techniques, diffraction techniques: bulk and surface diffraction techniques, spectroscopy techniques: photon, radiofrequency, electron, surface analysis and dept profiling: electron, mass, Ion beam, Reflectrometry, Techniques for property measurement: mechanical, electron, magnetic, thermal properties(Text1)	**L1,L2,L 3**
Module -3	
Inorganic semiconductor nanostructures: overview of semiconductor physics. Quantum confinement in semiconductor nanostructures: quantum wells, quantum wires, quantum dots, super-lattices, band offsets, electronic density of states (Text1). **Carbon Nanostructures:** Carbon molecules, Carbon Clusters, Carbon Nanotubes, application of Carbon Nanotubes (Text 2).	**L1, L2, L3**
Module -4	

Fabrication techniques: requirements of ideal semiconductor, epitaxial growth of quantum wells, lithography and etching, cleaved-edge over growth, growth of vicinal substrates, strain induced dots and wires, electrostatically induced dots and wires, Quantum well width fluctuations, thermally annealed quantum wells, semiconductor nanocrystals, collidal quantum dots, self-assembly techniques. **Physical processes:** modulation doping, quantum hall effect, resonant tunneling, charging effects, ballistic carrier transport, Inter band absorption, intra band absorption, Light emission processes, phonon bottleneck, quantum confined stark effect, nonlinear effects, coherence and dephasing, characterization of semiconductor nanostructures: optical electrical and structural (Text1).	**L1, L2, L3**
Module -5	
Methods of measuring properties: atomic, crystollography, microscopy, spectroscopy (Text 2). **Applications**: Injection lasers, quantum cascade lasers, single-photon sources, biological tagging, optical memories, coulomb blockade devices, photonic structures, QWIP's, NEMS, MEMS (Text1).	**L1, L2, L3**

Course outcomes: After studying this course, students will be able to:

1. Know the principles behind Nanoscience engineering and Nanoelectronics.
2. Apply the knowledge to prepare and characterize nanomaterials.
3. Know the effect of particles size on mechanical, thermal, optical and electrical properties of nanomaterials.
4. Design the process flow required to fabricate state of the art transistor technology.
5. Analyze the requirements for new materials and device structure in the future tec hnologies.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Books:

1. Ed Robert Kelsall, Ian Hamley, Mark Geoghegan, "Nanoscale Science and Technology", John Wiley, 2007.
2. Charles P Poole, Jr, Frank J Owens, "Introduction to Nanotechnology", John Wiley, Copyright 2006, Reprint 2011.

Reference Book:

Ed William A Goddard III, Donald W Brenner, Sergey E. Lyshevski, Gerald J Iafrate, "Hand Book of Nanoscience Engineering and Technology", CRC press, 2003.

STATIC TIMING ANALYSIS
[As per Choice Based Credit System (CBCS) scheme]
SEMESTER –II

Subject Code	**18EVE 243**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**04**	**SEE Marks**	**60**
Total Number of Lecture Hours	**50 (10 Hours per Module)**	**Exam Hours**	**03**

CREDITS – 04

Course objectives: This course will enable students to:

- Understand timing analyses at various process, environment and interconnect corners.
- Apply the learnt concepts of STA to evaluate the delay of the circuits.
- Understand and analyze the signal integrity issues for the IC.
- Generate the timing analysis report using EDA tool.
- Understand verification and analyze the generated report to identify issues for the violation
- Learn different techniques to meet timing in an IC design.
- Set up the timing analysis environment and perform the timing analysis for various cases.

Modules	**(RBT) Level**
Module -1	
Introduction: Nanometer Designs, What is Static Timing Analysis?. Why Static Timing Analysis?, Crosstalk and Noise, Design Flow, CMOS Digital Designs, FPGA Designs, Asynchronous Designs, STA at Different Design Phases, Limitations of Static Timing Analysis, Power Considerations, Reliability Considerations, **STA Concepts:** CMOS Logic Design, Basic MOS Structure, CMOS Logic Gate, Standard Cells, Modeling of CMOS Cells, Switching Waveform, Propagation Delay, Slew of a Waveform, Skew between Signals, Timing Arcs and Unateness, Min and Max Timing Paths, Clock Domains, Operating Conditions .	**L1-L2**
Module -2	
Standard Cell Library: Pin Capacitance, Timing Modeling, Linear Timing Model, Non-Linear Delay Model, Example of Non-Linear, Delay Model Lookup, Threshold Specifications and Slew Derating Timing Models - Combinational Cells, Delay and Slew Models, Positive or Negative Unate, General Combinational Block, Timing Models - Sequential Cells, Synchronous Checks: Setup and Hold, Example of Setup and Hold Checks, Negative Values in Setup and Hold Checks, Asynchronous Checks, Recovery and Removal Checks Pulse Width Checks, Example of Recovery, Removal and Pulse Width Checks, Propagation Delay, State-Dependent Models XOR, XNOR and Sequential Cells, Interface Timing Model for a Black	**L1**

Box, Advanced Timing Modeling, Receiver Pin Capacitance, Specifying Capacitance at the Pin Level, Specifying Capacitance at the Timing Arc Level, Output Current, Models for Crosstalk Noise Analysis, DC Current, Output Voltage,, Propagated Noise, Noise Models for Two-Stage Cells, Noise Models for Multi-stage and Sequential Cells, Other Noise Models, Power Dissipation Modeling, Active Power, Double Counting Clock Pin Power, Leakage Power, Other Attributes in Cell Library, Area Specification, Function Specification, SDF Condition, Characterization and Operating Conditions, What is the Process Variable, Derating using K-factors, Library Units.	
Module -3	
Interconnect Parasitics: RLC for Interconnect, Wireload Models, Interconnect Trees, Specifying Wireload Models, Representation of Extracted Parasitics, Detailed Standard Parasitic Format, Reduced Standard Parasitic Format, Standard Parasitic Exchange Format, Representing Coupling Capacitances, Hierarchical Methodology, Block Replicated in Layout, Reducing Parasitics for Critical Nets, Reducing Interconnect Resistance, Increasing Wire Spacing, Parasitics for Correlated Nets. **Delay Calculation**: Overview, Delay Calculation Basics, Delay Calculation with Interconnect, Pre-layout Timing, Post-layout Timing, Cell Delay using Effective Capacitance, Interconnect Delay, Elmore Delay, Higher Order Interconnect Delay Estimation, Full Chip Delay Calculation, Slew Merging, Different Slew Thresholds, Different Voltage Domains, Path Delay Calculation, Combinational Path Delay, Path to a Flip-flop, Input to Flip-flop Path, Flip-flop to Flip-flop Path, Multiple Paths, Slack Calculation.	**L1-L4**
Module -4	
Configuring the STA Environment: What is the STA Environment? Specifying Clocks, Clock Uncertainty, Clock Latency, Generated Clocks, Example of Master Clock at Clock Gating Cell Output, Generated Clock using Edge and Edge_shift Options, Generated Clock using Invert Option, Clock Latency for Generated Clocks, Typical Clock Generation Scenario, Constraining Input Paths, Constraining Output Paths, Example A, Example B, Example C, Timing Path Groups, Modeling of External Attributes, Modeling Drive Strengths, Modeling Capacitive Load, Design Rule Checks, Virtual Clocks, Refining the Timing Analysis, Specifying Inactive Signals, Breaking Timing Arcs in Cells, Point-to-Point Specification, Path Segmentation.	**L1-L4**
Module -5	
Timing Verification: Setup Timing Check, Flip-flop to Flip-flop Path, Input to Flip-flop Path, Input Path with Actual Clock, Flip-flop to Output Path, Input to Output Path, Frequency Histogram, Hold Timing Check, Flip-flop to Flip-flop Path, Hold Slack Calculation, Input to Flip-flop Path, Flip-flop to Output Path, Flip-flop to Output Path with Actual Clock, Input to Output Path, Multicycle Paths, Crossing Clock Domains, False Paths, Half-	**L1-L4**

Cycle Paths, Removal Timing Check, Recovery Timing Check, Timing across Clock Domains, Slow to Fast Clock Domains, Fast to Slow Clock Domains, Half-cycle Path - Case 1, Half-cycle Path - Case 2, Fast to Slow Clock Domain, Slow to Fast Clock Domain, Multiple Clocks, Integer Multiples, Non-Integer Multiples, Phase Shifted.	

Course outcomes: After studying this course, students will be able to:

- Evaluate the delay of any given digital circuits.
- Prepare the resources to perform the static timing analysis using EDA tool
- Prepare timing constraints for the design based on the specification.
- Generate the timing analysis report using EDA tool for different checks.
- Perform verification and analyse the generated report to identify critical issues and bottleneck for the violation and suggest the techniques to make the design to meet timing

Question paper pattern:

- The students will have to answer 5 full questions, selecting one full question from each module. Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

It is suggested that the students may be asked to conduct the following experiments to award a part of CIE marks which is reserved for the Other Activities:

In the following experiments, determine the parameters such as slack, critical path, Dynamic power, leakage power, timing and area report. Also, generate Verilog netlist, SDF file and write SDC constraints after synthesis based on the particular experiment.

1. Synthesize 4 bit counter & find the required parameters at 50 MHz (Repeat using Xilinx library also).
2. Synthesize 8 bit Mux and find the required parameters at 25 MHz (Repeat using Xilinx library also).
3. Synthesize synchronous 16 bit save carry adder for 100 MHz and find the required parameters.
4. Synthesize synchronous 16 bit save carry adder for 20 MHz and find the required parameters (Repeat the experiment for 3 Vendor library, Altera library).

5. Compare the area report and timing report as per the vendor and tablet using Pi-chart or Bar chart for expt - 4
6. Synthesize 8 bit multiplier using Xilinx Defence standard / Automotive library to determine the required parameters
7. For the given UART/Traffic signal controller, synthesize using 50 MHZ clock and 100 MHZ clock. Compare the result for both the clocks and determine the required parameters.
8. Compare one of the design through ASIC synthesis and FPGA synthesis to determine the required parameters

Text Book:

J. Bhasker, R Chadha,., "Static Timing Analysis for Nanometer Designs: A Practical Approach", Springer, 2009.

Reference Books:

1. Sridhar Gangadharan, Sanjay Churiwala, "Constraining Designs for Synthesis and Timing Analysis – A Practical Guide to Synopsis Design Constraints (SDC)", Springer, 2013.
2. Naresh Maheshwari and Sachin Sapatnekar, "Timing Analysis and Optimization of Sequential Circuits", Springer Science and Business Media, 1999.

LOW POWER VLSI DESIGN [As per Choice Based Credit System (CBCS) scheme] SEMESTER –II			
Subject Code	**18EVE251**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**04**	**SEE Marks**	**60**
Total Number of Lecture Hours	**50 (10 Hours per Module)**	**Exam Hours**	**03**
CREDITS – 04			

Course objectives: This course will enable students to:

- Apply State-of-the art approaches to power estimation and reduction.
- Describe the various power reduction and the power estimation methods.
- Explain power dissipation at all layers of design hierarchy from technology, circuit, logic, architecture and system
- Know the basics and advanced techniques in low power design which is a hot topic in today's market where the power plays a major role.
- Practice the low power techniques using current generation design style and process technology.

Modules	(RBT) Level
Module -1	
Introduction: Need for low power VLSI chips, charging and discharging capacitance, short circuit current in CMOS leakage current, static current, basic principles of low power design, low power figure of merits. **Simulation power analysis:** SPICE circuit simulation, discrete transistor modeling and analysis, gate level logic simulation, architecture level analysis, data correlation analysis in DSP systems, Monte Carlo simulation. (Text 1)	**L1, L2**
Module -2	
Probabilistic power analysis: Random logic signals, probability & frequency, probabilistic power analysis techniques, signal entropy. **Circuit:** Transistor and gate sizing, equivalent pin ordering, network restructuring and reorganization, special latches and flip flops, low power digital cell library, adjustable device threshold voltage. (Text 1)	**L1, L2, L3**
Module -3	
Logic: Gate reorganization, signal gating, logic encoding, state machine encoding, pre-computation logic (Text 1). **Low power Clock Distribution:** Power dissipation in clock distribution, single driver Vs distributed buffers, Zero skew Vs tolerable skew, chip & package co design of clock network (Text 2).	**L1, L2, L3**
Module -4	

Low power Architecture & Systems: Power & performance management, switching activity reduction, parallel architecture with voltage reduction, flow graph transformation (Text 1). **Low power arithmetic components:** Introduction, circuit design style, adders, multipliers, division (Text 2).	**L1- L4**
Module -5	
Low power memory design: Introduction, sources and reductions of power dissipation in memory subsystem, sources of power dissipation in DRAM and SRAM (Text 2). **Algorithm & Architectural Level Methodologies**: Introduction, design flow, Algorithmic level analysis & optimization, Architectural level estimation & synthesis (Text 2). **Advanced Techniques**: Adiabatic computation, pass transistor, Asynchronous circuits (Text 1).	**L1-L4**

Course outcomes: After studying this course, students will be able to:

1. Identify the sources of power dissipation in CMOS circuits.
2. Perform power analysis using simulation based approaches and probabilistic analysis.
3. Use optimization and trade-off techniques that involve power dissipation of digital circuits.
4. Make the power design a reality by making power dimension an integral part of the desigUse practical low power design techniques and their analysis at various levels of design abstraction and analyse how these are being captured in the latest design automation environments. n process
5. Use practical low power design techniques and their analysis at various levels of design abstraction and analyse how these are being captured in the latest design automation environments.
6. Use practical low power design techniques and their analysis at various levels of design abstraction and analyse how these are being captured in the latest design automation environments.

Question paper pattern:

- The students will have to answer 5 full questions, selecting one full question from each module. Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Books:

1. Gary K. Yeap, “Practical Low Power Digital VLSI Design”, Kluwer Academic, 1998.
2. Jan M.Rabaey, Massoud Pedram, “Low Power Design Methodologies”, Kluwer Academic, 2010.

Reference Books:

1. Kaushik Roy, Sharat Prasad, “Low-Power CMOS VLSI Circuit Design” Wiley, 2000
2. A.P.Chandrasekaran and R.W.Broadersen, “Low power digital CMOS design”, Kluwer Academic,1995.
3. A Bellamour and M I Elmasri, “Low power VLSI CMOS circuit design”, Kluwer Academic,1995.

SoC DESIGN [As per Choice Based credit System (CBCS) Scheme SEMESTER – II			
Subject Code	**18EVE252**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**04**	**SEE marks**	**60**
Total Number of Lecture Hours	**50 (10 Hours per Module)**	**Exam Hours**	**03**

CREDITS – 04

Course Objectives: This course will enable students to:

- Describe the ARM processor architecture and user-level assembly language programming
- Appreciate what a high-level language (in this case, C) really needs and how those needs are met by the ARM instruction set.
- raises the issues involved in debugging systems which use embedded
- processor cores and in the production testing of board-level systems.
- Learn the concept of memory hierarchy, discussing the principles
- of memory management and caches.

Modules	RBT Level
Module 1	
ARM Organization and Implementation:3-stage pipeline ARM organization, 5-stage pipeline ARM organization, ARM instruction execution, ARM implementation, The ARM coprocessor interface. **The ARM Instruction Set :**Introduction, Exceptions, Conditional execution, Branch and Branch with Link (B, BL),Branch, Branch with Link and eXchange (BX, BLX),Software Interrupt (SWI),Data processing instructions, Multiply instructions, Count leading zeros (CLZ - architecture v5T only), Single word and unsigned byte data transfer instruction, Half-word and signed byte data transfer instructions,Multiple register transfer instructions, Swap memory and register instructions (SWP), Status register to general register transfer instructions, General register to status register transfer instructions, Coprocessor instructions, Coprocessor data operations, Coprocessor data transfers, Coprocessor register transfers, Breakpoint instruction (BRK - architecture v5T only), Unused instruction space, Memory faults, ARM architecture variants.	L1,L2
Module 2	
Architectural Support for High-Level Languages: Abstraction in software design, Data types, Floating-point data types, The ARM floating-point architecture, Expressions, Conditional statements, Loops, Functions and procedures, Use of memory, Run-time environment. **Architectural Support for System Development:** The ARM memory interface, The Advanced Microcontroller Bus Architecture (AMBA), The ARM reference peripheral specification, Hardware	L1,L2

system prototyping tools, The ARMulator, The JTAG boundary scan test architecture, The ARM debug architecture, Embedded Trace, Signal processing support.	
Module 3	
ARM Processor Cores: ARM7TDMI, ARM8,ARM9TDMI, ARM10TDMI,Discussion,Example and exercises. **Memory Hierarchy:** Memory size and speed, On-chip memory, Caches, Cache design - an example, Memory management, Examples and exercises.	L1,L2
Module 4	
Architectural Support for Operating Systems: An introduction to operating systems, The ARM system control coprocessor, CP15 protection unit registers, ARM protection unit,CP15 MMU registers, ARM MMU architecture, Synchronization, Context switching, Input/ Output, Example and exercises. **ARM CPU Cores:** The ARM710T, ARM720T and ARM740T, The ARM810, The Strong ARM SA-110, The ARM920T and ARM940T, The ARM946E-S and ARM966E-S, The ARM1020E, Discussion, Example and exercises.	L1,L2
Module 5	
Embedded ARM Applications: The VLSI Ruby II Advanced Communication Processor, The VLSI ISDN Subscriber Processor, The One C™VWS22100 GSM chip, The Ericsson-VLSI Bluetooth Baseband Controller, The ARM7500 and ARM7500FE, The ARM7100 364, The SA-1100 368, Examples and exercises. **The AMULET Asynchronous ARM Processors:** Self-timed design 375, AMULET1 377, AMULET2 381, AMULET2e 384,AMULET3 387, The DRACO telecommunications controller 390, A self-timed future? 396, Example and exercises.	L1,L2,L3

Course Outcomes: After studying this course, students will be able to:

1. Apply the 3- and 5-stage pipeline ARM processor cores and analyse the implementation issues.
2. Use the concepts and methodologies employed in designing a System-on-chip (SoC) based around a microprocessor core and in designing the microprocessor core itself.
3. Understand how SoCs and microprocessors are designed and used, and why a modern processor is designed the way that it is.
4. Use integrated ARM CPU cores (including StrongARM) that incorporate full support for memory management.
5. Analyze the requirements of a modern operating system and use the ARM architecture to address the same.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Book:

- Steve Furber, “ARM System-On-Chip Architecture”, Addison Wesley, 2nd edition.

References Books:

1. Joseph Yiu, “The Definitive Guide to the ARM Cortex-M3”, 2nd edn, Newnes, (Elsevier), 2010.
2. Sudeep Pasricha and Nikil Dutt, "On-Chip Communication Architectures: System on Chip Interconnect”, Morgan Kaufmann, Publishers © 2008.
3. Michael Keating, Pierre Bricaud, “Reuse Methodology Manual for System on Chip designs”, Kluwer Accademic Publishers, 2nd edition, 2008.

MICRO ELECTRO MECHANICAL SYSTEMS [As per Choice Based credit System (CBCS) Scheme SEMESTER – II			
Subject Code	**18ELD253**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**04**	**SEE Marks**	**60**
Total Number of Lecture Hours	**50 (10 Hours per Module)**	**Exam Hours**	**03**
CREDITS – 04			

Course Objectives: This course will enable students to:

- Know an overview of microsystems, their fabrication and application areas.
- Teach working principles of several MEMS devices.
- Develop mathematical and analytical models of MEMS devices
- Know methods to fabricate MEMS devices
- Expose the students to various application areas where MEMS devices can be used.

Modules	RBT Level
Module 1	
Overview of MEMS and Microsystems: MEMS and Microsystem, Typical MEMS and Microsystems Products, Evolution of Microfabrication, Microsystems and Microelectronics, Multidisciplinary Nature of Microsystems, Miniaturization. Applications and Markets.	L1, L2
Module 2	
Working Principles of Microsystems: Introduction, Microsensors, Microactuation, MEMS with Microactuators, Microaccelerometers, Microfluidics. **Engineering Science for Microsystems Design and Fabrication:** Introduction, Atomic Structure of Matters, Ions and Ionization, Molecular Theory of Matter and Inter-molecular Forces, Doping of Semiconductors, The Diffusion Process, Plasma Physics, Electrochemistry.	L1, L2
Module 3	
Engineering Mechanics for Microsystems Design: Introduction, Static Bending of Thin Plates, Mechanical Vibration, Thermomechanics, Fracture Mechanics, Thin Film Mechanics, Overview on Finite Element Stress Analysis.	L1,L2,L3
Module 4	
Scaling Laws in Miniaturization: Introduction, Scaling in Geometry, Scaling in Rigid-Body Dynamics, Scaling in Electrostatic Forces, Scaling of	L1,L2,L3

Electromagnetic Forces, Scaling in Electricity, Scaling in Fluid Mechanics, Scaling in Heat Transfer.	
Module 5	
Overview of Micro-manufacturing: Introduction, Bulk Micro-manufacturing, Surface Micromachining, The LIGA Process, Summary on Micro-manufacturing. **Microsystem Design:** Introduction, Design Considerations, Process Design, Mechanical Design, Using Finite Element Method.	L1,L2,L3

Course Outcomes: After studying this course, students will be able to:

1. Understand the technologies related to Micro Electro Mechanical Systems.
2. Describe the design and fabrication processes involved with MEMS devices.
3. Analyse the MEMS devices and develop suitable mathematical models
4. Understand the various application areas for MEMS devices

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Book:

- Tai-Ran Hsu, MEMS and Micro systems: Design, Manufacture and Nanoscale Engineering, 2nd Ed, John Wiley & Sons, 2008. ISBN: 978-0-470-08301-7

Reference Books:

1. Hans H. Gatzen, Volker Saile, JurgLeuthold, Micro and Nano Fabrication: Tools and Processes, Springer, 2015.
2. Dilip Kumar Bhattacharya, Brajesh Kumar Kaushik, Micro electromechanical Systems (MEMS), Cenage Learning.

VLSI & ES Lab-2

[As per Choice Based Credit System (CBCS) scheme]

SEMESTER – II

Laboratory Code	**18EVEL26**	**IA Marks**	**40**
Number of Lecture Hours/Week	**01Hr Tutorial (Instructions) + 03 Hours Laboratory**	**Exam Mark**	**60**
		Exam Hour	**03**

CREDITS – 02

Course objectives: This course will enable students to:

- Learn the CAD tool and the flow of the Full Custom IC design cycle.
- Learn running DRC, LVS and Parasitic Extraction of the various designs.
- Create various components like inverter, differential amplifier and use the same in the design of operational amplifier, R-2R based DAC and ADC.
- Understand the suitability of different techniques of IPC and task switching in a multithreaded application.
- Study and implement different types of data structures required to implement inter task communication.
- Implement Inter task communication using an appropriate data structure.

Experiments	**(RBT) Level**
PART A: VLSI Design. **Experiments to be conducted using suitable CAD tool** 1. Design an **Inverter** with given specifications*, completing the design flow mentioned below: a. Draw the schematic and verify the following i) DC Analysis ii) Transient Analysis b. Draw the Layout and verify the DRC, ERC c. Check for XX d. Extract RC and back annotate the same and verify the Design e. Verify & Optimize for Time, Power and Area to the given constraint***	**L2,L3,L4**

2.Design the following circuits with given specifications*, completing the design flow mentioned below: a. Draw the schematic and verify the following i) DC Analysis ii) AC Analysis iii) Transient Analysis b. Draw the Layout and verify the DRC, ERC, LVS c. Check for XX d. Extract RC and back annotate the same and verify the Design i) Single Stage differential amplifier ii) Common source amplifier iii) Design an op-amp with given specification* using differential amplifier Common source amplifier in library** iv) Design a 4 bit R-2R based DAC for the given specification**	
3. Design an Integrator using OPAMP (First Order)	
4. Design a Differentiator using OPAMP (First Order)	
5. Design and characterize a basic Sigma delta ADC from the available designs.	
PART B: RTOS programs using C language in LINUX OS. 1. Develop programs to (a) create child process and display it's id and (b) Execute child process function using switch structure 2. Develop and test program for a multithreaded application, where communication is through a buffer for the conversion of lowercase text to uppercase text, using semaphore concept. 3. Develop and test program for a multithreaded application, where communication is through shared memory for the conversion of lowercase text to uppercase text. 4. Develop program for inter-thread communication using message queue. Data is to be input from the keyboard for the chosen application 5. Create 'n' number of child threads. Each thread prints the message "I'm in thread number …" and sleeps for 50 ms and then quits. The main thread waits for complete execution of all the child threads and then quits. Compile and execute in Linux. 6. Implement the usage of anonymous pipe with 512 bytes for data sharing between parent and child processes using handle inheritance mechanism	**L1, L2, L3**

Course outcomes: On the completion of this laboratory course, the students will be able to:

- Design, implement and analyse analog, digital and mixed mode circuits
- Learn the various issues in Mixed signal designs basically data converters.
- Acquire hands-on skills of using CAD tools in VLSI design.
- Appreciate the design process in VLSI through a mini-project on the design of a CMOS sub-system.
- Select a suitable task switching technique in a multithreaded application.
- Implement different techniques of message passing and Inter task communication.
- Implement different data structures such as pipes, queues and buffers in multithreaded programming.

Conduct of Practical Examination:

- All laboratory experiments are to be included for practical examination.
- For examination, two questions using different tool to be set.
- Students are allowed to pick one experiment from the lot.
- Strictly follow the instructions as printed on the cover page of answer script for breakup of marks.
- Change of experiment is allowed only once and Marks allotted to the procedure part to be made zero.

M.Tech-VLSI & ES-2018- THIRD SEMESTER SYLLABUS

CAD of DIGITAL SYSTEMS
[As per Choice Based Credit System (CBCS) scheme]
SEMESTER – III

Course Code	**18EVE31**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**04**	**SEE Marks**	**60**
Total Number of Lecture Hours	**50 (10 Hours per Module)**	**Exam Hours**	**03**

Credits –03

Course objectives: This course will enable students to:

- Use graph theory in physical design
- Learn various optimization methods
- Understand different techniques for placement and routing

Modules	RBT Levels
Module-1	
Introduction to Design Methodologies: The VLSI Design Problem, The Design Domains, Design Actions, Design Methods and Technologies. **VLSI Design Automation tools**: Algorithmic and System Design, Structural and Logic Design, Transistor-level Design, Layout Design, Verification Methods, Design Management Tools. **Algorithmic graph theory and computational complexity:** Terminology, Data Structures for the Representation of Graphs, Computational Complexity, Examples of Graph Algorithms. **Tractable and intractable problems:** Decision Problems, Complexity Classes, NP-completeness and NP-hardness, Consequences.	L1, L2
Module-2	
General purpose methods for combinational optimization: Backtracking and Branch-and-bound, Dynamic Programming, Integer Linear Programming, Local Search, Simulated Annealing, Tabu Search, Genetic Algorithms, A Few Final Remarks on General-purpose Methods. **Layout compaction:** Design Rules, Symbolic Layout, Problem Formulation, Algorithms for Constraint-graph Compaction, Other Issues.	L2,L3
Module-3	
Placement and partitioning: Circuit Representation, Wire-length Estimation, Types of Placement Problem, Placement Algorithm, Partitioning. **Floor planning:** Floorplanning Concepts, Shape Functions and Floorplan Sizing.	L2,L3
Module-4	

Routing: Types of Local Routing Problems, Area Routing, Channel Routing, Introduction to Global Routing, Algorithms for Global Routing. **Simulation:** General Remarks on VlSl Simulation, Gate-level Modeling and Simulation, Switch-level Modeling and Simulation.	L2,L3
Module-5	
Logic Synthesis and Verification: Introduction to Combinational Logic Synthesis, Binary-decision Diagrams, Two-level Logic Synthesis **High level synthesis:** Hardware Models for High Level Synthesis, Internal Representation of the Input Algorithm, Allocation, Assignment and Scheduling, Some Scheduling Algorithm, Some Aspects of the Assignment Problem, High-level Transformations.	L3,L4

Course Outcomes: After studying this course, students will be able to:

1. Solve graph theoretic problems.
2. Evaluate the computational complexity of an algorithm
3. Write algorithms for VLSI Automation
4. Simulate and synthesize digital circuits using VLSI automation tools.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Book:

- S H Gerez, " Algorithms for VLSI Design Automation", Wiley, India, 2nd edition

Reference Books:

- N.A. Sherwani, "Algorithms for VLSI Physical Design Automation". Springer International edition, 3rd edition.

ADVANCES IN IMAGE PROCESSING
[As per Choice Based credit System (CBCS) Scheme
SEMESTER – III

Subject Code	**18ECS321**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**04**	**SEE marks**	**60**
Total Number of Lecture Hours	**50 (10 Hours Per Module)**	**Exam Hours**	**03**

CREDITS – 04

Course Objectives: This course will enable students to:

1. Acquire fundamental knowledge in understanding the representation of the digital image and its properties
2. Equip with some pre-processing techniques required to enhance the image for further analysis purpose.
3. Select the region of interest in the image using segmentation techniques.
4. Represent the image based on its shape and edge information.
5. Describe the objects present in the image based on its properties and structure.

Modules	**RBT Level**
Module 1	
The image, its representations and properties: Image representations a few concepts, Image digitization, Digital image properties, Color images.	L1
Module 2	
Image Pre-processing: Pixel brightness transformations, geometric transformations, local pre-processing.	L1, L2
Module 3	
Segmentation: Thresholding; Edge-based segmentation – Edge image thresholding, Edge relaxation, Border tracing, Hough transforms; Region – based segmentation – Region merging, Region splitting, Splitting and merging, Watershed segmentation, Region growing post-processing.	L1, L2, L3
Module 4	
Shape representation and description: Region identification; Contour-based shape representation and description – Chain codes, Simple geometric border representation, Fourier transforms of boundaries, Boundary description using segment sequences, B-spline representation; Region-based shape representation and description – Simple scalar region descriptors, Moments, Convex hull.	L1, L2, L3
Module 5	
Mathematical Morphology: Basic morphological concepts, Four morphological principles, Binary dilation and erosion, Skeletons and object marking, Morphological segmentations and	L1, L2, L3

watersheds.

Course Outcomes: After studying this course, students will be able to:

- Understand the representation of the digital image and its properties
- Apply pre-processing techniques required to enhance the image for its further analysis.
- Use segmentation techniques to select the region of interest in the image for analysis
- Represent the image based on its shape and edge information.
- Describe the objects present in the image based on its properties and structure.
- Use morphological operations to simplify images, and quantify and preserve the main shape characteristics of the objects.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Books:

1. Milan Sonka, Vaclav Hlavac, Roger Boyle, "Image Processing, Analysis, and Machine Vision", Cengage Learning, 2013, ISBN: 978-81-315-1883-0

Reference Books:

1. Geoff Doughertry, Digital Image Processing for Medical Applications, Cambridge university Press, 2010
2. S.Jayaraman, S Esakkirajan, T.Veerakumar, Digital Image Processing, Tata McGraw Hill, 2011.

CMOS RF CIRCUIT DESIGN [As per Choice Based credit System (CBCS) Scheme SEMESTER – III			
Subject Code	**18EVE322**	**IA Marks**	**40**
Number of Lecture Hours/Week	**04**	**Exam marks**	**60**
Total Number of Lecture Hours	**50 (10 Hours per Module)**	**Exam Hours**	**03**
CREDITS – 04			

Course Objectives: This course will enable students to:

- Learn basic concepts in RF and microwave design emphasizing the effects of nonlinearity and noise.
- Appreciate communication system, multiple access and wireless standards necessary for RF circuit design.
- Deal with transceiver architecture, various receiver and transmitter designs, their merits and demerits
- Understand the design of RF building blocks such as Low Noise Amplifiers, Mixers, Oscillators and PLLs

Modules	**RBT Level**
Module 1	
Introduction to RF Design, Wireless Technology and Basic Concepts: A wireless world, RF design is challenging, The big picture. General considerations, Effects of Nonlinearity, Noise, Sensitivity and dynamic range, Passive impedance transformation. Scattering parameters, Analysis of nonlinear dynamic systems, conversion of gains and distortion	L1,L2,L3
Module 2	
Communication Concepts: General concepts, analog modulation, digital modulation, spectral re-growth, coherent and non-coherent detection, Mobile RF communications, Multiple access techniques, Wireless standards, Appendix 1: Differential phase shift keying.	L1,L2,L3
Module 3	
Transceiver Architecture: General considerations, Receiver architecture, Transmitter architectures, Direct conversion and two-step transmitters, RF testing for heterodyne, Homodyne, Image reject, Direct IF and sub sampled receivers.	L1,L2,L3
Module 4	
Low Noise Amplifiers and Mixers: General considerations, Problem of input matching, LNA topologies: common-source stage with inductive load, common-source stage with resistive feedback. Mixers-General considerations, passive down conversion mixers, Various mixers- working and implementation.	L1,L2,L3
Module 5	
VCO and PLLs- Oscillators- Basic topologies VCO and definition of phase noise, Noise power and trade off. Resonator VCO designs, Quadrature and single sideband generators. Radio	L1,L2,L3

frequency Synthesizers- PLLS, Various RF synthesizer architectures and frequency dividers, Power Amplifier design	

Course Outcomes: After studying this course, students will be able to:

1. Analyse the effect of nonlinearity and noise in RF and microwave design.
2. Exemplify the approaches taken in actual RF products.
3. Minimize the number of off-chip components required to design mixers, Low-Noise Amplifiers, VCO and PLLs.
4. Explain various receivers and transmitter topologies with their merits and drawbacks.
5. Demonstrate how the system requirements define the parameters of the circuits and the impact on the performance

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.

The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Book:

- B. Razavi, "RF Microelectronics", PHI, second edition.

Reference Books:

1.R. Jacob Baker, H.W. Li, D.E. Boyce "**CMOS Circuit Design, layout and Simulation**", PHI 1998.
2. Thomas H. Lee "**Design of CMOS RF Integrated Circuits**" Cambridge University press 1998.
3. Y.P. Tsividis, "**Mixed Analog and Digital Devices and Technology**", TMH 1996

EMBEDDED LINUX SYSTEM DESIGN AND DEVELOPMENT
[As per Choice Based Credit System (CBCS) scheme]
SEMESTER – III

Course Code	**18EVE323**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**04**	**SEE Marks**	**60**
Total Number of Lecture Hours	**50 (10 Hours per Module)**	**Exam Hours**	**03**

Credits –03

Course objectives: This course will enable students to:

- Understand transition roadmap from a traditional RTOS to embedded Linux.
- Explain the steps involved in building a GNU cross-platform tool chain
- Explains boot loader architecture, system memory map, both hardware and software memory maps, interrupt management, the PCI subsystem, timers, UART, and power management.
- Explains the MTD subsystem architecture for accessing flash devices, discusses various embedded file systems
- Learn various embedded drivers such as the Serial driver, Ethernet driver, I2C subsystem, and USB gadgets.

Modules	**RBT Levels**
Module-1	
Introduction: History of Embedded Linux, Why Embedded Linux, Embedded Linux Versus Desktop Linux, Frequently Asked Questions, Embedded Linux Distributions, Porting Roadmap. **Getting Started**: Architecture of Embedded Linux, Linux Kernel Architecture, User Space, Linux Start-Up Sequence, GNU Cross-Platform Tool chain.	L1, L2
Module-2	
Board Support Package: Inserting BSP in Kernel Build Procedure, Memory Map, Interrupt Management, The PCI Subsystem, Timers, UART, Power Management.	L2,L3
Module-3	
Embedded Storage: Flash Map, MTD—Memory Technology Device, MTD Architecture, Sample MTD Driver for NOR Flash, The Flash-Mapping Drivers, MTD Block and Character Devices, Mtdutils Package, Embedded File Systems, Optimizing Storage Space, Tuning Kernel Memory.	L2,L3
Module-4	
Embedded Drivers : Linux Serial Driver, Ethernet Driver , I2C Subsystem on Linux, USB Gadgets, Watchdog Timer, Kernel Modules**.**	L2,L3
Module-5	
Porting Applications: Architectural Comparison, Application Porting Roadmap, Programming with Pthreads, Operating System Porting Layer (OSPL), Kernel API Driver.	L2,L4

Course Outcomes: After studying this course, students will be able to:

- Understand the embedded Linux development environment.
- Understand and create Linux BSP for a hardware platform.
- Understand the Linux model for embedded storage and write drivers and applications for the same.
- Understand various embedded Linux drivers such as serial, I2C, and so on.
- Port applications to embedded Linux from a traditional RTOS.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Book:

- P.Raghvan,Amol Lad,Sriram Neelakandan, "Embedded Linux System Design And Development", Auerbach Publications,Taylor & Francis Group, 2006 .

Reference Book:

- Karim Yaghmour, Jon Masters, Gilad Ben-Yossef, and Philippe Gerum, "Building Embedded Linux Systems" O'Reilly publications, 2nd edition.

VLSI DESIGN FOR SIGNAL PROCESSING

[As per Choice Based credit System (CBCS) Scheme

SEMESTER – III

Subject Code	**18EVE331**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**04**	**SEE marks**	**60**
Total Number of Lecture Hours	**50 (10 Hours per Module)**	**Exam Hours**	**03**

CREDITS – 04

Course Objectives: This course will enable students to:

- Learn several high-level architectural transformations that can be used to design families of architectures for a given algorithm.
- Deal with high-level algorithm transformations such as strength reduction, look-ahead and relaxed look-ahead.

Modules	**RBT Level**
Module 1	
Introduction to DSP Systems: Typical DSP Algorithms, DSP Application Demands and Scaled CMOS Technologies, Representations of DSP Algorithms. **Iteration Bounds:** Data flow graph Representations, loop bound and Iteration bound. Algorithms for Computing Iteration Bound, Iteration Bound of multi rate data flow graphs.	L1, L2
Module 2	
Pipelining and Parallel Processing: pipelining of FIR Digital Filters, parallel processing, Pipelining and parallel processing for low power. **Retiming:** Definition and Properties, Solving Systems of Inequalities, Retiming Techniques.	L1,L2,L3
Module 3	
Unfolding: An Algorithm for Unfolding, Properties of Unfolding, Critical path, Unfolding and Retiming, Application of Unfolding. **Folding:** Folding Transformation, Register Minimization Techniques, Register Minimization in Folded Architectures, Folding of Multirate Systems.	L1,L2,L3
Module 4	
Systolic Architecture Design: systolic array design Methodology, FIR systolic array, Selection of Scheduling Vector, Matrix-Matrix Multiplication and 2D systolic Array Design, Systolic Design for space representation containing Delays. **Fast convolution**: Cook-Toom Algorithm, Winograd Algorithm, Iterated convolution, cyclic convolution Design of fast convolution Algorithm by Inspection.	L1,L2,L3
Module 5	
Pipelined and Parallel Recursive and Adaptive Filter: Pipeline	L1,L2,L3

Interleaving in Digital Filter, first order IIR digital Filter, Higher order IIR digital Filter, parallel processing for IIR filter, Combined pipelining and parallel processing for IIR Filter, Low power IIR Filter Design Using Pipelining and parallel processing, pipelined adaptive digital filter.	

Course Outcomes: After studying this course, students will be able to:

1. Illustrate the use of various DSP algorithms and addresses their representation using block diagrams, signal flow graphs and data-flow graphs
2. Use pipelining and parallel processing in design of high-speed /low-power applications
3. Apply unfolding in the design of parallel architecture
4. Evaluate the use of look-ahead techniques in parallel and pipelined IIR Digital filters.
5. Develop an algorithm or architecture or circuit design for DSP applications

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Book:

- Keshab K.Parthi, "VLSI Digital Signal Processing systems, Design and implementation ", Wiley 1999.

Reference Books:

1. Mohammed Isamail and Terri Fiez, "Analog VLSI Signal and Information Processing ", Mc Graw-Hill,1994.
2. S.Y. Kung, H.J. White House, T. Kailath, " VLSI and Modern Signal Processing ", Prentice Hall, 1985.
3. Jose E. France, Yannis Tsividis, " Design of Analog - Digital VLSI Circuits for Telecommunication and Signal Processing ", Prentice Hall, 1994.
4. Lars Wanhammar, “DSP Integrated Circuits”, Academic Press Series in Engineering, 1st Edition.

PATTERN RECOGNITION and MACHINE LEARNING
[As per Choice Based Credit System (CBCS) scheme]
SEMESTER – III

Course Code	**18ESP332**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**04**	**SEE Marks**	**60**
Total Number of Lecture Hours	**50 (10 Hours per Module)**	**Exam Hours**	**03**

Credits – 04

Course objectives: The objective of the course is to discusses main and modern concepts for model selection and parameter estimation in recognition, decision making and statistical learning problems. Special emphasis will be given to regression, classification, regularization, feature selection and density estimation in supervised mode of learning.

Modules	**RBT Levels**
Module-1	
Introduction: Probability Theory, Model Selection, The Curse of Dimensionality, Decision Theory, Information Theory **Distributions:** Binary and Multinomial Variables, The Gaussian Distribution, The Exponential Family, Nonparametric Methods. **(Ch.: 1,2)**	**L1,L2**
Module-2	
Supervised Learning **Linear Regression Models:** Linear Basis Function Models, The Bias-Variance Decomposition, Bayesian Linear Regression, Bayesian Model Comparison **Classification & Linear Discriminant Analysis:** Discriminant Functions, Probabilistic Generative Models, Probabilistic Discriminative Mode **Ch. :3,4)**	**L1,L2,L3**
Module-3	
Supervised Learning **Kernels:** Dual Representations, Constructing Kernels, Radial Basis Function Network, Gaussian Processes **Support Vector Machines:** Maximum Margin Classifiers, Relevance Vector Machines **Neural Networks:** Feed-forward Network, Network Training, Error Backpropagation **(Ch:5,6,7)**	**L1,L2,L3**
Module-4	
Unsupervised Learning: **Mixture Models:** K-means Clustering, Mixtures of Gaussians, Maximum likelihood, EM for Gaussian mixtures, Alternative View of EM. **Dimensionality Reduction:** Principal Component Analysis, Factor/Component Analysis, Probabilistic PCA, Kernel PCA, Nonlinear Latent Variable Models **(Ch.: 9,12)**	**L1,L2,L3**
Module-5	

Probabilistic Graphical Models: Bayesian Networks, Conditional Independence, Markov Random Fields, Inference in Graphical Models, Markov Model, Hidden Markov Models **(Ch.:8,13)**	**L1,L2,L3**

Course Outcomes: At the end of this course, students will be able to

1. Identify areas where Pattern Recognition and Machine Learning can offer a solution.
2. Describe the strength and limitations of some techniques used in computational Machine Learning for classification, regression and density estimation problems.
3. Describe and model data.
4. Solve problems in Regression and Classification.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Book:

1. Pattern Recognition and Machine Learning. Christopher Bishop. Springer, 2006

INTERNET of THINGS
[As per Choice Based Credit System (CBCS) scheme]
SEMESTER – III

Course Code	**18ECS333**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**04**	**SEE Marks**	**60**
Total Number of Lecture Hours	**50 (10 Hours per Module)**	**Exam Hours**	**03**

Credits – 04

Course objectives: This course will enable students to:

- Introduce concept of IOT and its applications in today's scenario.
- Understand IOT content generation and transport through networks
- Understand the devices employed for IOT data acquisition and communication access technologies
- Introduce some use cases of IOT

Module-1	**RBT**
What is IOT Genesis, Digitization, Impact, Connected Roadways, Buildings, Challenges **IOT Network Architecture and Design** Drivers behind new network Architectures, Comparing IOT Architectures, M2M architecture, IOT world forum standard, IOT Reference Model, Simplified IOT Architecture.	**L1, L2**
Module-2	
IOT Network Architecture and Design Core IOT Functional Stack, Layer1(Sensors and Actuators), Layer 2(Communications Sublayer), Access network sublayer, Gateways and backhaul sublayer, Network transport sublayer, IOT Network management. Layer 3(Applications and Analytics) – Analytics vs Control, Data vs Network Analytics IOT Data Management and Compute Stack	**L2,L3**
Module-3	
Engineering IOT Networks Things in IOT – Sensors, Actuators, MEMS and smart objects. Sensor networks, WSN, Communication protocols for WSN Communications Criteria, Range Frequency bands, power consumption, Topology, Constrained Devices, Constrained Node Networks IOT Access Technologies, IEEE 802.15.4 Competitive Technologies – Overview only of IEEE 802.15.4g, 4e, IEEE 1901.2a Standard Alliances – LTE Cat0, Cat-M, NB-IOT	**L2,L3**
Module-4	

Engineering IOT Networks IP as IOT network layer, Key Advantages, Adoption, Optimization, Constrained Nodes, Constrained Networks, IP versions, Optimizing IP for IOT. Application Protocols for IOT – Transport Layer, Application Transport layer, Background only of SCADA, Generic web based protocols, IOT Application Layer Data and Analytics for IOT – Introduction, Structured and Unstructured data, IOT Data Analytics overview and Challenges.	**L3,L4**
Module-5	
IOT in Industry (Three Use cases) IOT Strategy for Connected manufacturing, Architecture for Connected Factory Utilities – Power utility, IT/OT divide, Grid blocks reference model, Reference Architecture, Primary substation grid block and automation. Smart and Connected cities –Strategy, Smart city network Architecture, Street layer, city layer, Data center layer, services layer, Smart city security architecture, Smart street lighting.	**L3,L4**

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Course Outcomes: After studying this course, students will be able to:

1. Understand the basic concepts IOT Architecture and devices employed.
2. Analyze the sensor data generated and map it to IOT protocol stack for transport.
3. Apply communications knowledge to facilitate transport of IOT data over various available communications media.
4. Design a use case for a typical application in real life ranging from sensing devices to analyzing the data available on a server to perform tasks on the device.

Text Book:

- CISCO, IOT Fundamentals – Networking Technologies, Protocols, Use Cases for IOT, Pearson Education; First edition (16 August 2017). ISBN-10: 9386873745, ISBN-13: 978-9386873743

Reference Book:

- Arshdeep Bahga and Vijay Madisetti, 'Internet of Things – A Hands on Approach', Orient Blackswan Private Limited - New Delhi; First edition (2015), ISBN-10: 8173719543, ISBN-13: 978-8173719547

SCHEME OF TEACHING AND EXAMINATION 2016-17

M.Tech. in Communication Systems, Digital Communication & Networking, Digital Communication Engineering, Digital Electronics & Communication Systems, Digital Electronics & Communication

(Common to all 5 Programmes)

I SEMESTER

Sl. No	Subject Code	Title	Teaching Hours /Week		Examination				Credit
			Theory	Practical/Field Work/ Assignment	Duration	I.A. Marks	Theory/ Practical Marks	Total Marks	
1	16ELD11	Advanced Engineering Mathematics	4	-	3	20	80	100	4
2	16ECS12	Antenna Theory and Design	4	-	3	20	80	100	4
3	16EVE13	Advanced Embedded System	4	-	3	20	80	100	4
4	16ECS14	Advanced Digital Communication	4	-	3	20	80	100	4
5	16EXX15X	Elective-1	3	-	3	20	80	100	3
6	16ECSL16	Advanced Communication Lab		3	3	20	80	100	2
7	16ECS17	Seminar on advanced topics from refereed journals	-	3	-	100	-	100	1
TOTAL			**19**	**6**	**18**	**220**	**480**	**700**	**22**

Elective-1	
16ECS151	Advanced Computer Networks
16EVE152	Nanoelectronics
16ECS153	Optical Communication and Networking
16ECS154	Simulation, Modelling and Analysis

M.Tech. in Communication Systems, Digital Communication & Networking, Digital Communication Engineering, Digital Electronics & Communication Systems, Digital Electronics & Communication
(Common to all 5 Programmes)

II SEMESTER

Sl. No	Subject Code	Title	Teaching Hours /Week		Examination				Credit
			Theory	Practical/Field Work/ Assignment	Duration	I.A. Marks	Theory/ Practical Marks	Total Marks	
1	16ECS21	Advanced DSP	4	-	3	20	80	100	4
2	16ECS22	Error Control Coding	4	-	3	20	80	100	4
3	16ECS23	Wireless Communication	4	-	3	20	80	100	4
4	16ECS24	RF and Microwave Circuit Design	4	-	3	20	80	100	4
5	16EXX25X	Elective-2	3	-	3	20	80	100	3
6	16ECSL26	Advanced DSP Lab		3	3	20	80	100	2
7	16ECS27	Seminar on advanced topics from refereed journals	-	3	-	100	-	100	1
TOTAL			**19**	**6**	**18**	**220**	**480**	**700**	**22**

Elective-2	
16ELD251	Automotive Electronics
16ECS252	Multimedia Over Communication links
16ELD253	Micro Electro Mechanical Systems
16ECS254	Cryptography and Network Security

M.Tech. in Communication Systems, Digital Communication & Networking, Digital Communication Engineering, Digital Electronics & Communication Systems, Digital Electronics & Communication
(Common to all 5 Programmes)

III SEMESTER: Internship

Sl. No	Subject Code	Title	Teaching Hours /Week		Examination				Credit
			Theory	Practical/Field Work/ Assignment	Duration	I.A. Marks	Theory/ Practical Marks	Total Marks	
1	16ECS31	Seminar / Presentation on Internship (After 8 weeks from the date of commencement)	-	-	-	25	-	25	20
2	16ECS32	Report on Internship	-	-	-	25	-	25	
3	16ECS33	Evaluation and Viva-Voce of Internship	-	-	-	-	50	50	
4	16ECS34	Evaluation of Project phase -1	-	-	-	50	-	50	1
TOTAL			**-**	**-**	**-**	**100**	**50**	**150**	**21**

M.Tech. in Communication Systems, Digital Communication & Networking, Digital Communication Engineering, Digital Electronics & Communication Systems, Digital Electronics & Communication
(Common to all 5 Programmes)

IV SEMESTER

Sl. No	Subject Code	Title	Teaching Hours /Week		Examination				Credit
			Theory	Practical/Field Work/ Assignment	Duration	I.A. Marks	Theory/ Practical Marks	Total Marks	
1	16ECS41	Wireless Broadband LTE 4G	4	-	3	20	80	100	4
2	16EXX42X	Elective-3	3	-	3	20	80	100	3
3	16ECS43	Evaluation of Project phase -2	-	-	-	50	-	50	3
4	16ECS44	Evaluation of Project and Viva-Voce	-	-	-	-	100+100	200	10
TOTAL			**-**	**-**	**6**	**90**	**360**	**450**	**20**

Elective-3	
16EVE421	CMOS RF Circuit Design
16ECS422	Advances in Image Processing
16ECS423	Communication System Design using DSP Algorithms
16ECS424	Real Time Systems

Note:

1. Project Phase-1: 6-week duration shall be carried out between 2nd and 3rd Semester vacation. Candidates in consultation with the guide shall carry out literature survey/ visit industries to finalize the topic of Project.

2. Project Phase-2: 16-week duration during 4th semester**.** Evaluation shall be done by the committee constituted comprising of HoD as Chairman, Guide and Senior faculty of the department.

3. **Project Evaluation**: Evaluation shall be taken up at the end of 4thsemester. Project work evaluation and Viva-Voce examination shall be conducted.

a. Internal Examiner shall carry out the evaluation for 100 marks.
b. External Examiner shall carry out the evaluation for 100 marks.
c .The average of marks allotted by the internal and external examiner shall be the final marks of the project evaluation.
d. Viva-Voce examination of Project work shall be conducted jointly by Internal and External examiner for 100 marks.

M.Tech-Commn Stream-2016-FIRST SEMESTER SYLLABUS

ADVANCED ENGINEERING MATHEMATICS [As per Choice Based Credit System (CBCS) scheme] SEMESTER – I			
Subject Code	16ELD11	IA Marks	20
Number of Lecture Hours/Week	04	Exam Marks	80
Total Number of Lecture Hours	50 (10 Hours per Module)	Exam Hours	03
CREDITS – 04			

Course objectives: This course will enable students to:

- Acquaint with principles of linear algebra, calculus of variations, probability theory and random process.
- Apply the knowledge of linear algebra, calculus of variations, probability theory and random process in the applications of electronics and communication engineering sciences.

Modules	**Revised Bloom's Taxonomy (RBT) Level**
Module -1	
Linear Algebra-I Introduction to vector spaces and sub-spaces, definitions, illustrative examples and simple problems. Linearly independent and dependent vectors-definition and problems. Basis vectors, dimension of a vector space. Linear transformations- definition, properties and problems. Rank-Nullity theorem(without proof). Matrix form of linear transformations-Illustrative examples.**(Text 1 & Ref. 1)**	**L1,L2**
Module -2	
Linear Algebra-II Computation of Eigen values and Eigen vectors of real symmetric matrices-Given's method. Orthogonal vectors and orthogonal bases. Gram-Schmidt orthogonalization process. QR decomposition, singular value decomposition, least square approximations.**(Text 1 & Ref. 1)**	**L1,L2**
Module -3	
Calculus of Variations Concept of functional-Eulers equation. functional dependent on first and higher order derivatives, functional on several dependent variables. Isoperimetric problems-variation problems with moving boundaries.**(Text 2 & Ref. 2)**	**L1,L2**
Module -4	

Probability Theory Review of basic probability theory. Definitions of random variables and probability distributions, probability mass and density functions, expectation, moments, central moments, characteristic functions, probability generating and moment generating functions-illustrations. Binomial, Poisson, Exponential, Gaussian and Rayleigh distributions-examples.**(Text 3 & Ref. 3)**	**L1,L2**
Module -5	
Joint probability distributions Definition and properties of CDF, PDF, PMF, conditional distributions. Expectation, covariance and correlation. Independent random variables. Statement of central limit theorem-Illustrative examples. Random process- Classification, stationary and ergodic random process. Auto correlation function-properties, Gaussian random process.**(Text 3 & Ref. 3)**	**L1,L2**

Course Outcomes: After studying this course, students will be able to:

- Understand vector spaces, basis, linear transformations and the process of obtaining matrix of linear transformations arising in magnification and rotation of images.
- Apply the techniques of QR and singular value decomposition for data compression, least square approximation in solving inconsistent linear systems.
- Utilize the concepts of functionals and their variations in the applications of communication systems, decision theory, synthesis and optimization of digital circuits.
- Learn the idea of random variables (discrete/continuous) and probability distributions in analyzing the probability models arising in control systems and system communications.
- Apply the idea of joint probability distributions and the role of parameter-dependent random variables in random process.

Question paper pattern:

- The question paper will have 10 full questions carrying equal marks.
- Each full question consists of 16 marks with a maximum of four sub questions.
- There will be 2 full questions from each module covering all the topics of the module
- The students will have to answer 5 full questions, selecting one full question from each module.

Text Books:

1. David C.Lay, Steven R.Lay and J.J.McDonald: Linear Algebra and its Applications, 5th Edition, Pearson Education Ltd., 2015.
2. E. Kreyszig, "Advanced Engineering Mathematics", 10th edition, Wiley, 2015.
3. Scott L.Miller, Donald G.Childers: "Probability and Random Process with application to Signal Processing", Elsevier Academic Press, 2nd Edition,2013.

Reference books:

1. Richard Bronson: "Schaum's Outlines of Theory and Problems of Matrix Operations", McGraw-Hill, 1988.
2. Elsgolts L.: "Differential Equations and Calculus of Variations", MIR Publications, 3rd Edition, 1977.
3. T.Veerarajan: "Probability, Statistics and Random Process", 3rd Edition, Tata McGraw Hill Co.,2008.

Web links:

1. http://nptel.ac.in/courses.php?disciplineId=111
2. http://www.class-central.com/subject/math(MOOCs)
3. http://ocw.mit.edu/courses/mathematics/
4. www.wolfram.com

ANTENNA THEORY AND DESIGN

[As per Choice Based Credit System (CBCS) scheme]

SEMESTER – I

Subject Code	16ECS12	IA Marks	20
Number of Lecture Hours/Week	04	Exam Marks	80
Total Number of Lecture Hours	50 (10 Hours per Module)	Exam Hours	03

CREDITS – 04

Course objectives: This course will enable students to:

- Introduce and discuss different types of Antennas, various terminologies, excitations.
- Study different types of Arrays, Pattern-multiplication, Feeding techniques.
- Calculate gain of aperture antennas, Reflector antennas and analyze general feed model.
- Define, describe, and illustrate principle behind antenna synthesis.
- Introduction of Method of moments, Pocklington's integral equation, Source modeling.

Modules	**Revised Bloom's Taxonomy (RBT) Level**
Module -1	
Antenna Fundamentals and Definitions: Radiation Mechanisms, Overview, EM Fundamentals, Solution of Maxwell's Equations for Radiation Problems, Ideal Dipole, Radiation patterns, Directivity and Gain, Antenna impedance, Radiation efficiency, Antenna polarization.	**L1,L2**
Module -2	
Arrays: Array factor for linear arrays, Uniformly excited equally spaced linear arrays, Pattern multiplication, Directivity of linear arrays, Non-uniformly excited equally spaced linear arrays, Mutual coupling. **Antenna Synthesis**: Formulation of the synthesis problem, Synthesis principles, Line sources shaped beam synthesis, Linear array shaped beam synthesis, Fourier series, Woodward - Lawson sampling method, Comparison of shaped beam synthesis methods, low side lobe narrow main beam synthesis methods, Dolph Chebyshev linear array, Taylor line source method.	**L1,L2,L3, L4**
Module -3	
Resonant Antennas: Wires and Patches, Dipole antenna, Yagi-Uda antennas, Micro-strip antenna. **Broadband antennas**: Traveling wave antennas Helical antennas, Biconical antennas, Sleeve antennas, and Principles of frequency independent antennas, Spiral antennas, and Log - periodic antennas.	**L1,L2,L3, L4**

Module -4	
Aperture antennas: Techniques for evaluating gain, Reflector antennas- Parabolic reflector antenna principles, Axi-symmetric parabolic reflector antenna, Offset parabolic reflectors, Dual reflector antennas, Gain calculations for reflector antennas, Feed antennas for reflectors, Field representations, Matching the feed to the reflector, General feed model, Feed antennas used in practice.	**L1,L2,L3, L4**
Module -5	
CEM for antennas: The method of moments: Introduction of the methods moments, Pocklington's integral equation, Integral equation and Kirchhoff's networking equations, Source modeling weighted residual formulations and computational consideration, Calculation of antenna and scatter characteristics.	**L1,L2**

Course Outcomes: After studying this course, students will be able to:

- Classify different types of antennas
- Define and illustrate various types of array antennas
- Design antennas like Yagi-Uda, Helical antennas and other broad band antennas
- Describe different antenna synthesis methods
- Apply methods like MOM

Question paper pattern:

- The question paper will have 10 full questions carrying equal marks.
- Each full question consists of 16 marks with a maximum of four sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- The students will have to answer 5 full questions, selecting one full question from each module.

Text Book:

Stutzman and Thiele, "Antenna Theory and Design", 2nd Edition, John Wiley, 2010.

Reference Books:

1. C. A. Balanis, "Antenna Theory Analysis and Design", John Wiley, 2nd Edition 2007.
2. J. D. Krauss, "Antennas and Wave Propagation", McGraw Hill TMH, 4th Edition, 2010.
3. A.R.Harish, M.Sachidanada, "Antennas and propagation", Pearson Education, 2015.

ADVANCED EMBEDDED SYSTEM

[As per Choice Based Credit System (CBCS) scheme]

SEMESTER – I

Subject Code	16EVE13	IA Marks	20
Number of Lecture Hours/Week	04	Exam Marks	80
Total Number of Lecture Hours	50 (10 Hours per Module)	Exam Hours	03

CREDITS – 04

Course objectives: This course will enable students to:

- Understand the basic hardware components and their selection method based on the characteristics and attributes of an embedded system.
- Describe the hardware software co-design and firmware design approaches
- Explain the architectural features of ARM CORTEX M3, a 32 bit microcontroller including memory map, interrupts and exceptions.
- Program ARM CORTEX M3 using the various instructions, for different applications.

Modules	**Revised Bloom's Taxonomy (RBT) Level**
Module -1	
Embedded System: Embedded vs General computing system, classification, application and purpose of ES. Core of an Embedded System, Memory, Sensors, Actuators, LED, Opto coupler, Communication Interface, Reset circuits, RTC, WDT, Characteristics and Quality Attributes of Embedded Systems (Text 1: Selected Topics from Ch -1, 2, 3).	**L1, L2, L3**
Module -2	
Hardware Software Co-Design, embedded firmware design approaches, computational models, embedded firmware development languages, Integration and testing of Embedded Hardware and firmware, Components in embedded system development environment (IDE), Files generated during compilation, simulators, emulators and debugging (Text 1: Selected Topics From Ch-7, 9, 12, 13).	**L1, L2, L3**

Module -3	
ARM-32 bit Microcontroller: Thumb-2 technology and applications of ARM, Architecture of ARM Cortex M3, Various Units in the architecture, General Purpose Registers, Special Registers, exceptions, interrupts, stack operation, reset sequence (Text 2: Ch 1, 2, 3)	**L1, L2, L3**
Module -4	
Instruction Sets: Assembly basics, Instruction list and description, useful instructions, Memory Systems, Memory maps, Cortex M3 implementation overview, pipeline and bus interface (Text 2: Ch-4, 5, 6)	**L1, L2, L3**
Module -5	
Exceptions, Nested Vector interrupt controller design, Systick Timer, Cortex-M3 Programming using assembly and C language, CMSIS (Text 2: Ch-7, 8, 10)	**L1, L2, L3**

Course Outcomes: After studying this course, students will be able to:

- Understand the basic hardware components and their selection method based on the characteristics and attributes of an embedded system.
- Explain the hardware software co-design and firmware design approaches.
- Acquire the knowledge of the architectural features of ARM CORTEX M3, a 32 bit microcontroller including memory map, interrupts and exceptions.
- Apply the knowledge gained for Programming ARM CORTEX M3 for different applications.

Question paper pattern:

- The question paper will have 10 full questions carrying equal marks.
- Each full question consists of 16 marks with a maximum of four sub questions.
- There will be 2 full questions from each module covering all the topics of the module
- The students will have to answer 5 full questions, selecting one full question from each module.

Text Books:

1. K. V. Shibu, "Introduction to embedded systems", TMH education Pvt. Ltd. 2009.
2. Joseph Yiu, “The Definitive Guide to the ARM Cortex-M3”, 2nd edn, Newnes, (Elsevier), 2010.

Reference Book:

James K. Peckol, "Embedded systems- A contemporary design tool", John Wiley, 2008.

ADVANCED DIGITAL COMMUNICATION

[As per Choice Based Credit System (CBCS) scheme]

SEMESTER – I

Subject Code	16ECS14	IA Marks	20
Number of Lecture Hours/Week	04	Exam Marks	80
Total Number of Lecture Hours	50(10 Hours per Module)	Exam Hours	03

CREDITS – 04

Course objectives: This course will enable students to:

- Analyze the operation of different modulation techniques and analyze the error performance of digital modulation techniques in presence of AWGN noise.
- Explain and demonstrate the model of discrete time channel with ISI.
- Explain the model of discrete time channel by equalizer.
- Explain various types of equalizers used for channel modeling and adjusting the filter coefficients
- Understand the concept of spread spectrum communication system and analyze the error performance.

Modules	**Revised Bloom's Taxonomy (RBT) Level**
Module -1	
Digital Modulation Schemes: Representation of Digitally Modulated Signals, Memoryless Modulation Methods-PAM, Phase Modulation, QAM, Multidimensional Signalling, Signalling Schemes with memory: CPFSK, CPM, MSK, OQPSK. Transmit PSD for Modulation Schemes (Chapter 3: 3.1,3.2,3.3, 3.4.1 and 3.4.2 of Text).	**L1,L2,L3**
Module -2	
Optimum Receivers for AWGN channels: Waveform and Vector channel models, Waveform and Vector AWGN channels- Optimal detection, Implementation, Optimal Detection and Error Probability for Band limited signaling, Optimal detection and error probability for power limited signaling. Non Coherent Detection (without derivations) (Chapter 4: 4.1, 4.2 - 4.2.1, 4.2.2, 4.3, 4.4, 4.5.1, 4.5.2, eqn 4.5.45 to 4.5.47, 4.5.5 up to eqn 4.5.62 of Text).	**L1,L2,L3**
Module -3	

Multichannel and Multicarrier Signalling: Multichannel Communications in an AWGN channel, Multicarrier Communications in AWGN channel (Chapter 11- 11.1, 11.2-1 to 11.2-5 of Text). **Synchronization**: Signal Parameter estimation, Carrier Phase Estimation, Symbol Timing Recovery (Chapter 5- 5.1 to 5.3 of Text).	**L1,L2,L3**
Module -4	
Digital Communication through band-limited channels: Characterization of Band-limited channels, Optimum Receiver for channels with ISI and AWGN, Linear equalization, Decision feedback equalization (Chapter 9: 9.1,9.3- 9.3.1, 9.3.2, 9.4- 9.4.1, 9.4.2, 9.4.4, 9.4.5, 9.5- 9.5.1, 9.5.3 of Text). Adaptive equalization: Adaptive linear equalizer, adaptive decision feedback equalizer, Adaptive equalization of Trellis - coded signals (Chapter 10: 10.1, 10.2, 10.3 of Text).	**L1,L2,L3**
Module -5	
Spread spectrum signals for digital communication: Model of spread spectrum digital communication system, Direct sequence spread spectrum signals, Frequency hopped spread spectrum signals, CDMA, Time hopping SS, Synchronization of SS systems (Chapter 12 of Text).	**L1,L2**

Course Outcomes: After studying this course, students will be able to:

- Acquire knowledge of application and practical implementation of various Digital Modulation techniques.
- Explain Inter symbol interference (ISI) and its channel modeling and different filtering algorithms for the ISI elimination.
- Explain different types spread spectrum system
- Identify the effect of signal characteristics on the choice of a channel model.
- Analyse the performance of Digital Modulation techniques, Different filtering algorithms and Spread spectrum communication system

Question paper pattern:

- The question paper will have 10 full questions carrying equal marks.
- Each full question consists of 16 marks with a maximum of four sub questions.
- There will be 2 full questions from each module covering all the topics of the module
- The students will have to answer 5 full questions, selecting one full question from each module.

Text Book:

John G. Proakis, Masoud Salehi, "Digital Communications", McGraw Hill, 5th Edition, 2008.

Reference: Book:

Bernard Sklar, "Digital Communication - Fundamental and applications", Pearson education (Asia), Pvt. Ltd., 2nd edition, 2001.

ADVANCED COMPUTER NETWORKS

[As per Choice Based Credit System (CBCS) scheme]

SEMESTER –I

Subject Code	16ECS151	IA Marks	20
Number of Lecture Hours/Week	03	Exam Marks	80
Total Number of Lecture Hours	40 (08 Hours Per Module)	Exam Hours	03

CREDITS – 03

Course objectives: This course will enable students to:

- Develop an awareness towards basic networking principles
- Learn various aspects involved in multiple access and multiplexing
- Develop an awareness regarding the LAN architectures and the various data switching techniques
- Learn the scheduling techniques of networks
- Learn protocols operating in at different layers of computer networks
- Develop an awareness towards the network control and traffic management

Modules	**Revised Bloom's Taxonomy (RBT) Level**
Module -1	
Introduction to networks: Computer network, Telephone networks, Networking principles (Text 1), Protocol layering (Text 2), Multiplexing- TDM, FDM, SM, WDM (Text 1). **Multiple Access:** Introduction, Choices and constraints, base technologies, centralized and distributed access schemes (Text 2).	**L1, L2, L3**
Module -2	
Local Area Networks: Ethernet - Physical layer, MAC, LLC, LAN interconnection, Token ring- Physical layer, MAC, LLC, FDDI (Text 1). Switching- introduction, circuit switching, packet switching, multicasting (Text 2). **Scheduling:** Introduction, requirements, choices, performance bounds, best- effort techniques. Naming and addressing (Text 2).	**L1, L2, L3**

Module -3	
SONET, SDH (Text 2), ATM Networks- features, signaling and routing, header and adaptation layers (Text 1), virtual circuits, SSCOP, Internet-addressing, routing, end point control (Text 2). **Internet protocols-** IP, TCP, UDP, ICMP, HTTP (Text 2).	**L1, L2, L3**
Module -4	
Traffic Management: Introduction, framework for traffic management, traffic models, traffic classes, traffic scheduling (Text 2). **Control of Networks:** Objectives and methods of control, routing optimization in circuit and datagram networks, Markov chains, Queuing models in circuit and datagram networks (Text 1).	**L1, L2, L3**
Module -5	
Congestion and flow control: Window congestion control, rate congestion control, control in ATM Networks (Text 1), flow control model, open loop flow control, closed loop flow control (Text 2).	**L1, L2, L3, L4**

Course outcomes: After studying this course, students will be able to:

- Choose appropriate multiple access and multiplexing techniques as per the requirement.
- Choose standards for establishing a computer network
- Identify switching techniques based on the applications of the network
- Identify IP configuration for the network with suitable routing, scheduling, error control and flow control
- Analyze and develop various network traffic management and control techniques

Question paper pattern:

- The question paper will have 10 full questions carrying equal marks.
- Each full question consists of 16 marks with a maximum of four sub questions.
- There will be 2 full questions from each module covering all the topics of the module
- The students will have to answer 5 full questions, selecting one full question from each module.

Text Books:

1. J. Walrand and P. Varaya, "High performance communication networks", Harcourt Asia (Morgan Kaufmann), 2000.
2. S. Keshav, "An Engineering approach to Computer Networking", Pearson Education, 1997.

Reference Books:

1. Leon-Garcia, and I. Widjaja, "Communication network: Fundamental concepts and key architectures", TMH, 2000.
2. J. F. Kurose, and K. W. Ross, "Computer networking: A top down approach featuring the Internet", Pearson Education, 2001.

NANOELECTRONICS

[As per Choice Based Credit System (CBCS) scheme]

Subject Code	16EVE152	IA Marks	20
Number of Lecture Hours/Week	03	Exam Marks	80
Total Number of Lecture Hours	40 (08 Hours per Module)	Exam Hours	03

CREDITS – 03

Course objectives: This course will enable students to:

- Enhance basic engineering science and technological knowledge of nanoele ctronics.
- Explain basics of top-down and bottom-up fabrication process, devices and systems.
- Describe technologies involved in modern day electronic devices.
- Appreciate the complexities in scaling down the electronic devices in the future.

Modules	**Revised Bloom's Taxonomy (RBT) Level**
Module -1	
Introduction: Overview of nanoscience and engineering. Development milestones in microfabrication and electronic industry. Moores' law and continued miniaturization, Classification of Nanostructures, Electronic properties of atoms and solids: Isolated atom, Bonding between atoms, Giant molecular solids, Free electron models and energy bands, crystalline solids, Periodicity of crystal lattices, Electronic conduction, effects of nanometer length scale, Fabrication methods: Top down processes, Bottom up processes methods for templating the growth of nanomaterials, ordering of nanosystems (Text1).	**L1, L2**
Module -2	
Characterization: Classification, Microscopic techniques, Field ion microscopy, scanning probe techniques, diffraction techniques: bulk and surface diffraction techniques (Text1).	**L1-L3**
Module -3	

Characterization: spectroscopy techniques: photon, radiofrequency, electron, surface analysis and dept profiling: electron, mass, Ion beam, Reflectrometry, Techniques for property measurement: mechanical, electron, magnetic, thermal properties. **Inorganic semiconductor nanostructures:** overview of semiconductor physics. Quantum confinement in semiconductor nanostructures: quantum wells, quantum wires, quantum dots, super-lattices, band offsets, electronic density of states (Text1).	**L1-L3**
Module -4	
Fabrication techniques: requirements of ideal semiconductor, epitaxial growth of quantum wells, lithography and etching, cleaved-edge over growth, growth of vicinal substrates, strain induced dots and wires, electrostatically induced dots and wires, Quantum well width fluctuations, thermally annealed quantum wells, semiconductor nanocrystals, collidal quantum dots, self-assembly techniques. **Physical processes:** modulation doping, quantum hall effect, resonant tunneling, charging effects, ballistic carrier transport, Inter band absorption, intraband absorption, Light emission processes, phonon bottleneck, quantum confined stark effect, nonlinear effects, coherence and dephasing, characterization of semiconductor nanostructures: optical electrical and structural (Text1).	**L1-L3**
Module -5	
Methods of measuring properties: atomic, crystollography, microscopy, spectroscopy (Text 2). **Applications**: Injection lasers, quantum cascade lasers, single-photon sources, biological tagging, optical memories, coulomb blockade devices, photonic structures, QWIP's, NEMS, MEMS (Text 1).	**L1-L3**

Course outcomes: After studying this course, students will be able to:

- Know the principles behind Nanoscience engineering and Nanoelectronics.
- Apply the knowledge to prepare and characterize nanomaterials.
- Know the effect of particles size on mechanical, thermal, optical and electrical properties of nanomaterials.
- Design the process flow required to fabricate state of the art transistor techn ology.
- Analyze the requirements for new materials and device structure in the futur e technologies.

Question paper pattern:

- The question paper will have 10 full questions carrying equal marks.
- Each full question consists of 16 marks with a maximum of four sub questions.
- There will be 2 full questions from each module covering all the topics of the module
- The students will have to answer 5 full questions, selecting one full question from each module.

Text Books:

1. Ed Robert Kelsall, Ian Hamley, Mark Geoghegan, “Nanoscale Science and Technology”, John Wiley, 2007.
2. Charles P Poole, Jr, Frank J Owens, “Introduction to Nanotechnology”, John Wiley, Copyright 2006, Reprint 2011.

Reference Book:

Ed William A Goddard III, Donald W Brenner, Sergey E. Lyshevski, Gerald J Iafrate, “Hand Book of Nanoscience Engineering and Technology”, CRC press, 2003.

OPTICAL COMMUNICATION AND NETWORKING

[As per Choice Based Credit System (CBCS) scheme]

SEMESTER –I

Subject Code	16ECS153	IA Marks	20
Number of Lecture Hours/Week	03	Exam Marks	80
Total Number of Lecture Hours	40 (08 Hours per Module)	Exam Hours	03

CREDITS – 03

Course objectives: This course will enable students to:

- Mathematically analyze and conceptualize basics of optical networking and its associated nonlinear artifacts and effects.
- Develop awareness regarding optical devices and their working strategies
- Develop awareness of WDM principles, and that of power penalty issues existent in optical Networks
- Get insight into the design of various types of Lasers and understand the techniques of coherent transmission.
- Develop an awareness towards the backbone architectures of optical networking with the present trends in access networks
- Design second generation optical networks using various existent & devices like OADM, OLT and OXC and to mathematically model the problems in the design of WDM networks

Modules	**Revised Bloom's Taxonomy (RBT) Level**
Module -1	
Introduction to optical networking: Propagation of signals in optical fiber, Different losses, Nonlinear effects, Solutions, Optical sources, Detectors. **Optical Components (Part-1**): Couplers, Isolators, Circulators and Multiplexers.	**L1, L2, L3**
Module -2	
Optical Components (Part-2): Filters, Gratings, Interferometers, Amplifiers. **Modulation - Demodulation**: Formats, Ideal receivers, Practical detection receivers, Optical preamplifiers, Noise considerations, Bit error rates, Coherent detection.	**L1, L2, L3**

Module -3	
Transmission System Engineering: System model, Power penalty, Transmitter, Receiver, Different optical amplifiers **Client Layers:** Client layers of optical layer, SONET/SDH, Multiplexing, layers, Frame structure, ATM functions, Adaptation layers, Quality of Service (QoS) and flow control, ESCON, HIPPI.	**L1, L2, L3**
Module -4	
WDM network elements: Optical line terminal, Optical line amplifiers, Optical Add/ Drop Multiplexors, Optical cross connectors. **WDM Network Design**: WDM network design, Cost tradeoffs, LTD and RWA problems, Routing and wavelength assignment, Wavelength conversion.	**L1, L2, L3**
Module -5	
Control and Management (Part-1): Network management functions, management framework, Information model, management protocols, Layers within optical layer. **Control and Management (Part-2):** Performance and fault management, Impact of transparency, BER measurement, Optical trace, Alarm management, Configuration management.	**L1, L2, L3**

Course outcomes: After studying this course, students will be able to:

- Recognize and select various optical networking components according to the prescribed design specifications
- Learn the aspects of data transmission, loss hindrances and other artifacts affecting the network operation
- Learn the issues involved in setting up and maintenance of access part of optical network with the latest trends in the data communication
- Design a WDM network and study the component and network management aspects

Question paper pattern:

- The question paper will have 10 full questions carrying equal marks.
- Each full question consists of 16 marks with a maximum of four sub questions.
- There will be 2 full questions from each module covering all the topics of the module
- The students will have to answer 5 full questions, selecting one full question from each module.

Text Book:

Rajiv Ramswami and K. N. Sivarajan, "Optical Networks", Morgon Kauffman Publishers, 3rd edition, 2010.

Reference Books:

1. John M. Senior, "Optical fiber communication", Pearson edition, 2000.
2. Gerd Kaiser, "Optical fiber Communication Systems", John Wiley, New York, 1997.
3. P. E. Green, "Optical Networks", Prentice Hall, 1994.

SIMULATION, MODELLING AND ANALYSIS

[As per Choice Based Credit System (CBCS) scheme]

SEMESTER – I

Subject Code	16ECS154	IA Marks	20
Number of Lecture Hours/Week	03	Exam Marks	80
Total Number of Lecture Hours	40 (08 Hours per Module)	Exam Hours	03

CREDITS – 03

Course objectives: This course will enable students to:

- Understand the process of simulation and modeling
- Learn simulation of deterministic and probabilistic models, with a focus of statistical data analysis and simulation data.

Modules	**Revised Bloom's Taxonomy (RBT)**
Module -1	
Basic Simulation Modeling: Nature of simulation, Systems, Models and Simulation, Discrete-Event Simulation, Simulation of Single Server Queuing System, Simulation of inventory system, Parallel and distributed simulation and the high level architecture, Steps in sound simulation study, and Other types of simulation, Advantages and disadvantages. (1.1, 1.2, 1.3, 1.4, 1.4.1, 1.4.2, 1.4.3, 1.5, 1.5.1, 1.5.2, 1.6, 1.7, 1.8, 1.9 of Text)	**L1,L2**
Module -2	
Review of Basic Probability and Statistics Random Variables and their properties, Simulation Output Data and Stochastic Processes, Estimation of Means, Variances and Correlations, Confidence Intervals and Hypothesis tests for the Mean **Building valid, credible and appropriately detailed simulation models**: Introduction and definitions, Guidelines for determining the level of models detail, Management's Role in the Simulation Process, Techniques for increasing model validity and credibility, Statistical procedure for comparing the real world observations and simulation output data. (4.2, 4.3, 4.4, 4.5, 5.1, 5.2, 5.4, 5.5, 5.6, 5.6.1, 5.6.2 of Text)	**L1,L2, L3**
Module -3	

Selecting Input Probability Distributions: Useful probability distributions, activity I, II and III. Shifted and truncated distributions; Specifying multivariate distribution, correlations, and stochastic processes; Selecting the distribution in the absence of data, Models of arrival process. (6.2, 6.4, 6.5, 6.6, 6.8, 6.10, 6.11, 6.12 of Text).	**L1,L2, l3**
Module -4	
Random Number Generators: Linear congruential Generators, Other kinds, Testing number generators, **Generating the Random Variates**: General approaches, Generating continuous random variates, Generating discrete random variates, Generating random vectors, and correlated random variants, Generating arrival processes (7.2, 7.3, 7.4, 8.2, 8.3, 8.4, 8.5, 8.6 of Text).	**L1,L2, L3**
Module -5	
Output data analysis for a single system: Transient and steady state behavior of a stochastic process; Types of simulations with regard to analysis; Statistical analysis for terminating simulation; Statistical analysis for steady state parameters; Statistical analysis for steady state cycle parameters; Multiple measures of performance, Time plots of important variables. (9.2, 9.3, 9.4, 9.4.1, 9.4.3, 9.5, 9.5.1, 9.5.2, 9.5.3, 9.6, 9.7, 9.8 of Text)	**L1,L2,L3**

Course Outcomes:

After studying this course, students will be able to:

- Define the need of simulation and modeling.
- Describe various simulation models.
- Discuss the process of selecting of probability distributions.
- Perform output data analysis.

Question paper pattern:

- The question paper will have 10 full questions carrying equal marks.
- Each full question consists of 16 marks with a maximum of four sub questions.
- There will be 2 full questions from each module covering all the topics of the module
- The students will have to answer 5 full questions, selecting one full question from each module.

Text Book:

Averill Law, "Simulation modeling and analysis", McGraw Hill 4th edition, 2007.

Reference Books:

1. Tayfur Altiok and Benjamin Melamed, “Simulation modeling and analysis with ARENA”, Elsevier, Academic press, 2007.
2. Jerry Banks, "Discrete event system Simulation", Pearson, 2009
3. Seila Ceric and Tadikamalla, "Applied simulation modeling", Cengage, 2009.
4. George. S. Fishman, "Discrete event simulation", Springer, 2001.
5. Frank L. Severance, "System modeling and simulation", Wiley, 2009.

ADVANCED COMMUNICATION LAB

[As per Choice Based Credit System (CBCS) scheme]

SEMESTER – I

Laboratory Code	16ECSL16	IA Marks	20
Number of Lecture Hours/Week	01Hr Tutorial (Instructions) + 02 Hours Laboratory	Exam Marks	80
		Exam Hours	03

CREDITS – 02

Course objectives: This laboratory course enables students to get practical experience in

- Radiation pattern of antennas.
- Determining gain and directivity of a given antenna.
- Working of Klystron source.
- S-parameters of some microwave passive devices.

Laboratory Experiments: **NOTE:** Experiments can be done using Hardware tools such as Spectrum analyzers, Signal sources, Power Supplies, Oscilloscopes, High frequency signal sources, Fiber optic kits, Microwave measurement benches, DSP processor kit, FPGA kit, Logic analyzers, PC setups, etc. Software tools based experiments can be done using, FEKO or equivalent open source simulator, MATLAB etc.	**Revised Bloom's Taxonomy (RBT) Level**
1. Matlab/C implementation to obtain the radiation pattern of an antenna.	L3,L4
2. Study of radiation pattern of different antennas.	L2, L3
3. Determine the directivity and gains of Horn/ Yagi/ dipole/ Parabolic antennas.	L3,L4
4. Impedance measurements of Horn/Yagi/dipole/Parabolic antennas.	L3,L4
5. Study of radiation pattern of E & H plane horns.	L2, L3
6. Significance of Pocklington's integral equation.	L1,L2
7. Study of digital modulation techniques using CD4051 IC.	L2, L3
8. Conduct an experiment for Voice and data multiplexing using optical fiber.	L3,L4
9. Determination of the modes transit time, electronic timing range and sensitivity of Klystron source.	L3, L4
10. Determination of VI characteristics of GUNN diode, and measurement of guide wave length, frequency, and VSWR.	L3,L4

11. Determination of coupling coefficient and insertion loss of directional couplers and Magic tree.	L3,L4
12. Build a hardware pseudo-random signal source and determine statistics of the generated signal source.	L1,L2,L3,L4

Course outcomes: On the completion of this laboratory course, the students will be able to:

- Plot the radiation pattern of some antennas using Matlab and wave guide setup
- Obtain the S-parameters of Magic tee and directional couplers.
- Test the IC CD4051 for modulation techniques.
- Study multiplexing techniques using OFC kit.

Conduct of Practical Examination:

1. All laboratory experiments are to be included for practical examination.
2. Students are allowed to pick one experiment from the lot.
3. Strictly follow the instructions as printed on the cover page of answer script for breakup of marks.
4. Change of experiment is allowed only once and Marks allotted to the procedure part to be made zero.

ADVANCED DSP

[As per Choice Based Credit System (CBCS) Scheme
SEMESTER – II

Subject Code	16ECS21	IA Marks	20
Number of Lecture Hours/Week	04	Exam marks	80
Total Number of Lecture Hours	50 (10 Hours per Module)	Exam Hours	03

CREDITS – 04

Course objectives: This course will enable students to:

- Understand Multirate digital signal processing principles and its applications.
- Estimate the various spectral components present in the received signal using different spectral estimation methods such as Parametric and Nonparametric.
- Design and implement an optimum adaptive filter using LMS and RLS algorithms.
- Understand the concepts and mathematical representations of Wavelet transforms.

Modules	**RBT Level**
Module 1	
Multirate Digital Signal Processing: Introduction, decimation by a factor 'D', Interpolation by a factor 'I', sampling rate conversion by a factor 'I/D', Implementation of sampling rate conversion, Multistage implementation of sampling rate conversion, Applications of multirate signal processing, Digital filter banks, two channel quadrature mirror filter banks, M-channel QMF bank. (Text 1)	L1,L2,L3
Module 2	
Linear prediction and Optimum Linear Filters: Random signals, Correlation Functions and Power Spectra, Innovations Representation of a Stationary Random Process. Forward and Backward Linear Prediction. Solution of the Normal Equations The Levinson-Durbin Algorithm. Properties of the Linear Prediction-Error Filters. (Text 1)	L1,L2,L3
Module 3	
Adaptive filters: Applications of adaptive filters- Adaptive channel equalization,, Adaptive noise cancellation, Linear Predictive coding of Speech Signals, Adaptive direct form FIR filters-The LMS algorithm, Properties of LMS algorithm. **Adaptive direct form filters-** RLS algorithm. (Text 1)	L1,L2,L3
Module 4	
Power Spectrum Estimation: Non parametric Methods for Power Spectrum Estimation - Bartlett Method, Welch Method, Blackman and Tukey Methods. **Parametric Methods for Power Spectrum Estimation:** Relationship between the auto correlation and the model parameters, Yule and Walker methods for the AR Model Parameters, Burg Method for the AR Model parameters, Unconstrained least-squares method for the AR Model parameters, Sequential estimation methods for the AR Model parameters, ARMA Model for Power Spectrum Estimation. (Text 1)	L1, L2,L3
Module 5	

WAVELET TRANSFORMS: The Age of Wavelets, The origin of Wavelets, Wavelets and other reality transforms, History of wavelets, Wavelets of the future. **Continuous Wavelet and Short Time Fourier Transform:** Wavelet Transform, Mathematical preliminaries, Properties of wavelets. **Discrete Wavelet Transform**: Haar scaling functions, Haar wavelet function, Daubechies Wavelets. (Chapters 1, 3 & 4 of Text 2)	L1,L2,L3

Course Outcomes: After studying this course, students will be able to:

- Design adaptive filters for a given application
- Design multirate DSP Systems
- Implement adaptive signal processing algorithm
- Design active networks
- Understand advanced signal processing techniques, including multi-rate processing and time-frequency analysis techniques

Question paper pattern:

- The question paper will have 10 full questions carrying equal marks.
- Each full question consists of 16 marks with a maximum of four sub questions.
- There will be 2 full questions from each module covering all the topics of the module
- The students will have to answer 5 full questions, selecting one full question from each module.

Text Books:

1. "Digital Signal Processing, Principles, Algorithms and Applications", John G.Proakis, Dimitris G.Manolakis, Fourth edition, Pearson-2007.
2. Insight into Wavelets- from Theory to Practice", K.P Soman, Ramachandran, Resmi- PHI Third Edition-2010.

Reference Books

1. "Modern Digital signal processing", Robert. O. Cristi, Cengage Publishers, India, 2003.
2. "Digital signal processing: A Practitioner's approach", E.C. Ifeachor, and B. W. Jarvis, , Second Edition, Pearson Education, India, 2002, Reprint.
3. "Wavelet Transforms, Introduction to Theory and applications", Raghuveer. M. Rao, Ajit S.Bopardikar, Pearson Education, Asia, 2000.

ERROR CONTROL CODING

[As per Choice Based Credit System (CBCS) Scheme]

SEMESTER – II

Subject Code	16ECS22	IA Marks	20
Number of Lecture Hours/Week	04	Exam marks	80
Total Number of Lecture Hours	50 (10 Hours per Module)	Exam Hours	03

CREDITS – 04

Course objectives: This course will enable students to:

- Understand the concept of the Entropy, information rate and capacity for the Discrete memoryless channel.
- Apply modern algebra and probability theory for the coding.
- Compare Block codes such as Linear Block Codes, Cyclic codes etc and Convolutional codes.
- Detect and correct errors for different data communication and storage systems.
- Implement different Block code encoders and decoders.
- Analyze and implement convolutional encoders and decoders.
- Analyze and apply soft and hard Viterbi algorithm for decoding of convolutional codes.

Modules	**RBT Level**
Module 1	
Information theory: Introduction, Entropy, Source coding theorem, discrete memoryless channel, Mutual Information, Channel Capacity Channel coding theorem.(Chap. 5 of Text 1) **Introduction to algebra**: Groups, Fields, binary field arithmetic, Construction of Galois Fields GF (2^m) and its properties, (Only statements of theorems without proof) Computation using Galois filed GF (2^m) arithmetic, Vector spaces and Matrices. (Chap. 2 of Text 2)	L1,L2,L3
Module 2	
Linear block codes: Generator and parity check matrices, Encoding circuits, Syndrome and error detection, Minimum distance considerations, Error detecting and error correcting capabilities, Standard array and syndrome decoding, Single Parity Check Codes(SPC),Repetition codes, Self dual codes, Hamming codes, Reed-Muller codes. Product codes and Interleaved codes. (Chap. 3 of Text 2)	L1,L2,L3
Module 3	
Cyclic codes: Introduction, Generator and parity check polynomials, Encoding of cyclic codes, Syndrome computing and error detection, Decoding of cyclic codes, Error trapping Decoding, Cyclic hamming codes, Shortened cyclic codes.(Chap. 4 of Text2)	L1,L2,L3
Module 4	
BCH codes: Binary primitive BCH codes, Decoding procedures, Implementation of Galois field arithmetic, Implementation of error correction. (Chap. 6 of Text 2)	

Reed -Solomon codes. (Chap. 7 of Text 2) **Majority Logic decodable codes**: One -step majority logic decoding, One-step majority logic decodable codes, Two-step majority logic, decoding, Multiple-step majority logic. (Chap. 8 of Text 2)	L1,L2,L3
Module 5	
Convolution codes: Convolutional Encoding, Convolutional Encoder Representation, Formulation of the Convolutional Decoding Problem, Properties of Convolutional Codes: Distance property of convolutional codes, Systematic and Nonsystematic Convolutional Codes, Performance Bounds for Convolutional Codes, Coding Gain. Other Convolutional Decoding Algorithms: Sequential Decoding, Feedback Decoding.(Chap. 7 of Text 3)	L1,L2,L3

Course Outcomes: After studying this course, students will be able to:

- Analyse a discrete memoryless channel, given the source and transition probabilities.
- Apply the concept of modern linear algebra for the error control coding technique.
- Construct and Implement efficient LBC, Cyclic codes etc encoder and decoders.
- Apply decoding algorithms for efficient decoding of Block codes and Convolutional codes.

Question paper pattern:

- The question paper will have 10 full questions carrying equal marks.
- Each full question consists of 16 marks with a maximum of four sub questions.
- There will be 2 full questions from each module covering all the topics of the module
- The students will have to answer 5 full questions, selecting one full question from each module.

Text Books:

1. Simon Haykin, ”Digital Communication systems”, First edition, Wiley India Private. Ltd, 2014. ISBN 978-81-265-4231-4
2. Shu Lin and Daniel J. Costello. Jr, "Error control coding", Pearson, Prentice Hall, 2nd edition, 2004.
3. Bernard Sklar, ”Digital Communications - Fundamentals and Applications”, 2nd Edition Pearson Education (Asia) Ptv. Ltd, 2001.

Reference Books:

1. Blahut. R. E, "Theory and practice of error control codes", Addison Wesley, 1984.
2. Salvatore Gravano, “Introduction to Error control coding”, Oxford university press,2007.

WIRELESS COMMUNICATION

[As per Choice Based Credit System (CBCS) Scheme]

SEMESTER – II

Subject Code	16ECS23	IA Marks	20
Number of Lecture Hours/Week	04	Exam marks	80
Total Number of Lecture Hours	50 (10 Hours per Module)	Exam Hours	03

CREDITS – 04

Course objectives: This course will enable students to:

- Characterize small-scale fading in terms of Doppler spectrum, coherence time, power delay profile, and coherence bandwidth.
- Apply mathematical models of radio wave propagation.
- Analyze the error probabilities for common modulation schemes.
- Describe different types of diversity and how they improve performance for mobile radio channels.
- Analyze the AWGN channel capacity.

Modules	**RBT Level**
Module 1	
The Wireless channel: Physical modeling for wireless channels, Input/output model of wireless channels, Time and frequency response, Statistical models. (Text 1)	L1,L2,L3
Module 2	
Point-to-Point Communication, Detection diversity and channel uncertainty: Detection in Rayleigh fading channels, Time diversity, Antenna diversity, Frequency diversity, Impact of the channel uncertainty. (Text 1)	L1,L2,L3
Module 3	
Diversity: Introduction Micro-diversity, Micro-diversity and Simulcast combination of signals, Error probability in fading channels with diversity reception, Transmit diversity. (Chap. 13 of Text2)	L1,L2,L3
Module 4	
Capacity of wireless channel: AWGN channel capacity, Resources of AWGN channel, Linear time invariant Gaussian channel, Capacity of fading channels. (Text 1)	L1,L2,L3
Module 5	
MIMO Systems: Introduction, Space diversity and system based on space diversity, Smart antenna systems and MIMO, MIMO based system architecture; MIMO exploits multipath, Space time processing, Antenna considerations for MIMO. MIMO channel modeling, MIMO channel measurements, MIMO channel capacity, CDD, Space time coding, advantages and applications of MIMO, MIMO application in 3G.(Chap. 15 of Text 3)	L1,L2,L3

Course Outcomes: After studying this course, students will be able to:

- Acquire knowledge of characteristics of mobile/wireless communication channels
- Apply statistical models of multipath fading
- Understand the multiple radio access techniques

- Understand the need of coding, diversity, interleaving and link techniques for mo bile/wireless communications network
- Design receiver and transmitter diversity techniques
- Identify and describe modern techniques for high-rate wireless communications, using MIMO transmission

Question paper pattern:

- The question paper will have 10 full questions carrying equal marks.
- Each full question consists of 16 marks with a maximum of four sub questions.
- There will be 2 full questions from each module covering all the topics of the module
- The students will have to answer 5 full questions, selecting one full question from each module.

Text Books:

1. David Tse, P. Vishwanath, “Fundamentals of Wireless Communication”, Cambridge University press, 2006.
2. Andreas F.Molisch “Wireless Communications” 2nd Edition John Wiley & Sons.
3. Upena Dalal, “Wireless communication”, Oxford, 2009.

Reference Book:

Ke-Lin Du, ad M.N.S. Swamy, "Wireless communication systems-From RF subsystems to 4G enabling Technologies", Cambridge.

RF AND MICROWAVE CIRCUIT DESIGN

[As per Choice Based Credit System (CBCS) Scheme]

SEMESTER – II

Subject Code	16ECS24	IA Marks	20
Number of Lecture Hours/Week	04	Exam marks	80
Total Number of Lecture Hours	50 (10 Hours per Module)	Exam Hours	03

CREDITS – 04

Course Objectives: This course will enable students to

- Understand waves propagating in Networks.
- Use the Smith Chart for various applications.
- Understand the basic considerations in active networks
- Design active networks.
- Understand RF/MW Frequency Mixer and Phase Shifter Design

Modules	**RBT Level**
Module 1	
Wave propagation in networks: Introduction, Reasons for Using RF/Microwaves, Applications, RF Waves, RF and Microwave circuit design, Introduction to Components Basics, Analysis of Simple Circuit in Phasor Domain, RF Impedance Matching, Transmission Media, High Frequency Parameters, Formulation of S-parameters, Properties of S-Parameters, Transmission Matrix, Generalized S-parameters.	L1,L2
Module 2	
Smith chart and its Applications: Introduction, Smith Chart, Derivation of Smith Chart, Smith Chart Circular and Radial Scales, Application of Smith chart.	L1,L2
Module 3	
Basic consideration in active networks: Stability Considerations, Gain Considerations and Noise Considerations.	L1,L2
Module 4	
RF/Microwave Amplifiers: Small Signal Design: Introduction, Types of amplifier, Design of different types of amplifiers **RF/Microwave Frequency Conversion: Mixers**: Introduction, Mixer Types, Conversion Losses for SSB Mixers, SSB versus DSB mixers, One diode mixers, Two diode Mixers.	L1,L2,L3
Module 5	
RF/Microwave Control Circuit Design: Introduction, PN Junction Devices, Phase shifters, Digital phase shifters, Semiconductor phase shifters, PIN diode attenuators. **RF and Microwave IC design**: MICs, MIC materials, Types of MICs, Hybrid verses Monolithic ICs, Chip mathematics	L1,L2,L3

Course Outcomes: After studying this course, students will be able to:

- Discuss and analyse waves propagation in Networks

- Apply the Smith Chart for finding various parameters in transmission lines
- Analyse the basic considerations in active networks
- Describe and design active networks
- Design RF/MW Frequency Mixers and phase shifters

Question paper pattern:

- The question paper will have 10 full questions carrying equal marks.
- Each full question consists of 16 marks with a maximum of four sub questions.
- There will be 2 full questions from each module covering all the topics of the module
- The students will have to answer 5 full questions, selecting one full question from each module.

Text Book:

Matthew M. Radmanesh, "RF and Microwave Electronics Illustrated", Pearson Education edition, 2004.

Reference Book:

Reinhold Ludwig, and Pavel Bretchko, "RF circuit design theory and applications", Pearson Education edition, 2004.

AUTOMOTIVE ELECTRONICS [As per Choice Based credit System (CBCS) Scheme SEMESTER – II			
Subject Code	16ELD251	IA Marks	20
Number of Lecture Hours/Week	03	Exam marks	80
Total Number of Lecture Hours	40 (8 Hours per Module)	Exam Hours	03
CREDITS – 03			

Course Objectives: This course will enable students to:

- Understand the complete dynamics of automotive electronics
- Design and implement the electronics that attributes the smartness to the automobiles by way of unprecedented safety, add-on features, and comforts.

Modules	**RBT Level**
Module 1	
Automotive Fundamentals, the Systems Approach to Control and Instrumentation: Use Of Electronics In The Automobile, Antilock Brake Systems, (ABS), Electronic steering control, Power steering, Traction control, Electronically controlled suspension. (Chap.1 and 2 of Text)	L1,L2
Module 2	
Automotive instrumentation Control: Sampling, Measurement and signal conversion of various parameters. (Chap. 4 of Text)	L1,L2, L3
Module 3	
The basics of Electronic Engine control: Integrated body: Climate controls, Motivation for Electronic Engine Control, Concept of An Electronic Engine Control System, Definition of General Terms, Definition of Engine Performance Terms, Electronic fuel control system, Engine control sequence, Electronic Ignition, Sensors and Actuators, Applications of sensors and actuators, air flow rate sensor, Indirect measurement of mass air flow, Engine crankshaft angular position sensor, Automotive engine control actuators, Digital engine control, Engine speed sensor ,Timing sensor for ignition and fuel delivery, Electronic ignition control systems, Safety systems, Interior safety, Lighting, Entertainment systems. (Chap. 5 and 6 of Text)	L1,L2,L3
Module 4	

Vehicle Motion Control and Automotive diagnostics: Cruise control system, Digital cruise control, Timing light, Engine analyzer, On-board and off-board diagnostics, Expert systems. Stepper motor-based actuator, Cruise control electronics, Vacuum - antilock braking system, Electronic suspension system Electronic steering control, Computer-based instrumentation system, Sampling and Input\output signal conversion, Fuel quantity measurement, Coolant temperature measurement, Oil pressure measurement, Vehicle speed measurement, Display devices, Trip-Information-Computer, Occupant protection systems. (Chap. 8 and 10 of Text)	L1,L2, L3
Module 5	
Future automotive electronic systems: Alternative Fuel Engines, Collision Wide Range Air/Fuel Sensor, Alternative Engine, Low Tire Pressure Warning System, Collision avoidance Radar Warning Systems, Low Tire Pressure Warning System, Radio Navigation, Advance Driver information System. Alternative-Fuel Engines , Transmission Control , Collision Avoidance Radar Warning System, Low Tire Pressure Warning System, Speech Synthesis Multiplexing in Automobiles, Control Signal Multiplexing, Navigation Sensors, Radio Navigation, Sign post Navigation , Dead Reckoning Navigation Future Technology, Voice Recognition Cell Phone Dialing Advanced Driver information System, Automatic Driving Control. (Chap. 11 of Text)	L1,L2, L3

Course Outcomes: After studying this course, students will be able to:

- Understand and implement various control requirements in the automotive system.
- Comprehend dashboard electronics and engine system electronics.
- Identify various physical parameters that are to be sensed and monitored for maintaining the stability of the vehicle under dynamic conditions.
- Understand and implement the controls and actuator system pertaining to the comfort and safety of commuters.
- Design and implement sensor network for mechanical fault diagnostics in an automotive vehicle.

Question paper pattern:

- The question paper will have 10 full questions carrying equal marks.
- Each full question consists of 16 marks with a maximum of four sub questions.
- There will be 2 full questions from each module covering all the topics of the module
- The students will have to answer 5 full questions, selecting one full question from each module.

Text Book:

William B. Ribbens , "Understanding Automotive Electronics", SAMS/Elsevier publishing, 6th Edition, 1997.

Reference Book:

Robert Bosch Gmbh, "Automotive Electrics and Automotive Electronics-Systems and Components, Networking and Hybrid Drive", Springer Vieweg, 5th Edition, 2007.

MULTIMEDIA OVER COMMUNICATION LINKS

[As per Choice Based credit System (CBCS) Scheme

SEMESTER – II

Subject Code	16ECS252	IA Marks	20
Number of Lecture Hours/Week	03	Exam marks	80
Total Number of Lecture Hours	40 (8 Hours per Module)	Exam Hours	03

CREDITS – 03

Course Objectives: This course will enable students to:

- Gain fundamental knowledge in understanding the basics of different multimedia networks, applications, media types like text and image.
- Analyse media types like audio and video and gain knowledge on multimedia systems.
- Analyse Audio compression techniques required to compress Audio.
- Analyse compression techniques required to compress video.
- Gain fundamental knowledge about the Multimedia Communications in different Networks.

Modules	**RBT Level**
Module 1	
Multimedia Communications: Introduction, Multimedia information representation, multimedia networks, multimedia applications, Application and networking terminology.(Chap. 1 of Text1) **Information Representation**: Introduction, Text, Images. (Chap. 2- Sections 2.2 and 2.3 of Text 1)	L1, L2, L3
Module 2	
Information Representation: Audio and Video. (Chap. 2 - Sections 2.4 and 2.5 of Text 1) **Distributed multimedia systems**: Introduction, main Features of a DMS, Resource management of DMS, Networking, Multimedia operating systems. (Chap. 4 - Sections 4.1 to 4.5 of Text 2)	L1,L2, L3
Module 3	
Multimedia Processing in Communication: Introduction, Perceptual coding of digital Audio signals, Transform Audio Coders, Audio Sub band Coders. (Chap. 3 - Sections 3.1, 3.2, 3.6, 3.7 of Text 2)	L1,L2, L3
Module 4	
Multimedia Communication Standards: Introduction, MPEG approach to multimedia standardization, MPEG-1, MPEG-2, Overview of MPEG-4. (Chap. 5 - Sections 5.1 to 5.4 and 5.5.1 of Text 2)	L1,L2, L3
Module 5	
Multimedia Communication Across Networks: Packet audio/video in the network environment, Video transport across generic networks, Multimedia Transport across ATM Networks.	L1,L2, L3

(Chap. 6 - Sections 6.1, 6.2, 6.3 of Text 2)	

Course Outcomes: After studying this course, students will be able to:

- Understand basics of different multimedia networks and applications.
- Analyze media types like audio and video to represent in digital form.
- Understand different compression techniques to compress audio.
- Understand different compression techniques to compress audio video.
- Describe the basics of Multimedia Communication Across Networks

Question paper pattern:

- The question paper will have 10 full questions carrying equal marks.
- Each full question consists of 16 marks with a maximum of four sub questions.
- There will be 2 full questions from each module covering all the topics of the module
- The students will have to answer 5 full questions, selecting one full question from each module.

Text Books:

1. Fred Halsall, “Multimedia Communications”, Pearson education, 2001, ISBN -9788131709948.
2. K. R. Rao, Zoran S. Bojkovic, Dragorad A. Milovanovic, “Multimedia Communication Systems”, Pearson education, 2004. ISBN - 9788120321458.

Reference Book:

Raif steinmetz, Klara Nahrstedt, “Multimedia: Computing, Communications and Applications”, Pearson education, 2002, ISBN -9788177584417.

MICRO ELECTRO MECHANICAL SYSTEMS

[As per Choice Based credit System (CBCS) Scheme]

SEMESTER – II

Subject Code	16ELD253	IA Marks	20
Number of Lecture Hours/Week	03	Exam marks	80
Total Number of Lecture Hours	40 (8 Hours per Module)	Exam Hours	03

CREDITS – 03

Course Objectives: This course will enable students to:

- Understand overview of microsystems, their fabrication and application areas.
- Working principles of several MEMS devices.
- Develop mathematical and analytical models of MEMS devices
- Know methods to fabricate MEMS devices
- Various application areas where MEMS devices can be used.

Modules	**RBT Level**
Module 1	
Overview of MEMS and Microsystems: MEMS and Microsystem, Typical MEMS and Microsystems Products, Evolution of Microfabrication, Microsystems and Microelectronics, Multidisciplinary Nature of Microsystems, Miniaturization. Applications and Markets.	L1, L2
Module 2	
Working Principles of Microsystems: Introduction, Microsensors, Microactuation, MEMS with Microactuators, Microaccelerometers, Microfluidics. Engineering Science for Microsystems Design and Fabrication. Introduction, Atomic Structure of Matters, Ions and Ionization, Molecular Theory of Matter and Inter-molecular Forces, Doping of Semiconductors, The Diffusion Process, Plasma Physics, Electrochemistry.	L1, L2
Module 3	
Engineering Mechanics for Microsystems Design: Introduction, Static Bending of Thin Plates, Mechanical Vibration, Thermomechanics, Fracture Mechanics, Thin Film Mechanics, Overview on Finite Element Stress Analysis.	L1,L2, L3
Module 4	
Scaling Laws in Miniaturization: Introduction, Scaling in Geometry, Scaling in Rigid-Body Dynamics, Scaling in Electrostatic Forces, Scaling of Electromagnetic Forces, Scaling in Electricity, Scaling in Fluid Mechanics, Scaling in Heat Transfer.	L1,L2, L3
Module 5	
Overview of Micromanufacturing: Introduction, Bulk Micromanufacturing, Surface Micromachining, The LIGA Process, Summary on Micromanufacturing.	L1,L2, L3

Microsystem Design: Introduction, Design Considerations, Process Design, Mechanical Design, Using Finite Element Method.	

Course Outcomes: After studying this course, students will be able to:

- Appreciate the technologies related to Micro Electro Mechanical Systems.
- Understand design and fabrication processes involved with MEMS devices.
- Analyze the MEMS devices and develop suitable mathematical models
- Know various application areas for MEMS device

Question paper pattern:

- The question paper will have 10 full questions carrying equal marks.
- Each full question consists of 16 marks with a maximum of four sub questions.
- There will be 2 full questions from each module covering all the topics of the module
- The students will have to answer 5 full questions, selecting one full question from each module.

Text Book:

1. Tai-Ran Hsu, MEMS and Micro systems: Design, Manufacture and Nanoscale Engineering, 2nd Ed, Wiley.

Reference Books:

1. Hans H. Gatzen, Volker Saile, Jurg Leuthold, Micro and Nano Fabrication: Tools and Processes, Springer, 2015.
2. Dilip Kumar Bhattacharya, Brajesh Kumar Kaushik, Microelectromechanical Systems (MEMS), Cenage Learning.

CRYPTOGRAPHY AND NETWORK SECURITY

[As per Choice Based credit System (CBCS) Scheme

SEMESTER – II

Subject Code	16ECS254	IA Marks	20
Number of Lecture Hours/Week	03	Exam marks	80
Total Number of Lecture Hours	40 (8 Hours per Module)	Exam Hours	03

CREDITS – 03

Course Objectives: This course will enable students to:

- Understand the basics of symmetric key and public key cryptography.
- Understand some basic mathematical concepts and pseudorandom number generators required for cryptography.
- Authenticate and protect the encrypted data.
- Enrich knowledge about Email, IP and Web security.

Modules	**RBT Level**
Module 1	
Foundations: Terminology, Steganography, substitution ciphers and transpositions ciphers, Simple XOR, One-Time Pads, Computer Algorithms (Text 2: Chapter 1: Section 1.1 to 1.6) **SYMMETRIC CIPHERS:** Traditional Block Cipher structure, Data encryption standard (DES), The AES Cipher. (Text 1: Chapter 2: Section2.1, 2.2, Chapter 4)	L1,L2,L3
Module 2	
Introduction to modular arithmetic, Prime Numbers, Fermat's and Euler's theorem, primality testing, Chinese Remainder theorem, discrete logarithm. (Text 1: Chapter 7: Section 1, 2, 3, 4, 5) Principles of Public-Key Cryptosystems, The RSA algorithm, Diffie - Hellman Key Exchange, Elliptic Curve Arithmetic, Elliptic Curve Cryptography (Text 1: Chapter 8, Chapter 9: Section 9.1, 9.3, 9.4)	L1,L2,L3
Module 3	
Pseudo-Random-Sequence Generators and Stream Ciphers: Linear Congruential Generators, Linear Feedback Shift Registers, Design and analysis of stream ciphers, Stream ciphers using LFSRs, A5, Hughes XPD/KPD, Nanoteq, Rambutan, Additive generators, Gifford, Algorithm M, PKZIP (Text 2: Chapter 16)	L1,L2, L3
Module 4	
One-Way Hash Functions: Background, Snefru, N-Hash, MD4, MD5, Secure Hash Algorithm [SHA],One way hash functions using symmetric block algorithms, Using public key algorithms, Choosing a one-way hash functions, Message Authentication Codes. Digital Signature Algorithm, Discrete Logarithm Signature Scheme (Text 2: Chapter 18: Section 18.1 to 18.5, 18.7, 18.11 to 18.14 and Chapter 20: Section 20.1, 20.4)	L1,L2,L3
Module 5	
E-mail Security: Pretty Good Privacy-S/MIME (Text 1: Chapter 17: Section 17.1, 17.2).	L1,L2, L3

IP Security: IP Security Overview, IP Security Policy, Encapsulation Security Payload (ESP), Combining security Associations. (Text 1: Chapter 18: Section 18.1 to 18.4). **Web Security:** Web Security Considerations, SSL (Text 1: Chapter 15: Section 15.1, 15.2).	

Course Outcomes: After studying this course, students will be able to:

- Use basic cryptographic algorithms to encrypt the data.
- Generate some pseudorandom numbers required for cryptographic applications.
- Provide authentication and protection for encrypted data.

Question paper pattern:

- The question paper will have 10 full questions carrying equal marks.
- Each full question consists of 16 marks with a maximum of four sub questions.
- There will be 2 full questions from each module covering all the topics of the module
- The students will have to answer 5 full questions, selecting one full question from each module.

Text Books:

1. William Stallings , "Cryptography and Network Security Principles and Practice", Pearson Education Inc., 6th Edition, 2014, ISBN: 978-93-325-1877-3

2. Bruce Schneier, "Applied Cryptography Protocols, Algorithms, and Source code in C", Wiley Publications, 2nd Edition, ISBN: 9971-51-348-X

Reference Books:

1. Cryptography and Network Security, Behrouz A. Forouzan, TMH, 2007.
2. Cryptography and Network Security, Atul Kahate, TMH, 2003.

ADVANCED DSP LAB

[As per Choice Based Credit System (CBCS) scheme]

SEMESTER – II

Laboratory Code	16ECSL26	IA Marks	20
Number of Lecture Hours/Week	01Hr Tutorial (Instructions) + 02 Hours Laboratory	Exam Marks	80
		Exam Hours	03

CREDITS – 02

Course objectives: This laboratory course enables students to get practical experience

- Matlab implementation of LTI systems and multirate systems
- Realization of some systems using DSP 6713 processor

Laboratory Experiments:	**RBT Level**
PART-A: Experiments to be done using MATLAB	
1. Computation of Linear convolution, Circular convolution, Linear convolution using circular convolution	L1,L2, L3
2. Computation of DFT, IDFT, Circular convolution in frequency domain	
3. Comparison of DFT and DCT (in terms of energy compactness) Generate the sequence x[n]=n-64 for n=0, ...127. (a) Let X[k] = DFT{x[n]}. For various values of l, set to zero "high frequency coefficients" X[64-l]= ....X[64]= .....X[64+L]=0 and take the inverse DFT. Plot the results. (b) Let XDCT[k]=DCT(X[n]). For the same values of L, set to zero "high frequency coefficient" XDCT [127-L]= ....XDCT[127]. Take the inverse DCT for each case and compare the reconstruction with the previous case.	
4. Determination of power spectrum density of a given sequence	
5. Generation of DTMF Signals	
6. Implementation of Decimation Process and Implementation of Interpolation Process	
7. Time-Frequency Analysis with the Continuous Wavelet Transform	

8. Signal Reconstruction from Continuous Wavelet Transform Coefficients	
9.Denoising Signals and Images	
10.Haar Wavelet Image Compression	
PART-B: Experiments to be done using the DSP processor	
1. Write an ALP to obtain the response of a system using linear convolution whose input and impulse response are specified.	L1,L2, L3
2. Write an ALP to obtain the impulse response of the given system, given the difference equation.	
3. Computation of FFT when N is not a power of 2.	
4. Synthesis of Dual Tone Multi Frequency using 6713 processor	

Course outcomes: On the completion of this laboratory course, the students will be able to:

1. Realize the following using Matlab
   - Response of LTI systems.
   - DFT and DCT
   - Decimation
   - Wavelet Transforms
2. Implement the following using 6713 processor
   - Response of LTI systems and convolution.
   - FFT realization and DTMF generation.

Conduct of Practical Examination:

1. All laboratory experiments are to be included for practical examination.
2. One experiment from the Part-A Matlab part and one experiment from the Part-B Hardware part to be set for the examination.
3. Strictly follow the instructions as printed on the cover page of answer script for breakup of marks.
4. Change of experiment is allowed only once and Marks allotted to the Procedure part will be made zero.

M.Tech Commn. Stream-2016-FOURTH SEMESTER SYLLABUS

Wireless Broadband LTE 4G [As per Choice Based Credit System (CBCS) scheme] SEMESTER – IV			
Subject Code	16ECS41	IA Marks	20
Number of Lecture Hours/Week	04	Exam Marks	80
Total Number of Lecture Hours	50 (10 Hrs per Module)	Exam Hours	03
CREDITS – 04			

Course objectives: This course will enable students to:

- Explain the system architecture of LTE and E-UTRAN as per the standards
- Understand the Multiple Access process incorporated in the radio physical layer.
- Associate MAC of LTE radio interface protocols to set up, reconfigure and release the Radio Bearer and for transferring to the EPS bearer.
- Explain the mobility principles and procedures in the idle and active state.
- Analyse the main factors affecting LTE performance including mobile speed and transmission bandwidth.

Modules	**RBT Level**
Module -1	
LTE Standardization Phases, Evolution Beyond Release 8, LTE-Advanced for IMT-Advanced, LTE Specifications and 3GPP Structure. **System Architecture Based on 3GPP SAE:** Basic System Architecture Configuration with only E-UTRAN Access Network, System Architecture with E-UTRAN and Legacy 3GPP Access Networks, System Architecture with E-UTRAN and Non-3GPP Access Networks, Architecture Configuration, IMS Architecture, PCC and QoS.	**L2, L3**
Module -2	
Introduction to OFDMA, SC-FDMA and MIMO in LTE: LTE Multiple Access Background, OFDMA Basics, SC-FDMA Basics MIMO Basics. **Physical Layer:** Transport Channels and their Mapping to the Physical Channels, Modulation, Uplink User Data Transmission, Downlink User Data Transmission, Uplink Physical Layer Signaling Transmission, PRACH Structure, Downlink Physical Layer Signaling Transmission.	**L2, L3**
Module -3	

Physical Layer Procedures, UE Capability Classes and Supported Features Physical Layer Measurements, Physical Layer Parameter Configuration. **LTE Radio Protocols:** Protocol Architecture, The Medium Access Control The Radio Link Control Layer, Packet Data Convergence Protocol.	**L1, L2, L3**
Module -4	
Radio Resource Control (RRC): X2 Interface Protocols Understanding the RRC ASN.1 Protocol Definition, Early UE Handling in LTE. **Mobility:** Mobility Management in Idle State, Intra-LTE Handovers 190, Inter-system Handovers Differences in E-UTRAN and UTRAN Mobility.	**L2, L3**
Module -5	
Radio Resource Management: Overview of RRM Algorithms, Admission Control and QoS Parameters, Downlink Dynamic Scheduling and Link Adaptation, Uplink Dynamic Scheduling and Link Adaptation, Interference Management and Power Settings, Discontinuous Transmission and Reception (DTX/DRX), RRC Connection Maintenance. **Performance:** Layer 1 Peak Bit Rates, Terminal Categories Link Level Performance, Link Budgets Spectral Efficiency Latency, LTE Reframing to GSM Spectrum Dimensioning, Capacity Management Examples from HSPA Networks.	**L1, L2, L3**

Course outcomes:

- Understand the system architecture and the function standard specified components of the system of LTE 4G.
- Analyze the role of LTE radio interface protocols and EPS Data convergence protocols to set up, reconfigure and release data and voice from a number of users.
- Demonstrate the UTRAN and EPS handling processes from set up to release including mobility management for a variety of data call scenarios.
- Test and Evaluate the Performance of resource management and packet data processing and transport algorithms.

Question paper pattern:

- The question paper will have 10 full questions carrying equal marks.
- Each full question consists of 16 marks with a maximum of four sub questions.
- There will be 2 full questions from each module covering all the topics of the module
- The students will have to answer 5 full questions, selecting one full question from each module.

Text Book:

'LTE for UMTS Evolution to LTE-Advanced' Harri Holma and Antti Toskala, Second Edition - Wiley India ISBN-978-81-265-7293-9, 2018 / Wiley ISBN: 9780470660003, 2011.

Reference Books:

1. 'Fundamentals of LTE', by Arunabha Ghosh, Jun Zhang, Jeffrey G. Andrews), Rias Muhamed, 1st Edition, Sept 2010, Prentice Hall Communications Engineering and Emerging Technologies Series from Ted Rappaport,ISBN13: 9780137033119, ISBN10: 0137033117.
2. ' EVOLVED PACKET SYSTEM (EPS) ; THE LTE AND SAE EVOLUTION OF 3G UMTS' by Pierre Lescuyer and Thierry Lucidarme, 2008, John Wiley & Sons, Ltd. Print ISBN:978-0-470-05976-0.
3. ' LTE – The UMTS Long Term Evolution ; From Theory to Practice' by Stefania Sesia, Issam Toufik, and Matthew Baker, 2009 John Wiley & Sons Ltd, ISBN 978-0-470-69716-0.

CMOS RF Circuit Design

[As per Choice Based credit System (CBCS) Scheme
SEMESTER – IV

Subject Code	16EVE421	IA Marks	20
Number of Lecture Hours/Week	03	Exam marks	80
Total Number of Lecture Hours	40 (8 Hours per Module)	Exam Hours	03

CREDITS – 03

Course Objectives: This course will enable students to:

- Learn basic concepts in RF and microwave design emphasising the effects of nonlinearity and noise.
- Able to appreciate communication system, multiple access and wireless standards necessary for RF circuit design.
- Able to deal with transceiver architecture, various receiver and transmitter designs, their merits and demerits
- Understand the design of RF building blocks such as Low Noise Amplifiers and Mixers

Modules	**RBT Level**
Module 1	
Introduction to RF Design and Wireless Technology: **Basic concepts in RF design(I):** General considerations, Effects of Nonlinearity, Noise, Sensitivity and dynamic range	L1,L2,L3
Module 2	
Basic concepts in RF design (II): Passive impedance transformation, scattering parameters, analysis of nonlinear dynamic systems	L1,L2,L3
Module 3	
Communication Concepts: General concepts, analog modulation, digital modulation, spectral re-growth, Mobile RF communications, Multiple access techniques, Wireless standards	L1,L2,L3
Module 4	
Transceiver Architecture (I): General considerations, Receiver architecture	L1,L2,L3
Module 5	
Transceiver Architecture (II): Transmitter architectures **Low Noise Amplifiers:** LNA topologies: common-source stage with inductive load, common-source stage with resistive feedback. **Mixers:** General considerations, passive down conversion mixers.	L1,L2,L3

Course Outcomes: After studying this course, students will be able to:

- Analyse the effect of nonlinearity and noise in RF and microwave design.
- Exemplify the approaches taken in actual RF products.
- Minimize the number of off-chip components required to design mixers and Low-Noise Amplifiers.

- Explain various receivers and transmitter topologies with their merits and drawbacks.
- Demonstrate how the system requirements define the parameters of the circuits and how the performance of each circuit impacts that of the overall transceiver.

Question paper pattern:

- The question paper will have 10 full questions carrying equal marks.
- Each full question consists of 16 marks with a maximum of four sub questions.
- There will be 2 full questions from each module covering all the topics of the module
- The students will have to answer 5 full questions, selecting one full question from each module.

Text Book:

B. Razavi, "**RF Microelectronics**", PHI, second edition.

Reference Books:

1. R. Jacob Baker, H.W. Li, D.E. Boyce "**CMOS Circuit Design, layout and Simulation**", PHI 1998.
2. Thomas H. Lee "**Design of CMOS RF Integrated Circuits**" Cambridge University press 1998.
3. Y.P. Tsividis, "**Mixed Analog and Digital Devices and Technology**", TMH 1996

Advances in Image Processing

[As per Choice Based credit System (CBCS) Scheme

SEMESTER – IV

Subject Code	16ECS422	IA Marks	20
Number of Lecture Hours/Week	03	Exam marks	80
Total Number of Lecture Hours	40 (8 Hours per Module)	Exam Hours	03

CREDITS – 03

Course Objectives: This course will enable students to:

- Acquire fundamental knowledge in understanding the representation of the digital image and its properties
- Equip with some pre-processing techniques required to enhance the image for further analysis purpose.
- Select the region of interest in the image using segmentation techniques.
- Represent the image based on its shape and edge information.
- Describe the objects present in the image based on its properties and structure.

Modules	**RBT Level**
Module 1	
The image, its representations and properties: Image representations a few concepts, Image digitization, Digital image properties, Color images.	L1
Module 2	
Image Pre-processing: Pixel brightness transformations, geometric transformations, local pre-processing.	L1, L2
Module 3	
Segmentation: Thresholding; Edge-based segmentation – Edge image thresholding, Edge relaxation, Border tracing, Hough transforms; Region – based segmentation – Region merging, Region splitting, Splitting and merging, Watershed segmentation, Region growing post-processing.	L1, L2, L3
Module 4	
Shape representation and description: Region identification; Contour-based shape representation and description – Chain codes, Simple geometric border representation, Fourier transforms of boundaries, Boundary description using segment sequences, B-spline representation; Region-based shape representation and description – Simple scalar region descriptors, Moments, Convex hull.	L1, L2, L3
Module 5	
Mathematical Morphology: Basic morphological concepts, Four morphological principles, Binary dilation and erosion, Skeletons and object marking, Morphological segmentations and watersheds.	L1, L2, L3

Course Outcomes: After studying this course, students will be able to:

- Understand the representation of the digital image and its properties
- Apply pre-processing techniques required to enhance the image for its further analysis.
- Use segmentation techniques to select the region of interest in the image for analysis
- Represent the image based on its shape and edge information.
- Describe the objects present in the image based on its properties and structure.
- Use morphological operations to simplify images, and quantify and preserve the main shape characteristics of the objects.

Question paper pattern:

- The question paper will have 10 full questions carrying equal marks.
- Each full question consists of 16 marks with a maximum of four sub questions.
- There will be 2 full questions from each module covering all the topics of the module
- The students will have to answer 5 full questions, selecting one full question from each module.

Text Book:

Milan Sonka, Vaclav Hlavac, Roger Boyle, "Image Processing, Analysis, and Machine Vision", Cengage Learning, 2013, ISBN: 978-81-315-1883-0.

Reference Books:

1. Geoff Doughertry, Digital Image Processing for Medical Applications, Cambridge university Press, 2010
2. S.Jayaraman, S Esakkirajan, T.Veerakumar, Digital Image Processing, Tata McGraw Hill, 2011

Communication System Design using DSP Algorithms

[As per Choice Based credit System (CBCS) Scheme
SEMESTER – IV

Subject Code	16ECS423	IA Marks		20
Number of Lecture Hours/Week	03	Exam marks		80
Total Number of Lecture Hours	40 (8 Hours per Module)	Exam Hours		03

CREDITS – 03

Course Objectives: This course will enable students to:

- Understand communication systems, including algorithms that are particularly suited to DSP implementation.
- Understand Software and hardware tools, as well as FIR and IIR digital filters and the FFT.
- Discuss modulators and demodulators for classical analog modulation methods such as amplitude modulation (AM), double-sideband suppressed-carrier amplitude modulation (DSBSC-AM), single sideband modulation (SSB), and frequency modulation (FM).
- Explore digital communication methods leading to the implementation of a telephone-line modem.

Modules	RBT Level
Module 1	
Introduction to the course: Digital filters, Discrete time convolution and frequency responses, FIR filters - Using circular buffers to implement FIR filters in C and using DSP hardware, Interfacing C and assembly functions, Linear assembly code and the assembly optimizer. IIR filters - realization and implementation, FFT and power spectrum estimation: DTFT window function, DFT and IDFT, FFT, Using FFT to implement power spectrum.	**L1,L2**
Module 2	
Analog modulation scheme: Amplitude Modulation - Theory, generation and demodulation of AM, Spectrum of AM signal. Envelope detection and square law detection. Hilbert transform and complex envelope, DSP implementation of amplitude modulation and demodulation. **DSBSC:** Theory generation of DSBSC, Demodulation, and demodulation using coherent detection and Costas loop. Implementation of DSBSC using DSP hardware. **SSB:** Theory, SSB modulators, Coherent demodulator, Frequency translation, Implementation using DSP hardware. (Text 1, 2)	**L1,L2**
Module 3	
Frequency modulation: Theory, Single tone FM, Narrow band FM, FM bandwidth, FM demodulation, Discrimination and PLL methods, Implementation using DSP hardware. **Digital Modulation scheme:** PRBS, and data scramblers: Generation	**L1,L2**

of PRBS, Self -synchronizing data scramblers, Implementation of PRBS and data scramblers. RS-232C protocol and BER tester: The protocol, error rate for binary signaling on the Gaussian noise channels, Three bit error rate tester and implementation.	
Module 4	
PAM and QAM: PAM theory, baseband pulse shaping and ISI, Implementation of transmit filter and interpolation filter bank. Simulation and theoretical exercises for PAM, Hardware exercises for PAM. **QAM fundamentals:** Basic QAM transmitter, 2 constellation examples, QAM structures using passband shaping filters, Ideal QAM demodulation, QAM experiment. QAM receivers-Clock recovery and other frontend sub-systems. Equalizers and carrier recovery systems.	**L2,L3**
Module 5	
Experiment for QAM receiver frontend. Adaptive equalizer, Phase splitting, Fractionally spaced equalizer. Decision directed carrier tracking, Blind equalization, Complex cross coupled equalizer and carrier tracking experiment. Echo cancellation for full duplex modems: Multicarrier modulation, ADSL architecture, Components of simplified ADSL transmitter, A simplified ADSL receiver, Implementing simple ADSL Transmitter and Receiver.	**L2,L3**

Course outcomes: After studying this course, students will be able to:

- Implement DSP algorithms on TI DSP processors
- Implement FIR, IIR digital filtering and FFT methods
- Implement modulators and demodulators for AM,DSBSC-AM,SSB and FM
- Design digital communication methods leading to the implementation of a line communication system.

Question paper pattern:

- The question paper will have 10 full questions carrying equal marks.
- Each full question consists of 16 marks with a maximum of four sub questions.
- There will be 2 full questions from each module covering all the topics of the module
- The students will have to answer 5 full questions, selecting one full question from each module.

Text Book:

Tretter, Steven A., "**Communication System Design Using DSP Algorithms With Laboratory Experiments for the TMS320C6713™ DSK",** Springer USA*, 2008.*

Reference Books:

1. Robert. O. Cristi, "**Modern Digital signal processing",** Cengage Publishers, India, 2003.
2. S. K. Mitra, "**Digital signal processing: A computer based approach",** 3rd edition, TMH, India, 2007.
3. E.C. Ifeachor, and B. W. Jarvis, "**Digital signal processing: A Practitioner's approach",** Second Edition, Pearson Education, India, 2002,
4. Proakis, and Manolakis, "**Digital signal processing**", 3rd edition, Prentice Hall, 1996.

Real Time Systems

[As per Choice Based credit System (CBCS) Scheme
SEMESTER – IV

Subject Code	16ECS424	IA Marks	20
Number of Lecture Hours/Week	03	Exam marks	80
Total Number of Lecture Hours	40 (8 Hours per Module)	Exam Hours	03

CREDITS – 03

Course Objectives: This course will enable students to:

- Understand basics of Real Time systems.
- Distinguish a real-time system with other systems.
- Identify the functions of operating system
- Evaluate the need for Real time operating system.
- Design and develop embedded applications by means of real-time operating systems.

Modules	**RBT Level**
Module 1	
Introduction to Real-Time Embedded Systems: Brief history of Real Time Systems, A brief history of Embedded Systems. **System Resources:** Resource Analysis, Real-Time Service Utility, Scheduling Classes, The Cyclic Executive, Scheduler Concepts, Preemptive Fixed Priority Scheduling Policies, Real-Time OS, Thread Safe Re-entrant Functions.	L1, L2
Module 2	
Processing: Preemptive Fixed-Priority Policy, Feasibility, Rate Montonic least upper bound, Necessary and Sufficient feasibility, Deadline – Monotonic Policy, Dynamic priority policies. **I/O Resources:** Worst-case Execution time, Intermediate I/O, Execution efficiency, I/O Architecture. **Memory:** Physical hierarchy, Capacity and allocation, Shared Memory, ECC Memory, Flash file systems.	L1, L2
Module 3	
Multi-resource Services: Blocking, Deadlock and livestock, Critical sections to protect shared resources, priority inversion. **Soft Real-Time Services:** Missed Deadlines, QoS, Alternatives to rate monotonic policy, Mixed hard and soft real-time services.	L1, L2
Module 4	
Embedded System Components: Firmware components, RTOS system software mechanisms, Software application components. **Debugging Components:** Exceptions assert, Checking return codes, Single-step debugging, kernel scheduler traces, Test access ports, Trace ports, Power-On self test and diagnostics.	L1, L2, L3
Module 5	
Performance Tuning: Basic concepts of drill-down tuning,	L1, L2,

hardware – supported profiling and tracing, Building performance monitoring into software, Path length. **High availability and Reliability Design:** Reliability and Availability, Similarities and differences, Reliability, Reliable software, Available software, Design tradeoffs, Hierarchical applications for Fail-safe design.	L3

Course Outcomes: After studying this course, students will be able to:

- Analyze Real time operating systems.
- Describe the functions of Real time operating systems.
- Demonstrate embedded system applications.
- Design a Real Time operating system.

Question paper pattern:

- The question paper will have 10 full questions carrying equal marks.
- Each full question consists of 16 marks with a maximum of four sub questions.
- There will be 2 full questions from each module covering all the topics of the module
- The students will have to answer 5 full questions, selecting one full question from each module.

Text Book:

Sam Siewert, "Real-Time Embedded Systems and Components", Cengage Learning India Edition, 2007.

Reference Books:

1. Krishna CM and Kang Singh G, "Real time systems", Tata McGraw Hill, 2003, ISBN: 0-07-114243-64
2. Qing Li and Carolyn Yao, "Real-Time Concepts for Embedded Systems", CMP Books, 2003, ISBN:1578201241
3. Jane W. S. Liu, "Real Time Systems", Prentice Hall, 2000, ISBN: 0130996513
4. Phillip A. Laplante, "Real-Time Systems Design and Analysis", John Wiley & Sons, 2004.

VISVESVARAYA TECHNOLOGICAL UNIVERSITY, BELAGAVI
Scheme of Teaching and Examination – 2018-19
M.Tech in Communication Systems/ Digital Communication & Networking/ Digital Communication Engineering/ Digital Electronics & Communication Systems/ Digital Electronics & Communication (ECS)
Choice Based Credit System (CBCS)

I SEMESTER

Sl. No	Course	Course Code	Course Title	Teaching Hours /Week		Examination				Credits
				Theory	Practical/ Field work/ Assignment	Duration in hours	CIE Marks	SEE Marks	Total Marks	
1	PCC	18ELD11	Advanced Engineering Mathematics	04	--	03	40	60	100	4
2	PCC	18ECS12	Advanced Digital Signal Processing	04	--	03	40	60	100	4
3	PCC	18EVE13	Advanced Embedded System	04	--	03	40	60	100	4
4	PCC	18ECS14	Advanced Communication Systems-1	04	--	03	40	60	100	4
5	PCC	18ECS15	Advanced Communication Networks	04	--	03	40	60	100	4
6	PCC	18ECSL16	Advanced Digital Signal Processing Lab	-	04	03	40	60	100	2
7	PCC	18RMI17	Research Methodology and IPR	02	--	03	40	60	100	2
			TOTAL	**22**	**04**	**21**	**280**	**420**	**700**	**24**

Note: PCC: Professional core

Internship: All the students have to undergo mandatory internship of 6 weeks during the vacation of I and II semesters and /or II and III semesters. A University examination shall be conducted during III semester and the prescribed credit shall be counted forthe same semester. Internship shall be considered as a head of passing and shall be considered for the award of degree. Those, who do not take-up/complete the internship shall be declared as failed and have to complete during the subsequent University examination after satisfying the internship requirements.

VISVESVARAYA TECHNOLOGICAL UNIVERSITY, BELAGAVI
Scheme of Teaching and Examination – 2018-19
M.Techin Communication Systems/ Digital Communication & Networking/ Digital Communication Engineering/ Digital Electronics & Communication Systems/ Digital Electronics & Communication (ECS)
Choice Based Credit System (CBCS)

II SEMESTER

Sl. No	Course	Course Code	Course Title	Teaching Hours /Week		Examination				Credits
				Theory	Practical/ Field work/ Assignment	Duration in hours	CIE Marks	SEE Marks	Total Marks	
1	PCC	18ECS21	Advanced Communication Systems-2	04	--	03	40	60	100	4
2	PCC	18ECS22	Antenna Theory and Design	04	--	03	40	60	100	4
3	PCC	18ECS23	Error Control Coding	04	--	03	40	60	100	4
4	PEC	18XXX24X	Professional Elective 1	04	--	03	40	60	100	4
5	PEC	18XXX25X	Professional Elective 2	04	--	03	40	60	100	4
6	PCC	18ECSL26	Advanced Communication Lab	--	04	03	40	60	100	2
7	PCC	18ECS27	Technical Seminar	--	02	--	100	--	100	2
TOTAL				**20**	**06**	**18**	**340**	**360**	**700**	**24**

Note: PCC: Professional core, PEC: Professional Elective

Professional Elective 1		**Professional Elective 2**	
Course Code under 18XXX24X	**Course title**	**Course Code under 18XXX25X**	**Course title**
18ECS241	Wireless Sensor Networks	18ECS251	Multimedia Over Communication links
18EVE242	Nanoelectronics	18ESP252	Statistical Signal Processing
18ECS243	Cryptography and Network Security	18ELD253	Micro Electro Mechanical Systems

Note:

1. Technical Seminar: CIE marks shall be awarded by a committee comprising of HoD as Chairman, Guide/co-guide, if any, and a senior faculty of the department. Participation in the seminar by all postgraduate students of the same and other semesters of the programme shall be mandatory.
The CIE marks awarded for Technical Seminar, shall be based on the evaluation of Seminar Report, Presentation skill and Question and Answer session in the ratio 50:25:25.

2. Internship: All the students shall have to undergo mandatory internship of 6 weeks during the vacation of I and II semesters and /or II and III semesters. A University examination shall be conducted during III semester and the prescribed credit shall be counted in the same semester. Internship shall be considered as a head of passing and shall be considered for the award of degree. Those, who do not take-up/complete the internship shall be declared as failed and have to complete during the subsequent University examination after satisfying the internship requirements.

VISVESVARAYA TECHNOLOGICAL UNIVERSITY, BELAGAVI
Scheme of Teaching and Examination – 2018-19
M.Techin Communication Systems/ Digital Communication & Networking/ Digital Communication Engineering/ Digital Electronics & Communication Systems/ Digital Electronics & Communication (ECS)
Choice Based Credit System (CBCS)

III SEMESTER

Sl. No	Course	Course Code	Course Title	Teaching Hours /Week		Examination				Credits
				Theory	Practical/ Field work/ Assignment	Duration in hours	CIE Marks	SEE Marks	Total Marks	
1	PCC	18ECS31	LTE 4G Broadband	04	--	03	40	60	100	4
2	PEC	18XXX32X	Professional Elective 3	04	--	03	40	60	100	4
3	PEC	18XXX33X	Professional Elective 4	04	--	03	40	60	100	4
4	Project	18ECS34	Evaluation of Project phase -1	--	02	--	100	--	100	2
5	Internship	18ECSI35	Internship	(Completed during the intervening vacation of I and II semesters and /or II and III semesters.)		03	40	60	100	6
TOTAL				12	02	12	**260**	**240**	**500**	**20**

Note: PCC: Professional core, PEC: Professional Elective

Professional Elective 3		**Professional Elective 4**	
Course Code under 18XXX32X	**Course title**	**Course Code under 18XXX33X**	**Course title**
18ECS321	Advances in Image Processing	18ECS331	RF and Microwave Circuit Design
18ESP322	Array Signal Processing	18ESP332	Pattern Recognition & Machine Learning
18ECS323	Real Time Systems	18ECS333	IoT

Note:
1. Project Phase-1: Students in consultation with the guide/co-guide if any, shall pursue literature survey and complete the preliminary requirements of selected Project work. Each student shall prepare relevant introductory project document, and present a seminar.
CIE marks shall be awarded by a committee comprising of HoD as Chairman, Guide/co-guide if any, and a senior faculty of the department. The CIE marks awarded for project work phase -1, shall be based on the evaluation of Project Report, Project Presentation skill and Question and Answer session in the ratio 50:25:25.
SEE (University examination) shall be as per the University norms.
2. Internship: Those, who have not pursued /completed the internship shall be declared as failed and have to complete during subsequent University examinations after satisfying the internship requirements. Internship SEE (University examination) shall be as per the University norms.

VISVESVARAYA TECHNOLOGICAL UNIVERSITY, BELAGAVI
Scheme of Teaching and Examination – 2018-19
M.Tech in Communication Systems/ Digital Communication & Networking/ Digital Communication Engineering/ Digital Electronics & Communication Systems/ Digital Electronics & Communication (ECS)
Choice Based Credit System (CBCS)

IV SEMESTER

Sl. No	Course	Course Code	Course Title	Teaching Hours /Week		Examination				Credits
				Theory	Field work/ Assignment	Duration in hours	CIE Marks	SEE Marks Viva voce	Total Marks	
1	Project	18ECS41	Project work Phase -2	--	04	03	40	60	100	20
			TOTAL	--	**04**	**03**	**40**	**60**	**100**	**20**

Note:

1. Project Phase-2:

CIE marks shall be awarded by a committee comprising of HoD as Chairman, Guide/co-guide, if any, and a Senior faculty of the department. The CIE marks awarded for project work phase -2, shall be based on the evaluation of Project Report subjected to plagiarism check, Project Presentation skill and Question and Answer session in the ratio 50:25:25.

SEE shall be at the end of IV semester. Project work evaluation and Viva-Voce examination (SEE), after satisfying the plagiarism check, shall be as per the University norms.

FIRST SEMESTER SYLLABUS

ADVANCED ENGINEERING MATHEMATICS [As per Choice Based Credit System (CBCS) Scheme] SEMESTER – I			
Course Code	**18ELD11**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**04**	**SEE Marks**	**60**
Total Number of Lecture Hours	**50 (10 Hours per Module)**	**Exam Hours**	**03**
CREDITS – 04			

Course objectives: This course will enable students to:

- To learn principles of advanced engineering mathematics through linear algebra and calculus of variations.
- To understand probability theory and random process that serve as an essential tool for applications of electronics and communication engineering sciences

Modules	**Revised Bloom's Taxonomy (RBT) Level**
Module -1	
Linear Algebra-I Introduction to vector spaces and sub-spaces, definitions, illustrative example. Linearly independent and dependent vectors- Basis-definition and problems. Linear transformations-definitions.Matrix form of linear transformations-Illustrative examples (Text Book:1).	**L1,L2**
Module -2	
Linear Algebra-II Computation of eigen values and eigen vectors of real symmetric matrices-Given's method. Orthogonal vectors and orthogonal bases. Gram-Schmidt orthogonalization process (Text. Book:1).	**L1,L2**
Module -3	
Calculus of Variations : - Concept of functional-Eulers equation**.**Functionaldependent on first and higher order derivatives, Functional on several dependent variables. Isoperimetric problems-variation problems with moving boundaries. (Text.Book:2)	**L1,L2**
Module -4	
Probability Theory:-Review of basic probability theory. Definitions of random variables and probability distributions, probability mass and density functions, expectation, moments, central moments, characteristic functions, probability generating and moment generating functions-illustrations. Poisson, Gaussian and Erlang distributions-	**L1,L2**

Module -5	
Engineering Applications on Random processes:- Classification. Stationary, WSS and ergodic random process. Auto-correlation function-properties, Gaussian random process. (Text Book: 3)	**L1,L2**

Course Outcomes: After studying this course, students will be able to:

- Understand vector spaces, basis, linear transformations and the process of obtaining matrix of linear transformations arising in magnification and rotation of images.
- Apply the technique of singular value decomposition for data compression, least square approximation in solving inconsistent linear systems.
- Utilize the concepts of functional and their variations in the applications of communication systems, decision theory, synthesis and optimization of digital circuits.
- Learn the idea of random variables (discrete/continuous) and probability distributions in analyzing the probability models arising in control systems and system communications.
- Analyze random process through parameter-dependent variables in various random processes.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Books:

1. David C.Lay, Steven R.Lay and J.J.McDonald: "LinearAlgebra and its Applications", 5th Edition, Pearson Education Ltd., 2015
2. Elsgolts, L.:"Differential Equations and Calculus of Variations", MIR Publications, 3rd Edition, 1977.
3. T.Veerarajan: "Probability, Statistics and Random Process",3rd Edition,Tata Mc-Graw Hill Co.,2016.

Reference Books:

1. Gilbert Strang: Introduction to Linear Algebra, 5th Edition, Wellesley-Cambridge Press., 2016
2. Richard Bronson: "Schaum's Outlines of Theory and Problems of Matrix Operations", McGraw-Hill, 1988.
3. Scott L.Miller,DonaldG.Childers: "Probability and Random Process with application to Signal Processing", Elsevier Academic Press,2nd Edition,2013.

4. E. Kreyszig, “Advanced Engineering Mathematics”, 10th edition, Wiley, 2015.

Web links:

1. http://nptel.ac.in/courses.php?disciplineId=111
2. http://www.class-central.com/subject/math(MOOCs)
3. http://ocw.mit.edu/courses/mathematics/
4. www.wolfram.com

ADVANCED DIGITAL SIGNAL PROCESSING **[As per Choice Based Credit System (CBCS) Scheme** **SEMESTER – I**			
Course Code	**18ECS12**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**04**	**SEE Marks**	**60**
Total Number of Lecture Hours	**50** **(10 Hours per Module)**	**Exam Hours**	**03**
Credits – 04			

Course objectives: This course will enable students to

- Understand Multirate digital signal processing principles and its applications.
- Estimate the various spectral components present in the received signal using different spectral estimation methods such as Parametric and Nonparametric.
- Design and implement an optimum adaptive filter using LMS and RLS algorithms.
- Understand the concepts and mathematical representations of Wavelet transforms.

Modules	**RBT Levels**
Module-1	
Multirate Digital Signal Processing: Introduction, decimation by a factor 'D', Interpolation by a factor 'I', sampling rate conversion by a factor 'I/D', Implementation of sampling rate conversion, Multistage implementation of sampling rate conversion, Applications of multirate signal processing, Digital filter banks, two channel quadrature mirror filter banks, M-channel QMF bank. (Text 1)	L1, L2, L3
Module-2	
Linear prediction and Optimum Linear Filters: Random signals, Correlation Functions and Power Spectra, Innovations Representation of a Stationary Random Process. Forward and Backward Linear Prediction. Solution of the Normal Equations. The Levinson-Durbin Algorithm. Properties of the Linear Prediction-Error Filters. (Text 1)	L1, L2, L3
Module-3	
Adaptive filters: Applications of Adaptive Filters-Adaptive Channel Equalization, Adaptive noise cancellation, Linear Predictive coding of Speech Signals, Adaptive direct form FIR filters-The LMS algorithm, Properties of LMS algorithm. Adaptive direct form filters- RLS algorithm. (Text 1)	L1, L2, L3
Module-4	
Power Spectrum Estimation: Non parametric Methods for Power Spectrum Estimation - Bartlett Method, Welch Method, Blackman and Tukey Methods.	L1, L2,

Parametric Methods for Power Spectrum Estimation: Relationship between the auto correlation and the model parameters, Yule and Walker methods for the AR Model Parameters, Burg Method for the AR Model parameters, Unconstrained least-squares method for the AR Model parameters, Sequential estimation methods for the AR Model parameters, ARMA Model for Power Spectrum Estimation. (Text 1)	L3
Module-5	
WAVELET TRANSFORMS: The Age of Wavelets, The origin of Wavelets, Wavelets and other reality transforms, History of wavelets, Wavelets of the future. **Continuous Wavelet and Short Time Fourier Transform:** Wavelet Transform, Mathematical preliminaries, Properties of wavelets. Discrete Wavelet Transform: Haar scaling functions, Haar wavelet function, Daubechies Wavelets. (Chapters 1, 3 & 4 of Text 2)	L1, L2, L3

Course Outcomes: After studying this course, students will be able to:

- Design adaptive filters for a given application
- Design multirate DSP Systems
- Implement adaptive signal processing algorithm
- Design active networks
- Understand advanced signal processing techniques, including multi-rate processing and time-frequency analysis techniques

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Books:

1. "Digital Signal Processing, Principles, Algorithms and Applications", JohnG. Proakis, Dimitris G.Manolakis, Fourth edition, Pearson-2007.
2. Insight into Wavelets- from Theory to Practice", K.P Soman, Ramachandran, Resmi- PHI Third Edition-2010.

ADVANCED EMBEDDED SYSTEM **[As per Choice Based Credit System (CBCS) scheme] SEMESTER – I**			
Subject	**18EVE13**	**CIE**	**40**
Number of Lecture Hours/Week	**04**	**SEE Marks**	**60**
Total Number of Lecture Hours	**50 (10 Hours per Module)**	**Exam Hours**	**03**
CREDITS – 04			

Course objectives: This course will enable students to:

- Understand the basic hardware components and their selection method based on the characteristics and attributes of an embedded system.
- Describe the hardware software co-design and firmware design approaches
- Explain the architectural features of ARM CORTEX M3, a 32 bit microcontroller including memory map, interrupts and exceptions.
- Program ARM CORTEX M3 using the various instructions, for different applications.

Modules	**Revised Bloom's Taxonomy (RBT) Level**
Module -1	
Embedded System: Embedded vs General computing system, classification, application and purpose of ES. Core of an Embedded System, Memory, Sensors, Actuators, LED, Opto coupler, Communication Interface, Reset circuits, RTC, WDT, Characteristics and Quality Attributes of Embedded Systems (Text 1: Selected Topics from Ch -1, 2, 3).	**L1, L2, L3**
Module -2	
Hardware Software Co-Design, embedded firmware design approaches, computational models, embedded firmware development languages, Integration and testing of Embedded Hardware and firmware, Components in embedded system development environment (IDE), Files generated during compilation, simulators, emulators and debugging (Text 1: Selected Topics From Ch-7, 9, 12, 13).	**L1, L2, L3**
Module -3	
ARM-32 bit Microcontroller: Thumb-2 technology and applications of ARM, Architecture of ARM Cortex M3, Various Units in the architecture, General Purpose Registers, Special Registers, exceptions, interrupts, stack operation, reset sequence (Text 2: Ch 1, 2, 3)	**L1, L2, L3**
Module -4	

Instruction Sets: Assembly basics, Instruction list and description, useful instructions, Memory Systems, Memory maps, Cortex M3 implementation overview, pipeline and bus interface (Text 2: Ch-4, 5, 6).	**L1, L2, L3**
Module -5	
Exceptions, Nested Vector interrupt controller design, Systick Timer, Cortex-M3 Programming using assembly and C language, CMSIS (Text 2: Ch-7, 8, 10).	**L1, L2, L3**

Course Outcomes: After studying this course, students will be able to:

- Understand the basic hardware components and their selection method based on the characteristics and attributes of an embedded system.
- Explain the hardware software co-design and firmware design approaches.
- Acquire the knowledge of the architectural features of ARM CORTEX M3, a 32 bit microcontroller including memory map, interrupts and exceptions.
- Apply the knowledge gained for Programming ARM CORTEX M3 for different applications.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Books:

1. K. V. Shibu, "Introduction to embedded systems", TMH education Pvt. Ltd. 2009.

2. Joseph Yiu, “The Definitive Guide to the ARM Cortex-M3”, 2nd edn, Newnes, (Elsevier), 2010.

Reference Book:

James K. Peckol, "Embedded systems- A contemporary design tool", John Wiley, 2008.

Advanced Communications Systems -1(Theory & Practice)						
Course Code	**:**	**18ECS14**		**CIE Marks**	**:**	**40**
Hrs/Week	**:**	**L:T:P:S**	**4:0:0:0**	**SEE Marks**	**:**	**60**
Credits	**:**	**4**		**SEE Duration**	**:**	**3 Hrs**

Course Learning Objectives (CLO):

Students shall be able to

1. Understand different modulation, demodulation and equalization techniques and use them to analyze the error performance of digital modulation techniques in presence of AWGN noise.
2. Analyze and demonstrate the model of discrete time channel with ISI & the model of discrete time channel by equalizer.
3. Apply various types of equalizers used for channel modeling and adjusting the filter coefficients
4. Develop the concept of Spread Spectrum Communications over wideband channels.

Module -1	**10 Hrs**

Signal Representation – Low pass representation of bandpass signals, Low pass representation of bandpass random process [Text 1 , Chapter 2: 2.1, and 2.9 only]

Modulation: Representation of digitally modulated Signals , Modulation Schemes without memory (Band Limited Schemes - PAM,BPSK,QPSK,MPSK,MQAM, Power Limited Schemes – FSK,MFSK, DPSK,DQPSK), modulation schemes with memory (Basics of CPFSK and CPM – Full Treatment of MSK), Transmit PSD for Modulation Schemes. (Section 3.4 [Text 1 , Chapter 3: 3.1, 3.2 and 3.3]

Module -2	**10 Hrs**

Demodulation - Vector Channel, Vector Channel +AWGN, Performance parameters, Optimum Coherent Detection for power limited and Bandlimited schemes, Optimal Coherent detection for schemes with memory, Optimal Non – Coherent detection for schemes without and with memory (FSK, DPSK,DQPSK), Comparison of detection schemes. [Text 1, Chapter 4: 4.1, 4.2.- 4.2.2, 4.3, 4.4, 4.5.1, 4.5.2, 4.5.5 and 4.6]

Module - 3	**10 Hrs**

Bandlimited Channels: Bandlimited channel characterization, signalling through band limited linear filter channels, Sinc, RC, Duobinary and Modified Duobinary signaling schemes, Optimum receiver for channel with ISI and AWGN.

Linear Equalizers: Zero forcing Equalizer, MSE and MMSE, Baseband and Passband Linear Equalizers. Performance of ZFE and MSE.(Excluding 9.4-3, 9.4-4)[Text 1, Chapter 9: 9.1, 9.2 - 9.2.1, 9.2.2, 9.2.3, 9.3-9.3.1, 9.3.2 and 9.4

Unit – IV	**10 Hrs**

Non-Linear Equalizers: Decision - feedback equalization, Predictive DFE, Performance of DFE.[Text 1, Chapter 9: 9.5: 9.5-1 only]

Adaptive equalization: Adaptive linear equalizer, adaptive decision feedback equalizer, Adaptive Fractionally spaced Equalizer (Tap Leakage Algorithm), Adaptive equalization of Trellis - coded signals.[Text 1, Chapter 10: 10.1, 10.1-1, 10.1-2, 10.1-3, 10.1-6,10.1-7, 10.2, 10.3]

Unit – V	**10 Hrs**

Spread spectrum signals for digital communication: Model of spread spectrum digital communication system, Direct sequence spread spectrum signals, some applications of DS spread spectrum signals , generation of PN sequences, Frequency hopped spread spectrum signals , Time hopping SS, Synchronization of SS systems.

[Text 1, Chapter 12: 12.1, 12.2 (except 12.2-1), 12.2-2, 12.2-5, 12.3, 12.4, 12.5]

Expected Course Outcomes:

After going through this course the student will be able to:

- Explain the concept of low pass and Bandpass signals representations at the Transmitter, the process of Detection and Estimation at the receiver in the presence of AWGN only.
- Evaluate Receiver performance for various types of single carrier symbol modulations through ideal and AWGN Non-bandlimited and bandlimited channels.
- Design single carrier equalizers for various symbol modulation schemes and detection methods for defined channel models, and compute parameters to meet desired rate and performance requirements.
- Design and Evaluate Non band limited and Non power limited spread spectrum systems for communications in a Jamming environment, multiuser situation and low power intercept environment.

Text Books

1.	John G. Proakis, MasoudSalehi,"Digital Communications ",5e,Pearson Education(2014),ISBN:978-9332535893

Reference Books

2.	Bernard Sklar,"Digital Communications: Fundamentals and Applications: Fundamentals &Applications",2e,Pearson Education(2009),ISBN:978-8131720929
3.	Simon Haykin ,"Digital Communications Systems",1e,Wiley(2014),ISBN:978-8126542314

ADVANCED COMPUTER COMMUNICATION NETWORKS

[As per Choice Based Credit System (CBCS) scheme]

SEMESTER –I

Subject Code	18ECS15	IA Marks	40
Number of Lecture Hours/Week	04	Exam Marks	60
Total Number of Lecture Hours	50 (10 Hours Per Module)	Exam Hours	03

CREDITS – 04

Course objectives: This course will enable students to:

- Develop an awareness towards current practice in Networking
- Learn various aspects involved in wireless networks
- Develop an awareness regarding the Packet Processing ,Routing issues in computer networks
- Understand some of the shortest path routing protocols
- Develop an awareness towards the network control and traffic management
- Understand the congestion control and flow control mechanisms

Modules	Revised Bloom's Taxonomy
Module -1	
Functional Elements and Current Practice in Networking: Networking as Resource Sharing, Analogy with the Operating System of a Computer, The Functional Elements: Multiplexing, Switching, Routing, Network Management, Traffic Controls and Timescales, Current Practice: Network Infrastructure, Networking Architectures, Telephone and ISDN Networks, X.25 and Frame Relay Networks, The Internet, Asynchronous Transfer Mode (ATM) Networks. (Text 1)	**L1, L2, L3**
Module -2	
Wireless Networks: Bits over a Wireless Network, TCP Performance over Wireless Links, Adaptive and Cross-Layer Techniques, Random Access: Aloha, S-Aloha, and CSMA/CA, Wireless Local Area Networks, Wireless Ad Hoc Networks, Link Scheduling and Network Capacity, Scheduling Constraints, Centralized Scheduling, Capacity of a WANET, Wireless Sensor Networks: An Overview (Text 1)	**L1, L2, L3**
Module -3	
Packet Processing: Addressing and Address Lookup, Addressing, Addressing in IP Networks: Subnets and Classless Inter domain Routing, Efficient Longest Prefix Matching: Level-Compressed Tries, Hardware-Based Solutions, Packet Classification **Routing:** Engineering Issues, Shortest Path Routing of Elastic Aggregates, Elastic Aggregates and Traffic Engineering, Optimal Routing, Algorithms for Shortest Path Routing: Dijkstra's Algorithm, The Bellman–Ford Algorithm, Routing Protocols, Distance Vector Protocols, Link State Protocols.(Text 1)	**L1, L2, L3**
Module -4	

Traffic Management: Introduction, framework for traffic management, traffic models, traffic classes, traffic scheduling (Text 3). **Control of Networks:** Objectives and methods of control, routing optimization in circuit and datagram networks, Queuing models in circuit and datagram networks (Text 2).	**L1, L2, L3**
Module -5	
Congestion and flow control: Congestion control ,Window congestion control, Rate congestion control, control problems in ATM Networks (Text 2), flow control model, flow control classification, open loop flow control, closed loop flow control (Text 3).	**L1, L2, L3, L4**

Course outcomes: After studying this course, students will be able to:

- Choose appropriate Network Infrastructure and Networking Architectures which suits current practice in networking
- Identify the suitable random access methods which suits wireless networks
- Identify IP configuration for the network with suitable routing mechanisms
- Analyze and develop various network traffic management and control techniques
- Analyze and develop various congestion and flow control

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Books:

1. Anurag Kumar, D. Manjunath, Joy Kuri, “Communication Networking : An Analytical Approach” , Morgan Kaufmann publications, ISBN: 0-12-428751-4, 2004.
2. J. Walrand and P. Varaya, "High performance communication networks", Harcourt Asia (Morgan Kaufmann), 2000.
3. S. Keshav “An Engineering Appproach to Computer Networking”, Pearson Education, ISBN: 978-81-317-1145-3, 2011.

Reference Book:

1. Andrew S Tanenbaum , “Computer Networks”, 4th edition , Pearson Education

Advanced Digital Signal Processing Lab **[As per Choice Based Credit System (CBCS) scheme]** **SEMESTER – I**			
Course Code	**18ECSL16**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**01Hr Tutorial (Instructions) + 03 Hours Laboratory**	**SEE Marks**	**60**
Total Number of Lecture Hours		**Exam Hours**	**03**

Credits – 02

Course objectives: This laboratory courseenables students to get practical Experience in Digital Signal processing ,analysis and realization of LTI systems .

Laboratory Experiments:	**RBT Levels**
01. Generate various fundamental discrete time signals.	L1, L2,L3
02. Basic operations on signals (Multiplication, Folding, Scaling).	
03. Find out the DFT & IDFT of a given sequence without using inbuilt instructions.	
04. Interpolation & decimation of a given sequence.	
05. Generation of DTMF (Dual Tone Multiple Frequency) signals.	
06. Estimate the PSD of a noisy signal using periodogram and modified periodogram.	
07. Estimation Of PSD using different methods (Bartlett, Welch, Blackman-Tukey).	
08. Design of Chebychev Type I,II Filters.	
09. Cascade Digital IIR Filter Realization.	
10. Parallel Realization of IIR filter.	
11. Estimation of power spectrum using parametric methods (yule-walker & burg).	
12. Design of LPC filter using Levinson-Durbin algorithm.	
13. Time-Frequency Analysis with the Continuous Wavelet Transform.	
14. Signal Reconstruction from Continuous Wavelet Transform Coefficients.	

Course outcomes: On the completion of this laboratory course, the students will be able to have hands on experience on,

- Filter design.
- Filter Realization
- Signal Manipulations
- Wavelet Transforms
- Estimating PSD using various techniques

Conduct of Practical Examination:

- All laboratory experiments are to be included for practical examination.
- The experiments can be conducted in Matlab or using any other related tools.
- Strictlyfollowtheinstructionsasprintedonthecoverpageofanswerscriptforbr eakupofmarks.
- Change of experiment is allowed only once and Marks allotted to the Procedure part will be made zero.

RESEARCH METHODOLOGY AND IPR

[As per Choice Based Credit System (CBCS) scheme]
SEMESTER –I

Course Code	18RMI17	CIE Marks	40
Number of Lecture Hours/Week	02	Exam Hours	03
Total Number of Lecture Hours	25	SEE Marks	60
Credits - 02			

Course objectives:

- To give an overview of the research methodology and explain the technique of defining a research problem
- To explain the functions of the literature review in research.
- To explain carrying out a literature search, its review, developing theoretical and conceptual frameworks and writing a review.
- To explain various research designs and their characteristics.
- To explain the details of sampling designs, and also different methods of data collections.
- To explain the art of interpretation and the art of writing research reports.
- To explain various forms of the intellectual property, its relevance and business impact in the changing global business environment.
- To discuss leading International Instruments concerning Intellectual Property Rights.■

Module-1	**Teaching Hours/ RBT Level**
Research Methodology: Introduction, Meaning of Research, Objectives of Research, Motivation in Research, Types of Research, Research Approaches, Significance of Research, Research Methods versus Methodology, Research and Scientific Method, Importance of Knowing How Research is Done, Research Process, Criteria of Good Research, and Problems Encountered by Researchers in India. ■	**05** **L1, L2**
Module-2	

Defining the Research Problem: Research Problem, Selecting the Problem, Necessity of Defining the Problem, Technique Involved in Defining a Problem, An Illustration. **Reviewing the literature:** Place of the literature review in research, Bringing clarity and focus to your research problem, Improving research methodology, Broadening knowledge base in research area, Enabling contextual findings, How to review the literature, searching the existing literature, reviewing the selected literature, Developing a theoretical framework, Developing a conceptual framework, Writing about the literature reviewed. ■	**05** **L1, L2**
Module-3	
Research Design: Meaning of Research Design, Need for Research Design, Features of a Good Design, Important Concepts Relating to Research Design, Different Research Designs, Basic Principles of Experimental Designs, Important Experimental Designs. **Design of Sample Surveys:** Introduction, Sample Design, Sampling and Non-sampling Errors, Sample Survey versus Census Survey, Types of Sampling Designs. ■	**05** **L1, L2**
Module-4	
Data Collection: Experimental and Surveys, Collection of Primary Data, Collection of Secondary Data, Selection of Appropriate Method for Data Collection, Case Study Method. **Interpretation and Report Writing:** Meaning of Interpretation, Technique of Interpretation, Precaution in Interpretation, Significance of Report Writing, Different Steps in Writing Report, Layout. **Interpretation and Report Writing (continued):** of the Research Report, Types of Reports, Oral Presentation, Mechanics of Writing a Research Report, Precautions for Writing Research Reports. ■	**05** **L1, L2, L3, L4**
Module-5	

Intellectual Property: The Concept, Intellectual Property System in India, Development of TRIPS Complied Regime in India, Patents Act, 1970, Trade Mark Act, 1999,The Designs Act, 2000, The Geographical Indications of Goods (Registration and Protection) Act1999, Copyright Act,1957,The Protection of Plant Varieties and Farmers' Rights Act, 2001,The Semi-Conductor Integrated Circuits Layout Design Act, 2000, Trade Secrets, Utility Models, IPR and Biodiversity, The Convention on Biological Diversity (CBD) 1992, Competing Rationales for Protection of IPRs, Leading International Instruments Concerning IPR, World Intellectual Property Organisation (WIPO),WIPO and WTO, Paris Convention for the Protection of Industrial Property, National Treatment, Right of Priority, Common Rules, Patents, Marks, Industrial Designs, Trade Names, Indications of Source, Unfair Competition, Patent Cooperation Treaty (PCT), Advantages of PCT Filing, Berne Convention for the Protection of Literary and Artistic Works, Basic Principles, Duration of Protection, Trade Related Aspects of Intellectual Property Rights(TRIPS) Agreement, Covered under TRIPS Agreement, Features of the Agreement, Protection of Intellectual Property under TRIPS, Copyright and Related Rights, Trademarks, Geographical indications, Industrial Designs, Patents, Patentable Subject Matter, Rights Conferred, Exceptions, Term of protection, Conditions on Patent Applicants, Process Patents, Other Use without Authorization of the Right Holder, Layout-Designs of Integrated Circuits, Protection of Undisclosed Information, Enforcement of Intellectual Property Rights, UNSECO. ■	**05** **L1, L2, L3, L4**

Course outcomes:

At the end of the course the student will be able to:

- Discuss research methodology and the technique of defining a research problem
- Explain the functions of the literature review in research, carrying out a literature search, developing theoretical and conceptual frameworks and writing a review.
- Explain various research designs and their characteristics.
- Explain the art of interpretation and the art of writing research reports
- Discuss various forms of the intellectual property, its relevance and

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

SECOND SEMESTER SYLLABUS

ADVANCED COMMUNICATIONS SYSTEMS -2 **[As per Choice Based Credit System (CBCS) scheme]** **SEMESTER – II**			
Course Code	**18ECS21**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**04**	**SEE Marks**	**60**
Total Number of Lecture Hours	**50 (10 Hours per Module)**	**Exam Hours**	**03**
Credits – 04			

Course Learning Objectives (CLO):

Students shall be able to

1. Describe modelsfor fading channels, and concepts of diversity in time, frequency and space.
2. Demonstrate the concept of synchronization, maximal ratio combining, Rake Receivers, multicarrier OFDM and MIMO.
3. Analyze the capacity and error performance and implementation of maximal ratio combining, Rake receivers, OFDM and MIMO in presence of AWGN noise
   Design simple MIMO-OFDM system for a deterministic multipath channel.

Modules	**RBT Levels**
Module-1	
Synchronization – Signal Parameter estimation, Carrier Phase Estimation, Symbol Timing Recovery, Performance of ML estimators.[Text 1, Chapter 5] **Fading** – Large scale, small scale; Statistical characterization of multipath channels – Delay and Doppler spread, classification of multipath channels, scattering function; Binary signaling over frequency non selective Rayleigh fading channel. [Text 1, Chapter 13]	**L1,L2**
Module-2	
Fading Contd: - Diversity techniques for performance improvement with binary signaling over FNS, Slow fading channels – power combining and Maximal ratio combining; Frequency selective channels – Rake receivers, Performance, Tap weight Synchronization, Application to CDMA. [Text 1, Chapter 13] **Multicarrier Signalling:**A brief overview of Frequency Diversity. [Text 2, Sec 3.4.1, 3.4.2] Multicarrier Communications in AWGN channel- Single carrier	**L1,L2**

vs Multicarrier, OFDM, FFT Implementation, Spectral Characteristics, Power and bit allocation, Peak to Average Power Ratio, Channel Coding Considerations [Text 1, 11.2.1 to 11.2.9] and [Text 2, Sec 3.4.4]	
Module-3	
Capacity of wireless channel: AWGN channel capacity [Sec 5.1 All subsections], Resources of AWGN channel [5.2 All sub sections], Linear time invariant Gaussian channel[5.3 All sub sections], Capacity of Fading Channels [Sec5.4 All subsections]. [Text 2 Chapter 5]	**L1,L2**
Module-4	
MIMO spatial multiplexing and channel modeling: Multiplexing capability of deterministic MIMO channels,Physical modeling of MIMO channels, Modeling of MIMO fading channels**.** [Text 2, Chapter 7]	
Module-5	
MIMO capacity and multiplexing architectures: The V-BLAST architecture, Fast fading MIMO channel, Capacity with CSI at receiver, Performance gains, Full CSI, Performance gains in a MIMO channel, Receiver architectures – (Linear decorrelator, Successive cancellation, Linear MMSE receiver), Information theoretic optimality, Connections with CDMA multiuser detection and ISI equalization, Slow fading MIMO channel. [Sections 8.1 to 8.4, Text 2]	**L1,L2**

Expected Course Outcomes:

After going through this course the student will be able to:

- Explain the concepts of multi-channel signaling (including OFDM) scheme and synchronization for carrier and symbol timing recovery at receiver.
- Evaluate the capacity and degradation in performance of various symbol signaling schemes in a multipath fading environment.
- Develop & analyze schemes to improve performance in a multipath fading environment including maximal ratio combining, RAKE receivers, OFDM and MIMO.
- Develop and evaluate the performance of aOFDM MIMO scheme to meet specified rate in a given multipath environment.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.

- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Books:

1. John G. Proakis, MasoudSalehi,"Digital Communications ",5e,Pearson Education(2014),ISBN:978-9332535893
2. David Tse, PramodViswanath, "Fundamentals of Wireless Communication",1e,Cambridge University Press(2005), ISBN:0521845270

Reference Books

Simon Haykin ,"Digital Communications Systems",Wiley(2014),ISBN:978-0-471-64735-5

ANTENNA THEORY AND DESIGN
[As per Choice Based Credit System (CBCS) scheme]
SEMESTER – I

Subject Code	**18ECS22**	**IA Marks**	**20**
Number of Lecture Hours/Week	**04**	**Exam Marks**	**80**
Total Number of Lecture Hours	**50 (10 Hours per Module)**	**Exam Hours**	**03**

CREDITS – 04

Course objectives: This course will enable students to:

- Introduce and discuss different types of Antennas, various terminologies, excitations.
- Study different types of Arrays, Pattern-multiplication, Feeding techniques.
- Calculate gain of aperture antennas, Reflector antennas and analyze general feed model.
- Define, describe, and illustrate principle behind antenna synthesis.
- Introduction of Method of moments, Pocklington's integral equation, Source modeling.

Modules	**Revised Bloom's Taxonomy (RBT) Level**
Module -1	
Antenna Fundamentals and Definitions: Radiation Mechanisms, Overview, EM Fundamentals, Solution of Maxwell's Equations for Radiation Problems, Ideal Dipole, Radiation patterns, Directivity and Gain, Antenna impedance, Radiation efficiency, Antenna polarization.	**L1,L2**
Module -2	
Arrays: Array factor for linear arrays, Uniformly excited equally spaced linear arrays, Pattern multiplication, Directivity of linear arrays, Non-uniformly excited equally spaced linear arrays, Mutual coupling. **Antenna Synthesis**: Formulation of the synthesis problem, Synthesis principles, Line sources shaped beam synthesis, Linear array shaped beam synthesis, Fourier series, Woodward - Lawson sampling method, Comparison of shaped beam synthesis methods, low side lobe narrow main beam synthesis methods, Dolph Chebyshev linear array, Taylor line source method.	**L1,L2,L3, L4**
Module -3	
Resonant Antennas: Wires and Patches, Dipole antenna, Yagi-Uda antennas, Micro-strip antenna. **Broadband antennas**: Traveling wave antennas Helical antennas, Biconical antennas, Sleeve antennas, and Principles of frequency independent antennas, Spiral antennas, and Log - periodic antennas.	**L1,L2,L3, L4**

Module -4	
Aperture antennas: Techniques for evaluating gain, Reflector antennas- Parabolic reflector antenna principles, Axi-symmetric parabolic reflector antenna, Offset parabolic reflectors, Dual reflector antennas, Gain calculations for reflector antennas, Feed antennas for reflectors, Field representations, Matching the feed to the reflector, General feed model, Feed antennas used in practice.	**L1,L2,L3, L4**
Module -5	
CEM for antennas: The method of moments: Introduction of the methods moments, Pocklington's integral equation, Integral equation and Kirchhoff's networking equations, Source modeling weighted residual formulations and computational consideration, Calculation of antenna and scatter characteristics.	**L1,L2**

Course Outcomes: After studying this course, students will be able to:

- Classify different types of antennas
- Define and illustrate various types of array antennas
- Design antennas like Yagi-Uda, Helical antennas and other broad band antennas
- Describe different antenna synthesis methods
- Apply methods like MOM

Question paper pattern:

- The question paper will have 10 full questions carrying equal marks.
- Each full question consists of 16 marks with a maximum of four sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- The students will have to answer 5 full questions, selecting one full question from each module.

Text Book:

Stutzman and Thiele, "Antenna Theory and Design", 2nd Edition, John Wiley, 2010.

Reference Books:

1. C. A. Balanis, "Antenna Theory Analysis and Design", John Wiley, 2nd Edition 2007.
2. J. D. Krauss, "Antennas and Wave Propagation", McGraw Hill TMH, 4th Edition, 2010.
3. A.R.Harish, M.Sachidanada, "Antennas and propagation", Pearson Education, 2015.

ERROR CONTROL CODING
[As per Choice Based Credit System (CBCS) Scheme]
SEMESTER – 2

Subject Code	**18ECS23**	**CIE Marks**	**20**
Number of Lecture Hours/Week	**04**	**SEE marks**	**80**
Total Number of Lecture Hours	**50 (10 Hours per Module)**	**Exam Hours**	**03**

CREDITS – 04

Course objectives: This course will enable students to:

- Understand the concept of the Entropy, information rate and capacity for the Discrete memoryless channel.
- Apply modern algebra and probability theory for the coding.
- Compare Block codes such as Linear Block Codes, Cyclic codes etc and Convolutional codes.
- Detect and correct errors for different data communication and storage systems.
- Implement different Block code encoders and decoders.
- Analyze and implement convolutional encoders and decoders.
- Analyze and apply soft and hard Viterbi algorithm for decoding of convolutional codes.

Modules	**RBT Level**
Module 1	
Information theory: Introduction, Entropy, Source coding theorem, discrete memoryless channel, Mutual Information, Channel Capacity Channel coding theorem.(Chap. 5 of Text 1) **Introduction to algebra**: Groups, Fields, binary field arithmetic, Construction of Galois Fields GF (2^m) and its properties, (Only statements of theorems without proof) Computation using Galois filed GF (2^m) arithmetic, Vector spaces and Matrices. (Chap. 2 of Text 2)	L1,L2,L3
Module 2	
Linear block codes: Generator and parity check matrices, Encoding circuits, Syndrome and error detection, Minimum distance considerations, Error detecting and error correcting capabilities, Standard array and syndrome decoding, Single Parity Check Codes (SPC),Repetition codes, Self dual codes, Hamming codes, Reed-Muller codes. Product codes and Interleaved codes. (Chap. 3 of Text 2)	L1,L2,L3
Module 3	
Cyclic codes: Introduction, Generator and parity check polynomials, Encoding of cyclic codes, Syndrome computing and error detection, Decoding of cyclic codes, Error trapping Decoding, Cyclic hamming codes, Shortened cyclic codes.(Chap. 4 of Text2)	L1,L2,L3
Module 4	
BCH codes: Binary primitive BCH codes, Decoding procedures, Implementation of Galois field arithmetic. (Chap. 6 (6.1,6.2,6.7) of Text	

2) Primitive BCH codes over GF (q), **Reed -Solomon codes.** (Chap. 7 (7.2,7.3) of Text 2) **Majority Logic decodable codes**: One -step majority logic decoding, Multiple-step majority logic. (Chap. 8 (8.1,8.4) of Text 2)	L1,L2,L3
Module 5	
Convolution codes: Encoding of convolutional codes: Systematic and Nonsystematic Convolutional Codes, Feedforward encoder inverse, A catastrophic encoder, Structural properties of convolutional codes: state diagram, state table, state transition table, tree diagram, trellis diagram. Viterbi algorithm, Sequential decoding: Log Likelihood Metric for Sequential Decoding. (11.1,11.2, 12.1,13.1 of Text 2)	L1,L2,L3

Course Outcomes: After studying this course, students will be able to:

- Analyse a discrete memoryless channel, given the source and transition probabilities.
- Apply the concept of modern linear algebra for the error control coding technique.
- Construct and Implement efficient LBC, Cyclic codes etc encoder and decoders.
- Apply decoding algorithms for efficient decoding of Block codes and Convolutional codes.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Books:

4. David C.Lay, Steven R.Lay and J.J.McDonald: "LinearAlgebra and its Applications",
   5thEdition, Pearson Education Ltd., 2015
5. Elsgolts, L.:"Differential Equations and Calculus of Variations", MIR Publications, 3rd
   Edition, 1977.
6. T.Veerarajan: "Probability, Statistics and Random Process",3rd Edition,Tata Mc-Graw Hill
   Co.,2016.

Reference Books:

5. Gilbert Strang: Introduction to Linear Algebra, 5thEdition, Wellesley-Cambridge Press., 2016
6. Richard Bronson: "Schaum's Outlines of Theory and Problems of Matrix Operations", McGraw-Hill, 1988.
7. Scott L.Miller,DonaldG.Childers: "Probability and Random Process with application to Signal Processing", Elsevier Academic Press,2nd Edition,2013.
8. E. Kreyszig, "Advanced Engineering Mathematics", 10th edition, Wiley, 2015.

Professional Elective 1

Wireless Sensor Networks **[As per Choice Based Credit System (CBCS) scheme]** **SEMESTER – II**			
Course Code	**18ECS241**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**03**	**SEE Marks**	**60**
Total Number of Lecture Hours	**40 (08 Hours per Module)**	**Exam Hours**	**03**
Credits – 04/03			

Course Outcomes:

At the end of this course, students will be able to

- Design wireless sensor network system for different applications under consideration.
- Understand the hardware details of different types of sensors and select right type of sensor for various applications.
- Understand radio standards and communication protocols to be used for wireless sensor

Modules	RBT Levels
Module-1	
Introduction: Sensor Mote Platforms, WSN Architecture and Protocol Stack (Chap. 1Text 1) **WSN Applications:**Military Applications, Environmental Applications, Health Applications, Home Applications, Industrial Applications, (Chap. 2 Text 1)	L1, L2, L3
Module-2	
Factors InfluencingWSN Design: Hardware Constraints Fault Tolerance Scalability Production Costs WSN Topology, Transmission Media, Power Consumption, (Chap. 3 Text 1) **Physical Layer:** Physical Layer Technologies, Overview of RF Wireless Communication, Channel Coding (Error Control Coding), Modulation, Wireless Channel Effects, PHY Layer Standards (Chap. 4 of Text 1)	L1, L2, L3
Module-3	
Medium Access Control: Challenges for MAC , CSMA Mechanism, Contention-Based Medium Access, Reservation-Based Medium Access, Hybrid Medium Access(Chap. 5 of Text 1) **Network Layer:** Challenges for Routing, Data-centric and Flat-Architecture Protocols, Hierarchical Protocols, Geographical Routing Protocols (Chap. 7 of Text 1)	L1, L2, L3

Module-4	
Transport Layer: Challenges for Transport Layer, Reliable Multi-Segment Transport (RMST) Protocol, Pump Slowly, Fetch Quickly (PSFQ) Protocol, Congestion Detection and Avoidance (CODA) Protocol , Event-to-Sink Reliable Transport (ESRT) Protocol, GARUDA (Chap. 8 Text 1) **Application Layer:** Source Coding (Data Compression), Query Processing, Network Management (Chap. 9 Text 1)	L1, L2, L3
Module-5	
Time Synchronization: Challenges for Time Synchronization , Network Time Protocol, Timing-Sync Protocol for Sensor Networks(TPSN), Reference-Broadcast Synchronization (RBS), Adaptive Clock Synchronization (ACS)(Chap. 11 of Text1) **Localization;** Challenges in Localization, Ranging Techniques, Range-Based Localization Protocols, Range-Free Localization Protocols.(Chap. 12 Text 1)	L1, L2, L3

Course Outcomes: After studying this course, students will be able to:

- Acquire knowledge of characteristics of mobile/wireless communication channels
- Apply statistical models of multipath fading
- Understand the multiple radio access techniques

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as see marks is 60.

Text books:

1. **Ian F. Akyildiz** and **Mehmet Can Vuran** "Wireless Sensor Networks",John Wiley & Sons Ltd. ISBN 978-0-470-03601-3 (H/B), 2010.
2. **Ananthram Swami, et. Al.,** Wireless Sensor Networks Signal Processing and Communications Perspectives", John Wiley & Sons Ltd. ISBN 978-0-470-03557-3 2007.

NANOELECTRONICS

[As per Choice Based Credit System (CBCS) scheme]

SEMESTER – II

Subject Code	**18EVE242**	**CIE**	**40**
Number of Lecture Hours/Week	**04**	**SEE Marks**	**60**
Total Number of Lecture Hours	**50 (10 Hours per Module)**	**Exam Hours**	**03**

CREDITS – 04

Course objectives: This course will enable students to:

- Enhance basic engineering science and technological knowledge of nanoelectron ics.
- Explain basics of top-down and bottom-up fabrication process, devices and systems.
- Describe technologies involved in modern day electronic devices.
- Appreciate the complexities in scaling down the electronic devices in the future.

Modules	**Revised Bloom's Taxonomy (RBT) Level**
Module -1	
Introduction: Overview of nanoscience and engineering. Development milestones in microfabrication and electronic industry. Moores' law and continued miniaturization, Classification of Nanostructures, Electronic properties of atoms and solids: Isolated atom, Bonding between atoms, Giant molecular solids, Free electron models and energy bands, crystalline solids, Periodicity of crystal lattices, Electronic conduction, effects of nanometer length scale, Fabrication methods: Top down processes, Bottom up processes methods for templating the growth of nanomaterials, ordering of nanosystems (Text 1).	**L1, L2**
Module -2	
Characterization: Classification, Microscopic techniques, Field ion microscopy, scanning probe techniques, diffraction techniques: bulk and surface diffraction techniques,spectroscopy techniques: photon, radiofrequency, electron, surface analysis and dept profiling: electron, mass, Ion beam, Reflectrometry, Techniques for property measurement: mechanical, electron, magnetic, thermal properties(Text1)	**L1,L2,L3**
Module -3	

Inorganic semiconductor nanostructures: overview of semiconductor physics. Quantum confinement in semiconductor nanostructures: quantum wells, quantum wires, quantum dots, super-lattices, band offsets, electronic density of states (Text1). **Carbon Nanostructures:**Carbon molecules, Carbon Clusters, Carbon Nanotubes, application of Carbon Nanotubes (Text 2).	**L1-L3**
Module -4	
Fabrication techniques: Requirements of ideal semiconductor, epitaxial growth of quantum wells, lithography and etching, cleaved-edge over growth, growth of vicinal substrates, strain induced dots and wires, electrostatically induced dots and wires, Quantum well width fluctuations, thermally annealed quantum wells, semiconductor nanocrystals, collidal quantum dots, self-assembly techniques. **Physical processes:** modulation doping, quantum hall effect, resonant tunneling, charging effects, ballistic carrier transport, Inter band absorption, intra band absorption, Light emission processes, phonon bottleneck, quantum confined stark effect, nonlinear effects, coherence and dephasing, characterization of semiconductor nanostructures: optical electrical and structural (Text1).	**L1-L3**
Module -5	
Methods of measuring properties: atomic, crystollography, microscopy, spectroscopy (Text 2). **Applications**: Injection lasers, quantum cascade lasers, single-photon sources, biological tagging, optical memories, coulomb blockade devices, photonic structures, QWIP's, NEMS, MEMS (Text1).	**L1-L3**

Course outcomes: After studying this course, students will be able to:

- Know the principles behind Nanoscience engineering and Nanoelectronics.
- Apply the knowledge to prepare and characterize nanomaterials.
- Know the effect of particles size on mechanical, thermal, optical and electrical properties of nanomaterials.
- Design the process flow required to fabricate state of the art transistor technology.
- Analyze the requirements for new materials and device structure in the future technologies.

Question paper pattern:

- The question paper will have 10 full questions carrying equal marks.
- Each full question consists of 16 marks with a maximum of four sub questions.
- There will be 2 full questions from each module covering all the topics of the module
- The students will have to answer 5 full questions, selecting one full question from each module.

Text Books:

1. Ed Robert Kelsall, Ian Hamley, Mark Geoghegan, "Nanoscale Science and Technology", John Wiley, 2007.
2. Charles P Poole, Jr, Frank J Owens, "Introduction to Nanotechnology", John Wiley, Copyright 2006, Reprint 2011.

Reference Book:

Ed William A Goddard III, Donald W Brenner, Sergey E. Lyshevski, Gerald J Iafrate, "Hand Book of Nanoscience Engineering and Technology", CRC press, 2003.

CRYPTOGRAPHY AND NETWORK SECURITY
[As per Choice Based credit System (CBCS) Scheme]
SEMESTER – II

Subject Code	**18ECS243**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**04**	**SEE Marks**	**60**
Total Number of Lecture Hours	**50 (10 Hours Per Module)**	**Exam Hours**	**03**

CREDITS – 04

Course Objectives: This course will enable students to:

- Understand the basics of symmetric key and public key cryptography.
- Understand some basic mathematical concepts and pseudorandom number generators required for cryptography.
- Authenticate and protect the encrypted data.
- Enrich knowledge about Email, IP and Web security.

Modules	**RBT Level**
Module 1	
Foundations: Terminology, Steganography, substitution ciphers and transpositions ciphers, Simple XOR, One-Time Pads, Computer Algorithms (Text 2: Chapter 1: Section 1.1 to 1.6) **SYMMETRIC CIPHERS:** Traditional Block Cipher structure, Data encryption standard (DES), The AES Cipher. (Text 1: Chapter 2: Section2.1, 2.2, Chapter 4)	L1,L2,L3
Module 2	
Introduction to modular arithmetic, Prime Numbers, Fermat's and Euler's theorem, primality testing, Chinese Remainder theorem, discrete logarithm. (Text 1: Chapter 7: Section 1, 2, 3, 4, 5) Principles of Public-Key Cryptosystems, The RSA algorithm, Diffie - Hellman Key Exchange, Elliptic Curve Arithmetic, Elliptic Curve Cryptography (Text 1: Chapter 8, Chapter 9: Section 9.1, 9.3, 9.4)	L1,L2,L3
Module 3	
Pseudo-Random-Sequence Generators and Stream Ciphers: Linear Congruential Generators, Linear Feedback Shift Registers, Design and analysis of stream ciphers, Stream ciphers using LFSRs, A5, Hughes XPD/KPD, Nanoteq, Rambutan, Additive generators, Gifford, Algorithm M, PKZIP (Text 2: Chapter 16)	L1,L2, L3
Module 4	
One-Way Hash Functions: Background, Snefru, N-Hash, MD4, MD5, Secure Hash Algorithm [SHA],One way hash functions using symmetric block algorithms, Using public key algorithms, Choosing a one-way hash functions, Message Authentication Codes. Digital Signature Algorithm, Discrete Logarithm Signature Scheme (Text 2: Chapter 18: Section 18.1 to 18.5, 18.7, 18.11 to 18.14 and Chapter 20: Section 20.1, 20.4)	L1,L2,L3

Module 5	
E-mail Security: Pretty Good Privacy-S/MIME (Text 1: Chapter 17: Section 17.1, 17.2). **IP Security:** IP Security Overview, IP Security Policy, Encapsulation Security Payload (ESP), Combining security Associations. (Text 1: Chapter 18: Section 18.1 to 18.4). **Web Security:** Web Security Considerations, SSL (Text 1: Chapter 15: Section 15.1, 15.2).	L1,L2, L3

Course Outcomes: After studying this course, students will be able to:

- Use basic cryptographic algorithms to encrypt the data.
- Generate some pseudorandom numbers required for cryptographic applications.
- Provide authentication and protection for encrypted data.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Books:

1. William Stallings , "Cryptography and Network Security Principles and Practice", Pearson Education Inc., 6th Edition, 2014, ISBN: 978-93-325-1877-3

2. Bruce Schneier, "Applied Cryptography Protocols, Algorithms, and Source code in C", Wiley Publications, 2nd Edition, ISBN: 9971-51-348-X

Reference Books:

1. Cryptography and Network Security, Behrouz A. Forouzan, TMH, 2007.
2. Cryptography and Network Security, Atul Kahate, TMH, 2003.

Professional Elective 2

MULTIMEDIA OVER COMMUNICATION LINKS [As per Choice Based credit System (CBCS) Scheme] SEMESTER – II			
Subject Code	**18ECS251**	**CIE Marks**	**20**
Number of Lecture Hours/Week	**04**	**SEE Marks**	**80**
Total Number of Lecture Hours	**50 (10 Hours Per Module)**	**Exam Hours**	**03**
CREDITS – 04			

Course Objectives: This course will enable students to:

- Gain fundamental knowledge in understanding the basics of different multimedia networks, applications, media types like text and image.
- Analyse media types like audio and video and gain knowledge on multimedia systems.
- Analyse Audio compression techniques required to compress Audio.
- Analyse compression techniques required to compress video.
- Gain fundamental knowledge about the Multimedia Communications in different Networks.

Modules	**RBT Level**
Module 1	
Multimedia Communications: Introduction, Multimedia information representation, multimedia networks, multimedia applications, Application and networking terminology.(Chap. 1 of Text1) **Information Representation**: Introduction, Text, Images. (Chap. 2- Sections 2.2 and 2.3 of Text 1)	L1, L2, L3
Module 2	
Information Representation: Audio and Video. (Chap. 2 - Sections 2.4 and 2.5 of Text 1) **Distributed multimedia systems**: Introduction, main Features of a DMS, Resource management of DMS, Networking, Multimedia operating systems. (Chap. 4 - Sections 4.1 to 4.5 of Text 2)	L1,L2, L3
Module 3	
Multimedia Processing in Communication: Introduction, Perceptual coding of digital Audio signals, Transform Audio Coders, Audio Sub band Coders. (Chap. 3 - Sections 3.1, 3.2, 3.6, 3.7 of Text 2)	L1,L2, L3
Module 4	
Multimedia Communication Standards: Introduction, MPEG approach to multimedia standardization, MPEG-1, MPEG-2, Overview of MPEG-4. (Chap. 5 - Sections 5.1 to 5.4 and 5.5.1 of	L1,L2, L3

Text 2)	
Module 5	
Multimedia Communication Across Networks: Packet audio/video in the network environment, Video transport across generic networks, Multimedia Transport across ATM Networks. (Chap. 6 - Sections 6.1, 6.2, 6.3 of Text 2).	L1,L2, L3

Course Outcomes: After studying this course, students will be able to:

- Understand basics of different multimedia networks and applications.
- Analyze media types like audio and video to represent in digital form.
- Understand different compression techniques to compress audio.
- Understand different compression techniques to compress audio video.
- Describe the basics of Multimedia Communication Across Networks

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Books:

1. Fred Halsall, “Multimedia Communications”, Pearson education, 2001, ISBN -9788131709948.
2. K. R. Rao, Zoran S. Bojkovic, Dragorad A. Milovanovic, “Multimedia Communication Systems”, Pearson education, 2004. ISBN - 9788120321458.

Reference Book:

Raif steinmetz, Klara Nahrstedt, “Multimedia: Computing, Communications and Applications”, Pearson education, 2002, ISBN -9788177584417.

STATISTICAL SIGNAL PROCESSING
[As per Choice Based Credit System (CBCS) scheme]
SEMESTER – II

Course Code	**18ESP252**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**04**	**SEE Marks**	**60**
Total Number of Lecture Hours	**50 (10 Hours per Module)**	**Exam Hours**	**03**

Credits – 04

Course objectives: This course will enable students to:

- Understand random processes and its properties
- Understand the basic theory of signal detection and estimation
- Identify the engineering problems that can be put into the frame of statistical signal processing
- Solve the identified problems using the standard techniques learned through this course,
- Make contributions to the theory and the practice of statistical signal processing.

Modules	RBT Levels
Module-1	
Random Processes: Random variables, random processes, white noise, filtering random processes, spectral factorization, ARMA, AR and MA processes(Text 1).	**L1, L2**
Module-2	
Signal Modeling: Least squares method, Padé approximation, Prony's method, finite data records, stochastic models, Levinson-Durbin recursion; Schurrecursion; Levinsonrecursion(Text 1).	**L2, L3**
Module-3	
Spectrum Estimation: Nonparametric methods, minimum-variance spectrum estimation, maximum entropy method, parametric methods, frequency estimation, principal components spectrum estimation(Text 1).	**L1, L2**
Module-4	
Optimal and Adaptive Filtering: FIR and IIR Wiener filters, Discrete Kalman filter, FIR Adaptive filters: Steepest descent, LMS, LMS-based algorithms (Text 1).	**L2, L3**
Module-5	
Array Processing: Array fundamentals, beam-forming, optimum array processing, performance considerations, adaptive beam-forming, linearly constrained minimum-variance beam-formers, side-lobe cancellers. (Text 2).	**L2, L3**

Course outcomes: After studying this course, students will be able to:

- Characterize an estimator.
- Design statistical DSP algorithms to meet desired needs
- Apply vector space methods to statistical signal processing problems
- Understand Wiener filter theory and design discrete and continuous Wiener filters
- Understand Kalman Filter theory and design discrete Kalman filters
- Use computer tools (such as Matlab) in developing and testing stochastic DSP algorithms

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Book:

1. Monson H.Hayes, "Statistical Digital Signal Processing and Modeling", John Wiley & Sons (Asia) Pvt.Ltd., 2002.
2. Dimitris G. Manolakis, Vinay K. Ingle, and Stephen M. Kogon, "Statistical and Adaptive Signal Processing: Spectral Estimation, Signal Modeling, Adaptive Filtering and Array Processing" ,McGraw-HillInternationalEdition,2000.

MICRO ELECTRO MECHANICAL SYSTEMS
[As per Choice Based credit System (CBCS) Scheme]
SEMESTER – II

Subject Code	**18ELD253**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**04**	**SEE Marks**	**60**
Total Number of Lecture Hours	**50 (10 Hours per Module)**	**Exam Hours**	**03**

CREDITS – 04

Course Objectives: This course will enable students to:

- Know an overview of microsystems, their fabrication and application areas.
- Teach working principles of several MEMS devices.
- Develop mathematical and analytical models of MEMS devices
- Know methods to fabricate MEMS devices
- Expose the students to various application areas where MEMS devices can be used.

Modules	**RBT Level**
Module 1	
Overview of MEMS and Microsystems: MEMS and Microsystem, Typical MEMS and Microsystems Products, Evolution of Microfabrication, Microsystems and Microelectronics, Multidisciplinary Nature of Microsystems, Miniaturization. Applications and Markets.	L1, L2
Module 2	
Working Principles of Microsystems: Introduction, Microsensors, Microactuation, MEMS with Microactuators, Microaccelerometers, Microfluidics. **Engineering Science for Microsystems Design and Fabrication:** Introduction, Atomic Structure of Matters, Ions and Ionization, Molecular Theory of Matter and Inter-molecular Forces, Doping of Semiconductors, The Diffusion Process, Plasma Physics, Electrochemistry.	L1, L2
Module 3	
Engineering Mechanics for Microsystems Design: Introduction, Static Bending of Thin Plates, Mechanical Vibration, Thermomechanics, Fracture Mechanics, Thin Film Mechanics, Overview on Finite Element Stress Analysis.	L1,L2,L3
Module 4	
Scaling Laws in Miniaturization:	L1,L2,L3

Introduction, Scaling in Geometry, Scaling in Rigid-Body Dynamics, Scaling in Electrostatic Forces, Scaling of Electromagnetic Forces, Scaling in Electricity, Scaling in Fluid Mechanics, Scaling in Heat Transfer.	
Module 5	
Overview of Micro-manufacturing: Introduction, Bulk Micro-manufacturing, Surface Micromachining, The LIGA Process, Summary on Micro-manufacturing. **Microsystem Design:** Introduction, Design Considerations, Process Design, Mechanical Design, Using Finite Element Method.	L1,L2,L3

Course Outcomes: After studying this course, students will be able to:

- Understand the technologies related to Micro Electro Mechanical Systems.
- Describe the design and fabrication processes involved with MEMS devices.
- Analyse the MEMS devices and develop suitable mathematical models
- Understand the various application areas for MEMS devices

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Book:

Tai-Ran Hsu, MEMS and Micro systems: Design, Manufacture and Nanoscale Engineering, 2nd Ed, John Wiley & Sons, 2008. ISBN: 978-0-470-08301-7

Reference Books:

1. Hans H. Gatzen, Volker Saile, JurgLeuthold, Micro and Nano Fabrication: Tools and Processes, Springer, 2015.
2. Dilip Kumar Bhattacharya, Brajesh Kumar Kaushik, Micro electromechanical Systems (MEMS), Cenage Learning.

ADVANCED COMMUNICATION LAB
[As per Choice Based Credit System (CBCS) scheme]
SEMESTER – II

Laboratory Code	**18ECSL26**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**01Hr Tutorial (Instructions)+ 03 Hours Laboratory**	**SEE Marks**	**60**
		Exam Hours	**03**

CREDITS – 02

Course objectives: This laboratory course enables students to get practical experience in

- Radiation pattern of antennas.
- Determining gain and directivity of a given antenna.
- Working of Klystron source.
- S-parameters of some microwave passive devices.

Laboratory Experiments: **NOTE:** Experiments can be done using Hardware tools such as Spectrum analyzers, Signal sources, Power Supplies, Oscilloscopes, High frequency signal sources, Fiber optic kits, Microwave measurement benches, DSP processor kit, FPGA kit, Logic analyzers, PC setups, etc. Software tools based experiments can be done using, FEKO or equivalent open source simulator, MATLAB etc.	**Revised Bloom's Taxonomy (RBT) Level**
1. Matlab/C implementation to obtain the radiation pattern of an antenna.	L3,L4
2. Study of radiation pattern of different antennas.	L2, L3
3. Determine the directivity and gains of Horn/ Yagi/ dipole/ Parabolic antennas.	L3,L4
4. Impedance measurements of Horn/Yagi/dipole/Parabolic antennas.	L3,L4
5. Study of radiation pattern of E & H plane horns.	L2, L3
6. Significance of Pocklington's integral equation.	L1,L2
7. Study of digital modulation techniques using CD4051 IC.	L2, L3
8. Conduct an experiment for Voice and data multiplexing using optical fiber.	L3,L4
9. Determination of the modes transit time, electronic timing range and sensitivity of Klystron source.	L3, L4
10. Determination of VI characteristics of GUNN diode, and measurement of guide wave length, frequency, and VSWR.	L3,L4
11. Determination of coupling coefficient and insertion loss of directional couplers and Magic tree.	L3,L4
12. Build a hardware pseudo-random signal source and determine statistics of the generated signal source.	L1,L2,L3,L4

Course outcomes: On the completion of this laboratory course, the students will be able to:

- Plot the radiation pattern of some antennas using Matlab and wave guide setup
- Obtain the S-parameters of Magic tee and directional couplers.
- Test the IC CD4051 for modulation techniques.
- Study multiplexing techniques using OFC kit.

Conduct of Practical Examination:

1. All laboratory experiments are to be included for practical examination.
2. Students are allowed to pick one experiment from the lot.
3. Strictly follow the instructions as printed on the cover page of answer script for breakup of marks.
4. Change of experiment is allowed only once and Marks allotted to the procedure part to be made zero.

THIRD SEMESTER SYLLABUS

LTE 4G Broadband **[As per Choice Based Credit System (CBCS) Scheme]** **SEMESTER – III**			
Subject Code	**18ECS31**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**04**	**SEE Marks**	**60**
Total Number of Lecture Hours	**50 (10 Hours Per Module)**	**Exam Hours**	**03**
CREDITS – 04			

Course objectives: This course will enable students to:

- Explain the system architecture of LTE and E-UTRAN as per the standards
- Understand the Multiple Access process incorporated in the radio physical layer.
- Associate MAC of LTE radio interface protocols to set up, reconfigure and release the Radio Bearer and for transferring to the EPS bearer.
- Explain the mobility principles and procedures in the idle and active state.
- Analyse the main factors affecting LTE performance including mobile speed and

Modules	**RBT Level**
Module -1	
Evolution Beyond Release 8, LTE-Advanced for IMT-Advanced, LTE Specifications and 3GPP Structure. **System Architecture Based on 3GPP SAE:** Basic System Architecture Configuration with only E-UTRAN Access Network, System Architecture with E-UTRAN and Legacy 3GPP Access Networks, System Architecture with E-UTRAN and Non-3GPP Access Networks, IMS Architecture, PCC and QoS.	**L2, L3**
Module -2	
Introduction to OFDMA, SC-FDMA and MIMO in LTE: LTE Multiple Access Background, OFDMA Basics, SC-FDMA Basics MIMO Basics. **Physical Layer:** Transport Channels and their Mapping to the Physical Channels, Modulation, Uplink User Data Transmission, Downlink User Data Transmission, Uplink Physical Layer Signaling Transmission, PRACH Structure, Downlink Physical Layer Signaling Transmission.	**L2, L3**
Module -3	

Physical Layer Procedures, UE Capability Classes and Supported Features Physical Layer Measurements and Parameter Configuration. **LTE Radio Protocols:** Protocol Architecture, The Medium Access Control The Radio Link Control Layer, Packet Data Convergence Protocol.	**L1, L2, L3**
Module -4	
Radio Resource Control (RRC): X2 Interface Protocols Understanding the RRC ASN.1 Protocol Definition, Early UE Handling in LTE. **Mobility:** Mobility Management in Idle State, Intra-LTE Handovers 190, Inter-system Handovers Differences in E-UTRAN and UTRAN Mobility.	**L2, L3**
Module -5	
Radio Resource Management: Overview of RRM Algorithms, Admission Control and QoS Parameters, Downlink Dynamic Scheduling and Link Adaptation, Uplink Dynamic Scheduling and Link Adaptation, Interference Management and Power Settings, Discontinuous Transmission and Reception (DTX/DRX), RRC Connection Maintenance. **Performance:** Layer 1 Peak Bit Rates, Terminal Categories Link Level Performance, Link Budgets Spectral Efficiency Latency, LTE Reframing to GSM Spectrum Dimensioning.	**L1, L2, L3**

Course outcomes:

- Understand the system architecture and the function standard specified components of the system of LTE 4G.
- Analyze the role of LTE radio interface protocols and EPS Data convergence protocols to set up, reconfigure and release data and voice from a number of users.
- Demonstrate the UTRAN and EPS handling processes from set up to release including mobility management for a variety of data call scenarios.
- Test and Evaluate the Performance of resource management and packet data processing and transport algorithms.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Book:

'LTE for UMTS Evolution to LTE-Advanced' Harri Holma and Antti Toskala, Second Edition - 2011, John Wiley & Sons, Ltd. Print ISBN: 9780470660003.

Reference Books:

1. 'Fundamentals of LTE', by Arunabha Ghosh, Jun Zhang, Jeffrey G. Andrews), Rias Muhamed, 1st Edition, Sept 2010, Prentice Hall Communications Engineering and Emerging Technologies Series from Ted Rappaport,ISBN13: 9780137033119, ISBN10: 0137033117.
2. ' LTE – The UMTS Long Term Evolution ; From Theory to Practice' by Stefania Sesia, Issam Toufik, and Matthew Baker, 2009 John Wiley & Sons Ltd, ISBN 978-0-470-69716-0.

Professional Elective 3

Advances in Image Processing **[As per Choice Based credit System (CBCS) Scheme** **SEMESTER – III**			
Subject Code	**18ECS321**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**04**	**SEE marks**	**60**
Total Number of Lecture Hours	**50 (10 Hours Per Module)**	**Exam Hours**	**03**
CREDITS – 04			

Course Objectives: This course will enable students to:

1. Acquire fundamental knowledge in understanding the representation of the digital image and its properties
2. Equip with some pre-processing techniques required to enhance the image for further analysis purpose.
3. Select the region of interest in the image using segmentation techniques.
4. Represent the image based on its shape and edge information.
5. Describe the objects present in the image based on its properties and structure.

Modules	**RBT Level**
Module 1	
The image, its representations and properties: Image representations a few concepts, Image digitization, Digital image properties, Color images.	L1
Module 2	
Image Pre-processing: Pixel brightness transformations, geometric transformations, local pre-processing.	L1, L2
Module 3	
Segmentation: Thresholding; Edge-based segmentation – Edge image thresholding, Edge relaxation, Border tracing, Hough transforms; Region – based segmentation – Region merging, Region splitting, Splitting and merging, Watershed segmentation, Region growing post-processing.	L1, L2, L3
Module 4	
Shape representation and description: Region identification; Contour-based shape representation and description – Chain codes, Simple geometric border representation, Fourier transforms of boundaries, Boundary description using segment sequences, B-spline representation; Region-based shape representation and description – Simple scalar region descriptors, Moments, Convex hull.	L1, L2, L3
Module 5	
Mathematical Morphology: Basic morphological concepts, Four morphological principles, Binary dilation and erosion, Skeletons	L1, L2, L3

and object marking, Morphological segmentations and watersheds.	

Course Outcomes: After studying this course, students will be able to:

1.Understand the representation of the digital image and its properties
2.Apply pre-processing techniques required to enhance the image for its further analysis.
3.Use segmentation techniques to select the region of interest in the image for analysis
4.Represent the image based on its shape and edge information.
5.Describe the objects present in the image based on its properties and structure.
6.Use morphological operations to simplify images, and quantify and preserve the main shape characteristics of the objects.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Books:

1. Milan Sonka, Vaclav Hlavac, Roger Boyle, “Image Processing, Analysis, and Machine Vision”, Cengage Learning, 2013, ISBN: 978-81-315-1883-0

Reference Books:

1. Geoff Doughertry, Digital Image Processing for Medical Applications, Cambridge university Press, 2010
2. S.Jayaraman, S Esakkirajan, T.Veerakumar, Digital Image Processing, Tata McGraw Hill, 2011.

Array Signal Processing **[As per Choice Based Credit System (CBCS) scheme]** **SEMESTER – III**			
Course Code	**18ESP322**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**04**	**SEE Marks**	**60**
Total Number of Lecture Hours	**50 (10 Hours per Module)**	**Exam Hours**	**03**
Credits – 04			

Course Objectives: This course will enable students to:

- Understand various aspects of array signal processing.
- Explain the Concepts of Spatial Frequency along with the Spatial Samplings
- Describe array design methods and direction of arrival estimation techniques.

Modules	**RBT Level**
Module 1	
Spatial Signals: Signals in space and time, Spatial Frequency Vs Temporal Frequency, Review of Co-ordinate Systems, Maxwell's Equation, Wave Equation. Solution to Wave equation in Cartesian Co-ordinate system –Wave number vector, Slowness vector.	**L1,L2**
Module 2	
Wave number-Frequency Space Spatial Sampling: Spatial Sampling Theorem-Nyquist Criteria, Aliasing in Spatial frequency domain, Spatial sampling of multidimensional signals.	**L1,L2**
Module 3	
Sensor Arrays: Linear Arrays, Planar Arrays, Frequency – Wave number Response and Beam pattern, Array manifold vector, Conventional Beam former, Narrowband beam former.	**L1,L1**
Module 4	
Uniform Linear Arrays: Beam pattern in θ, u and ψ -space, Uniformly Weighted Linear Arrays. **Beam Pattern Parameters:** Half Power Beam Width, Distance to First Null, Location of side lobes and Rate of Decrease, Grating Lobes, Array Steering.	**L1,L1**
Module 5	
Array Design Methods: Visible region, Duality between Time - Domain and Space -Domain Signal Processing, Schelkunoff's Zero Placement Method, Fourier Series Method with windowing, Woodward -Lawson Frequency-Sampling Design.	**L2,L3**

Non parametric method -Beam forming, Delay and sum Method, Capons Method.	

Course Outcomes: At the end of the course, the students will be able to

- Understand the important concepts of array signal processing
- Understand the various array design techniques
- Understand the basic principle of direction of arrival estimation techniques

Question paper pattern:

- The question paper will have 10 full questions carrying equal marks.
- Each full question consists of 16 marks with a maximum of four sub questions.
- There will be 2 full questions from each module covering all the topics of the module
- The students will have to answer 5 full questions, selecting one full question from each module.

Text Book:

1. Harry L. Van Trees "Optimum Array Processing Part IV of Detection, Estimation, and Modulation Theory" John Wiley & Sons, 2002, ISBN: 9780471093909.

Reference Books:

1. Don H. Johnson Dan E. Dugeon, "Array Signal Processing: Concepts and Techniques", Prentice Hall Signal Processing Series, 1st Edition ,ISBN-13: 978-0130485137.
2. Petre Stoica and Randolph L. Moses "Spectral Analysis of Signals" Prentice Hall, 2005,ISBN: 0-13-113956-8.
3. Sophocles J. Orfanidis, "Electromagnetic Waves and Antennas", ECE Department Rutgers University, 94 Brett Road Piscataway, NJ 08854-8058. http://www.ece.rutgers.edu/~orfanidi/ewa/

Real Time Systems **[As per Choice Based credit System (CBCS) Scheme** **SEMESTER – III**			
Subject Code	**18ECS323**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**04**	**SEE Marks**	**60**
Total Number of Lecture Hours	**50 (10 Hours Per Module)**	**Exam Hours**	**03**

CREDITS – 04

Course Objectives: This course will enable students to:

- Understand basics of Real Time systems.
- Distinguish a real-time system with other systems.
- Identify the functions of operating system
- Evaluate the need for Real time operating system.
- Design and develop embedded applications by means of real-time operating systems.

Modules	**RBT Level**
Module 1	
Introduction to Real-Time Embedded Systems: Brief history of Real Time Systems, A brief history of Embedded Systems. **System Resources:** Resource Analysis, Real-Time Service Utility, Scheduling Classes, The Cyclic Executive, Scheduler Concepts, Preemptive Fixed Priority Scheduling Policies, Real-Time OS, Thread Safe Re-entrant Functions.	L1, L2
Module 2	
Processing: Preemptive Fixed-Priority Policy, Feasibility, Rate Montonic least upper bound, Necessary and Sufficient feasibility, Deadline – Monotonic Policy, Dynamic priority policies. **I/O Resources:** Worst-case Execution time, Intermediate I/O, Execution efficiency, I/O Architecture. **Memory:** Physical hierarchy, Capacity and allocation, Shared Memory, ECC Memory, Flash file systems.	L1, L2
Module 3	
Multi-resource Services: Blocking, Deadlock and livestock, Critical sections to protect shared resources, priority inversion. **Soft Real-Time Services:** Missed Deadlines, QoS, Alternatives to rate monotonic policy, Mixed hard and soft real-time services.	L1, L2
Module 4	
Embedded System Components: Firmware components, RTOS system software mechanisms, Software application components. **Debugging Components:** Exceptions assert, Checking return codes, Single-step debugging, kernel scheduler traces, Test access ports, Trace ports, Power-On self test and diagnostics.	L1, L2, L3

Module 5	
Performance Tuning: Basic concepts of drill-down tuning, hardware – supported profiling and tracing, Building performance monitoring into software, Path length. **High availability and Reliability Design:** Reliability and Availability, Similarities and differences, Reliability, Reliable software, Available software, Design tradeoffs, Hierarchical applications for Fail-safe design.	L1, L2, L3

Course Outcomes: After studying this course, students will be able to:

- Analyze Real time operating systems.
- Describe the functions of Real time operating systems.
- Demonstrate embedded system applications.
- Design a Real Time operating system.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Book:

Sam Siewert, "Real-Time Embedded Systems and Components", Cengage Learning India Edition, 2007.

Reference Books:

1. Krishna CM and Kang Singh G, "Real time systems", Tata McGraw Hill, 2003, ISBN: 0-07-114243-64
2. Qing Li and Carolyn Yao, "Real-Time Concepts for Embedded Systems", CMP Books, 2003, ISBN:1578201241
3. Jane W. S. Liu, "Real Time Systems", Prentice Hall, 2000, ISBN: 0130996513
4. Phillip A. Laplante, "Real-Time Systems Design and Analysis", John Wiley & Sons, 2004.

Professional Elective 4

RF AND MICROWAVE CIRCUIT DESIGN [As per Choice Based Credit System (CBCS) Scheme] SEMESTER – III			
Subject Code	**18ECS331**	**IA Marks**	**40**
Number of Lecture Hours/Week	**04**	**Exam marks**	**60**
Total Number of Lecture Hours	**50 (10 Hours per Module)**	**Exam Hours**	**03**
CREDITS – 04			

Course Objectives: This course will enable students to

- Understand waves propagating in Networks.
- Use the Smith Chart for various applications.
- Understand the basic considerations in active networks
- Design active networks.
- Understand RF/MW Frequency Mixer and Phase Shifter Design

Modules	**RBT Level**
Module 1	
Wave propagation in networks: Introduction, Reasons for Using RF/Microwaves, Applications, RF Waves, RF and Microwave circuit design, Introduction to Components Basics, Analysis of Simple Circuit in Phasor Domain, RF Impedance Matching, Transmission Media, High Frequency Parameters, Formulation of S-parameters, Properties of S-Parameters, Transmission Matrix, Generalized S-parameters.	L1,L2
Module 2	
Smith chart and its Applications: Introduction, Smith Chart, Derivation of Smith Chart, Smith Chart Circular and Radial Scales, Application of Smith chart.	L1,L2
Module 3	
Basic consideration in active networks: Stability Considerations, Gain Considerations and Noise Considerations.	L1,L2
Module 4	
RF/Microwave Amplifiers: Small Signal Design: Introduction, Types of amplifier, Design of different types of amplifiers **RF/Microwave Frequency Conversion: Mixers**: Introduction, Mixer Types, Conversion Losses for SSB Mixers, SSB versus DSB mixers, One diode mixers, Two diode Mixers.	L1,L2,L3
Module 5	
RF/Microwave Control Circuit Design: Introduction, PN Junction Devices, Phase shifters, Digital phase shifters,	L1,L2,L3

Semiconductor phase shifters, PIN diode attenuators. **RF and Microwave IC design**: MICs, MIC materials, Types of MICs, Hybrid verses Monolithic ICs, Chip mathematics	

Course Outcomes: After studying this course, students will be able to:

- Discuss and analyse waves propagation in Networks
- Apply the Smith Chart for finding various parameters in transmission lines
- Analyse the basic considerations in active networks
- Describe and design active networks
- Design RF/MW Frequency Mixers and phase shifters

Question paper pattern:

- The question paper will have 10 full questions carrying equal marks.
- Each full question consists of 16 marks with a maximum of four sub questions.
- There will be 2 full questions from each module covering all the topics of the module
- The students will have to answer 5 full questions, selecting one full question from each module.

Text Book:

Matthew M. Radmanesh, "RF and Microwave Electronics Illustrated", Pearson Education edition, 2004.

Reference Book:

Reinhold Ludwig, and Pavel Bretchko, "RF circuit design theory and applications", Pearson Education edition, 2004.

PATTERN RECOGNITION and MACHINE LEARNING **[As per Choice Based Credit System (CBCS) scheme]** **SEMESTER – III**			
Course Code	**18ESP332**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**04**	**SEE Marks**	**60**
Total Number of Lecture Hours	**50 (10 Hours per Module)**	**Exam Hours**	**03**
Credits – 04			

Course objectives: The objective of the course is to discusses main and modern concepts for model selection and parameter estimation in recognition, decision making and statistical learning problems. Special emphasis will be given to regression, classification, regularization, feature selection and density estimation in supervised mode of learning.

Modules	**RBT Levels**
Module-1	
Introduction: Probability Theory, Model Selection, The Curse of Dimensionality, Decision Theory, Information Theory **Distributions:** Binary and Multinomial Variables, The Gaussian Distribution, The Exponential Family, Nonparametric Methods.**(Ch.: 1,2)**	**L1,L2**
Module-2	
Supervised Learning **Linear Regression Models:** Linear Basis Function Models, The Bias-Variance Decomposition, Bayesian Linear Regression, Bayesian Model Comparison **Classification & Linear Discriminant Analysis:** Discriminant Functions, Probabilistic Generative Models, Probabilistic Discriminative Mode**(Ch. :3,4)**	**L1,L2,L3**
Module-3	
Supervised Learning **Kernels:** Dual Representations, Constructing Kernels, Radial Basis Function Network, Gaussian Processes **Support Vector Machines:** Maximum Margin Classifiers, Relevance Vector Machines **Neural Networks:** Feed-forward Network, Network Training, Error Backpropagation**(Ch:5,6,7)**	**L1,L2,L3**
Module-4	
Unsupervised Learning: **Mixture Models:** K-means Clustering, Mixtures of Gaussians, Maximum likelihood, EM for Gaussian mixtures, Alternative View of EM. **Dimensionality Reduction:** Principal Component Analysis,	**L1,L2,L3**

Factor/Component Analysis, Probabilistic PCA, Kernel PCA, Nonlinear Latent Variable Models **(Ch.: 9,12)**	
Module-5	
Probabilistic Graphical Models: Bayesian Networks, Conditional Independence, Markov Random Fields, Inference in Graphical Models, Markov Model, Hidden Markov Models **(Ch.:8,13)**	**L1,L2,L3**

Course Outcomes: At the end of this course, students will be able to

- Identify areas where Pattern Recognition and Machine Learning can offer a solution.
- Describe the strength and limitations of some techniques used in computational Machine Learning for classification, regression and density estimation problems.
- Describe and model data.
- Solve problems in Regression and Classification.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Book:

1. Pattern Recognition and Machine Learning. Christopher Bishop. Springer, 2006

IoT

[As per Choice Based Credit System (CBCS) scheme]

SEMESTER – III

Course Code	**18ECS333**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**04**	**SEE Marks**	**60**
Total Number of Lecture Hours	**50 (10 Hours per Module)**	**Exam Hours**	**03**

Credits – 04

Course objectives: This course will enable students to:

- Introduce concept of IOT and its applications in today's scenario.
- Understand IOT content generation and transport through networks
- Understand the devices employed for IOT data acquisition and communication access technologies
- Introduce some use cases of IOT

Module-1	**RBT**
What is IOT Genesis, Digitization, Impact, Connected Roadways, Buildings, Challenges **IOT Network Architecture and Design** Drivers behind new network Architectures, Comparing IOT Architectures, M2M architecture, IOT world forum standard, IOT Reference Model, Simplified IOT Architecture.	**L1, L2**
Module-2	
IOT Network Architecture and Design Core IOT Functional Stack, Layer1(Sensors and Actuators) , Layer 2(Communications Sublayer), Access network sublayer, Gateways and backhaul sublayer, Network transport sublayer, IOT Network management. Layer 3(Applications and Analytics) – Analytics vs Control, Data vs Network Analytics IOT Data Management and Compute Stack	**L2,L3**
Module-3	
Engineering IOT Networks Things in IOT – Sensors, Actuators, MEMS and smart objects. Sensor networks, WSN, Communication protocols for WSN Communications Criteria, Range Frequency bands, power consumption, Topology, Constrained Devices, Constrained Node Networks IOT Access Technologies, IEEE 802.15.4 Competitive Technologies – Overview only of IEEE 802.15.4g, 4e, IEEE 1901.2a Standard Alliances – LTE Cat0, Cat-M, NB-IOT	**L2,L3**

Module-4	
Engineering IOT Networks IP as IOT network layer, Key Advantages, Adoption, Optimization, Constrained Nodes, Constrained Networks, IP versions, Optimizing IP for IOT. Application Protocols for IOT – Transport Layer, Application Transport layer, Background only of SCADA, Generic web based protocols, IOT Application Layer Data and Analytics for IOT – Introduction, Structured and Unstructured data, IOT Data Analytics overview and Challenges.	**L3,L4**
Module-5	
IOT in Industry (Three Use cases) • IOT Strategy for Connected manufacturing, Architecture for Connected Factory • Utilities – Power utility, IT/OT divide, Grid blocks reference model, Reference Architecture, Primary substation grid block and automation. • Smart and Connected cities –Strategy, Smart city network Architecture, Street layer, city layer, Data center layer, services layer, Smart city security architecture, Smart street lighting.	**L3,L4**

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Course Outcomes: After studying this course, students will be able to:

- Understand the basic concepts IOT Architecture and devices employed.
- Analyze the sensor data generated and map it to IOT protocol stack for transport.
- Apply communications knowledge to facilitate transport of IOT data over various available communications media.
- Design a use case for a typical application in real life ranging from sensing devices to analyzing the data available on a server to perform tasks on the device.

Text Book:

Cisco, IOT Fundamentals – Networking Technologies, Protocols, Use Cases for IOT, Pearson Education; First edition (16 August 2017). ISBN-10: 9386873745, ISBN-13: 978-9386873743

Reference Books:

Arshdeep Bahga and Vijay Madisetti, 'Internet of Things – A Hands on Approach', Orient Blackswan Private Limited - New Delhi; First edition (2015), ISBN-10: 8173719543, ISBN-13: 978-8173719547