



COUNCIL OF SCIENTIFIC AND INDUSTRIAL RESEARCH

Human Resource Development Group

CSIR Complex, Library Avenue, Pusa, New Delhi 110 012

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Email: tgsm@csirhrdg.res.in, web <http://csirhrdg.res.in>

Hemant Kulkarni
Senior Principal Scientist

Ref No. SYM/10245/19-HRD

Aug 08, 2019

Dr Ravindra R Malagi
Professor
Dept. of Product Design & Manufacturing
Visvesvaraya Technological University, Belagavi-590 018 Karnataka 9448907847

SUBJECT: 3rd International Conference & Exhibition on Fatigue, Durability & Fracture Mechanics & Symposium on Condition Assessment/ Residual Life Assessment & Extension during Aug 29-31, 2019 at Visvesvaraya Technological University, Belagavi

Dear Dr Malagi

With reference to your application on the above subject, we are happy to inform you that Director General, CSIR has been pleased to sanction a grant of **Rs.100000/- (Rupees One Lakh Only)** subject to the following conditions:

1. The grant received from CSIR should be duly acknowledged by email along with a certificate that the grant would be specifically utilized for the purpose for which it has been sanctioned.
2. The grant may be reimbursed within four months from the date of Conference/Seminar/Workshop etc. is over by filling-in the Grant-in-Aid Bill Form in duplicate duly signed and rubber stamped by the concerned officials, indicating clearly the designation of the official along with Audited Statement of Expenditure for release of grant. Current Proforma for Grant-in-aid bill, Audited Statement of Expenditure and NEFT are available on our website URL <http://csirhrdg.res.in/Home/Index/1/InPage/53/14>, If any Utilization Certificates of Previous Grant for symposia (as per Col.No. 15 of the Application Performa) not submitted till date, please attach copies of Utilization Certificates also. Any claim received beyond 4 months will be entertained only in exceptional cases subject to submission of reasons for delay, duly forwarded through Head of the Organisation. In no case, the claim will be entertained after 6 months. All the pages of above documents should be self attested by the organizer.
3. Invitation cards should be sent to the Director General, CSIR and Head, HRDG. CSIR may nominate three scientists for the above event and registration fee should not be charged from them. In case of nomination, the Head, HRDG or the undersigned would issue a letter with a copy to the nominee(s).
4. Softcopy (preferably in CD/ DVD in PDF format) of the full paper proceedings of above event should be sent to the undersigned.
5. An overall activity report by the Convener / Organizing Secretary should be made available by email to us with regard to outcome of the gathering, the recommendations and plan of action for future. The names, addresses & email IDs of the participants / delegates should also be sent immediately after the event by email.

Yours sincerely,

(Hemant Kulkarni)



सॉफ्टवेयर टेक्नोलॉजी पार्क्स ऑफ इंडिया
(भारत सरकार के इलेक्ट्रॉनिक्स और सूचना प्रौद्योगिकी मंत्रालय के अन्तर्गत एक स्वायत्त सोसाइटी)
सं. 76 & 77, 6th Floor, Cyber Park, Electronics City, Hosur Road, Bengaluru - 560100
दूरभाष : +91-80-6618 6000-07, फ़ैक्स : +91-80-28521161, पृष्ठारण : www.blr.stpi.in
Software Technology Parks of India
(An Autonomous Society under the Ministry of Electronics & Information Technology, Govt. of India)
No.76 & 77, 6th Floor, Cyber Park, Electronics City, Hosur Road, Bengaluru-560100.
Tel : +91-80-6618 6000-07, Fax : +91-80-28521161, URL : www.blr.stpi.in

Ref No: STPI-B/Sponsorship/2019-20/15903

8th Aug. 2019

To,

Dr. Ravindra. R. Malagi,
Convenor, FatigueDurability India 2019
Professor, Product Design and Manufacturing,
Visvesvaraya Technological University,
Jnana Sangama, Machhe,
Belagavi, Karnataka 590018

Dear Sir,

Sub: STPI Sponsorship for the Fatigue Durability India 2019 event.

This is in reference to your letter dated 01.07.2019 with regard to sponsorship for 3rd International Conference on Fatigue, Durability and Fracture Mechanics & Symposium on Condition Assessment / Residual Life Assessment to be held on 29th to 31st August 2019 at Visvesvaraya Technological University, Belagavi. We are please to inform that, STPI is extending support for the event with the sponsorship amount of Rs. 50,000/- (exclusive of taxes) for Souvenir Page Advertisement.

You are requested to raise an Invoice for the said Sponsorship amount in the name of Director STPI-Bengaluru and forward the same for release of payment. Kindly quote your GST No. in the Invoice.

STPI-B GST No. is 29AAATS2468J3Z0 (0 - Zero)

Thanking You,

Yours faithfully,

V. Sridhar,
Senior Admin officer

मुख्यालय / Head Quarter : नई दिल्ली, New Delhi

उप केन्द्र / Sub Centers : मैसूरू, मणिपाल, मंगलूरू, हुब्लल्ली, Mysuru, Manipal, Mangaluru, Hubballi

अन्य केन्द्र / Other Centers : चेन्नै, गांधीनगर, गुवाहाटी, हैदराबाद, नोएडा, पुणे, तिरुवनंतपुरम, भुवनेश्वर, कोलकता
Chennai, Gandhinagar, Guwahati, Hyderabad, Noida, Pune, Thiruvananthapuram, Bhubaneshwar, Kolkata



Karnataka Science and Technology Promotion Society

Dept. of Information Technology, Bio Technology and Science & Technology, GoK
"Vijnana Bhavan", 3rd Floor, #24/2, 21st Main Road, Banashankari 2nd Stage, Bangalore-70
Ph/fax : 080-26711166, E-mail : ksteps.dst@gmail.com

Dr. H. Honne Gowda
Special Director (Technical),
Dept. of IT, BT and S&T/Managing director, KSTePS

No. KSTePS/VGST/GRD-677/KFIST(L1)/2018

Date: 27.08.2018

Dear Sir/Madam,

Sub: Intimation of selection of KFIST Level (1) project under the VGST Scheme – reg.

Greetings from KSTePS, Dept. of Information Technology, Biotechnology and Science and Technology!!

We are pleased to inform you that the project titled **"Infrastructure to carry out research work on development of expert system for the prediction of cutting forces in Turning"** submitted under the VGST scheme of KFIST Level (1) for the Financial Year 2017-18 has been approved by the Government based on the recommendations of Vision Group on Science and Technology under the Chairmanship of Prof. CNR Rao, Honorary President, JNCASR.

The total project grant award for a period of 2 years is Rs. 20.00 lakhs, which will be released annually @ Rs. 10.00 lakhs based on the progress of work. You are requested to take an immediate action to initiate the project at the earliest and to be completed within 2 years after receiving the cheque of 1st instalment from our office.

The grant will be paid to the Head of the Institution, under whose supervision the Principal Investigator shall be responsible for completion of the stated objectives of the project. The Principal Investigator through the Institution Head shall have to submit the progress report in soft copy (word & pdf) once in 6 months without any fail. The grants shall be used only for the purposes described in the grant application by following due procedures of KTPP Act. Any deviation from the scheduled plan must have a prior approval from the VGST.

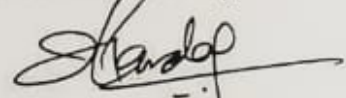
Please provide the cheque in favour address of your institution, for releasing the sanctioned grants.

Future releases of grants will be based on satisfactory project performance. The funding agency has the right to terminate the project, if it is found to be not satisfactorily pursuing and fulfilling the stated project goals and objectives. Any unspent balance must be returned back to the funding agency within 60 days following the conclusion of the project. Any publications or other dissemination arising from research supported by VGST grants should be acknowledged.

I want to personally thank you for being selected as one of the VGST program members and we wish you and the Principal Investigator a great success in the implementation of the project.

Thanking You

Yours sincerely,



(H. Honne Gowda)

To,
The Registrar
Visvesvaraya Technological University
Jnana Sangama, Belagavi - 590 018

CC:

1. Dr. R. R. Malagi, Dept. of Product Design and Manufacturing, Centre for PG Studies
Visvesvaraya Technological University, 'Jnana Sangama', Belagavi - 590 018- **Principal Investigator of KFIST (L1) under VGST scheme**
2. Consultant, Vision Group on Science & Technology, KSTePS, Dept. of IT, BT and S&T,
7th Floor, 4th block, MS Building, Bengaluru- 560 001



Visvesvaraya Technological University

"Jnana Sangama", Belagavi - 590 018, Karnataka State

Dr. H. N. Jagannatha Reddy, BE,ME,Ph.D.
Registrar

Phone : (0831) 2405468
Fax : (0831) 2405467

Ref. No: VTU/Aca./2016-17/A-9/ 1981

Date: 11 JUL 2016

To,
The Managing Director,
Karnataka Science and Technology Promotion Society (KSTePS),
Department of IT, BT and S & T,
Government of Karnataka,
Vignana Bhavan, No. 24/2, 3rd Floor,
21st Main Road, Banashankari II Stage,
BENGALURU - 560 070.

Sir,

Sub: VGST/K-Fist (Level -1) Programme grants for the FY: 2015-16 reg.,
Ref: KSTePS/VGST/05/K-Fist/2015-16 dated: 20-06-2016.

With reference to the above subject, this is to acknowledge that, we have received a sum of ₹10.00 Lakhs (Rupees Ten lakhs only) vide Cheque bearing No. 942500 dated: 20-06-2016 drawn in favour of The Finance Officer, VTU, Belagavi from Karnataka Science and Technology Promotion Society (KSTePS) under Vision Group on Science and Technology (VGST), Department of IT, BT and S & T, Government of Karnataka (GoK) towards the first installment for the year 2015-16 under the scheme VGST - K-FIST(Level 1) Programme entitled "VTU-Chip Design Laboratory (VTU-CDL)" submitted by the Programme Co-ordinator Dr. Meghana Kulkarni, Dept. of VLSI Design & Embedded Systems, Center for PG Studies, VTU, Belagavi.

Thanking you,

Yours faithfully,

REGISTRAR

Copy to:

1. The PG Co-ordinator, Center for PG Studies, VTU, Belagavi.
2. The Special Officer, DPAR Section, VTU, Belagavi.
3. Dr. Meghana Kulkarni, Dept. of VLSI Design & Embedded Systems, CPGS, VTU, Belagavi.

Dr. M&K
13/7/16

20/07/16

1A



Visvesvaraya Technological University, Belgaum-590018

RECEIPT

Receipt No. : **96712**

Date: **29-Jun-16**

Received From **KARNATAKA SCIENCE AND TECHNOLOGY PROMOTION**

Received by : DD / Cheque / Cash

Sl.No	DD /Cheque No.	Date	Bank	Amount
1	942500	20/6/2016	SBM	1000000
Sl.No	Particulars	Amount		
1	Govt. Grants	1000000		
	Total	1000000		

In word(Rupees): Rupees Ten Lacs Only

For Finance Officer



ಕರ್ನಾಟಕ ವಿಜ್ಞಾನ ಮತ್ತು ತಂತ್ರಜ್ಞಾನ ಪ್ರೋತ್ಸಾಹಕ ಸೊಸೈಟಿ

ವಿಜ್ಞಾನ ಮತ್ತು ತಂತ್ರಜ್ಞಾನ ಇಲಾಖೆ, ಕರ್ನಾಟಕ ಸರ್ಕಾರ

'ವಿಜ್ಞಾನ ಭವನ' ನಂ: 24/2, 3ನೇ ಮಹಡಿ, 21ನೇ ಮುಖ್ಯ ರಸ್ತೆ, ಬನಶಂಕರಿ 2ನೇ ಹಂತ, ಬೆಂಗಳೂರು - 560 070

ದೂರವಾಣಿ/ಫ್ಯಾಕ್ಸ್ : 080 - 26711166/ 26711160; ಇ-ಮೇಲ್ : ksteps.dst@gmail.com

ಡಾ. ಹೆಚ್. ಹೊನ್ನೇಗೌಡ

ವ್ಯವಸ್ಥಾಪಕ ನಿರ್ದೇಶಕರು, ಕೆಸ್ಪಿಪ್

ನಂ. ಕೆಸ್ಪಿಪ್/ವಿತಂದಾಸ/05/K-Fist/2015-16

ದಿನಾಂಕ: 20-06-2016

ಮಾನ್ಯರೇ

ವಿಷಯ: 2015-16ನೇ ಸಾಲಿನ ವಿಜ್ಞಾನ ಮತ್ತು ತಂತ್ರಜ್ಞಾನ ದಾರ್ಶನಿಕ ಸಮೂಹದ K-Fist (Level-1) ಯೋಜನೆಯಡಿಯಲ್ಲಿ ಅನುದಾನ ಬಿಡುಗಡೆ ಮಾಡುವ ಬಗ್ಗೆ.

ಉಲ್ಲೇಖ: ವಿಯಇ 87 ವಿತ್ರಮ 2016, ದಿ. 21.05.2016

ವಿಜ್ಞಾನ ಮತ್ತು ತಂತ್ರಜ್ಞಾನ ಇಲಾಖೆಯು, ಖ್ಯಾತ ವಿಜ್ಞಾನಿ ಭಾರತರತ್ನ ಪ್ರೊಫೆಸರ್ ಸಿ.ಎನ್.ಆರ್. ರಾವ್, F.R.S. ರವರ ಅಧ್ಯಕ್ಷತೆಯಲ್ಲಿ ವಿಜ್ಞಾನ ಮತ್ತು ತಂತ್ರಜ್ಞಾನ ದಾರ್ಶನಿಕ ಸಮೂಹವನ್ನು 2008ರಲ್ಲಿ ಸ್ಥಾಪಿಸಿದ್ದು, ಈ ಯೋಜನೆಯಡಿ ಹಲವಾರು ವೈಜ್ಞಾನಿಕ ಕಾರ್ಯಕ್ರಮಗಳನ್ನು ಕಳೆದ 8 ವರ್ಷಗಳಿಂದ ರಾಜ್ಯಾದ್ಯಂತ ಯಶಸ್ವಿಯಾಗಿ ಅನುಷ್ಠಾನಗೊಳಿಸಿಕೊಂಡು ಬರುತ್ತಿರುವುದು ಸರಿಯಷ್ಟೆ. 2015-16ನೇ ಸಾಲಿನಲ್ಲಿ ತಮ್ಮ ಸಂಸ್ಥೆಯಿಂದ ಸಲ್ಲಿಸಿದ ಪ್ರಸ್ತಾವನೆಯಾದ "VTU-Chip Design Laboratory (VTU-CDL)" ನ್ನು ವಿ.ಜಿ.ಎಸ್.ಐ. ಯ ಪ್ರಮುಖ ಕಾರ್ಯಕ್ರಮವಾದ Karnataka Fund For Infrastructure Strengthening In Science And Technology (K-FIST) ನ ಯೋಜನೆಯಡಿಯಲ್ಲಿ ದಾರ್ಶನಿಕ ಸಮೂಹವು ಆಯ್ಕೆ ಮಾಡಿ, ಸರ್ಕಾರ ಆದೇಶ ನೀಡಿರುವುದು ತಮಗೆ ತಿಳಿದ ವಿಷಯವಾಗಿದೆ.

ವಿಜ್ಞಾನ ಮತ್ತು ತಂತ್ರಜ್ಞಾನ ಇಲಾಖೆಯ ಅಂಗ ಸಂಸ್ಥೆಯಾದ ಕರ್ನಾಟಕ ವಿಜ್ಞಾನ ಮತ್ತು ತಂತ್ರಜ್ಞಾನ ಪ್ರೋತ್ಸಾಹಕ ಸೊಸೈಟಿ (ಕೆಸ್ಪಿಪ್)ಯನ್ನು ಪ್ರಸ್ತುತ ವರ್ಷದಿಂದ ದಾರ್ಶನಿಕ ಸಮೂಹದ ಕಾರ್ಯಕ್ರಮಗಳ ಉಸ್ತುವಾರಿ ಸಂಸ್ಥೆಯಾಗಿ ನೇಮಿಸಲಾಗಿದೆ. ಆದುದರಿಂದ, ತಮ್ಮ ಸಂಸ್ಥೆಯಿಂದ ಆಯ್ಕೆಗೊಂಡ ಪ್ರಸ್ತಾವನೆಗೆ ಮೊದಲ ಕಂತಾಗಿ ರೂ. 10.00 ಲಕ್ಷಗಳ ಅನುದಾನವನ್ನು **Finance Officer, VTU, Belagavi** ಹೆಸರಿನಲ್ಲಿ ಚೆಕ್‌ನ್ನು (ಚೆಕ್ ಸಂಖ್ಯೆ: 942500, ದಿ:20.06.2016) ನೀಡಲಾಗುತ್ತಿದೆ. ಚೆಕ್ ಸ್ವೀಕರಿಸಿದ ನಂತರ, ಸ್ವೀಕೃತ ರಶೀದಿ (Acknowledgement) ಯನ್ನು ಕೆಸ್ಪಿಪ್‌ಗೆ ಕಳುಹಿಸುವುದು.

ಸದರಿ ಅನುದಾನವನ್ನು ಉದ್ದೇಶಿತ ಯೋಜನೆಗೆ ಮಾತ್ರ ಬಳಸಿಕೊಳ್ಳುವುದು ಹಾಗೂ ಎಲ್ಲಾ ವೆಚ್ಚಗಳನ್ನು ಕರ್ನಾಟಕ ಸಾರ್ವಜನಿಕ ಸಂಗ್ರಹಣೆಯಲ್ಲಿ ಪಾರದರ್ಶಕತೆ ಅಧಿನಿಯಮ, 1999 (Karnataka Transparency in Public Procurements Act, 1999 - <http://finance.kar.nic.in/index.htm>) ಅನುಸಾರ ಹಾಗೂ ದಾರ್ಶನಿಕ ಸಮೂಹ ಅನುಮೋದಿಸಿರುವ ವಿವಿಧ ಶೀರ್ಷಿಕೆಗಳಿಗೆ ಅನುಗುಣವಾಗಿ

ಯೋಜನೆಯನ್ನು ಅನುಷ್ಠಾನಗೊಳಿಸುವುದು. ಬಿಡುಗಡೆಯಾದ ಅನುದಾನವನ್ನು ಬಳಸಿಕೊಂಡ ನಂತರ ಎಲ್ಲಾ ವೆಚ್ಚಗಳನ್ನು ನೋಂದಾಯಿತ ಆಡಿಟರ್ ಮೂಲಕ ಆಡಿಟ್ ಮಾಡಿಸಿ, ಉಪಯೋಗತಾ ಪ್ರಮಾಣ ಪತ್ರವನ್ನು ದ್ವಿಪ್ರತಿಯಲ್ಲಿ ಈ ಪತ್ರದೊಂದಿಗೆ ಲಗತ್ತಿಸಿರುವ ಸ್ವರೂಪದಲ್ಲಿ (Format) ಕೆಸ್ಫೆಸ್ ಸಂಸ್ಥೆಯ ಮೇಲ್ಕಂಡ ವಿಳಾಸಕ್ಕೆ ಕಳುಹಿಸಿಕೊಡುವುದು. ಈ ಯೋಜನೆಗೆ ಸಂಬಂಧ ಪಟ್ಟ ಎಲ್ಲಾ ಲೆಕ್ಕ ಪತ್ರಗಳನ್ನು ಸಂರಕ್ಷಿಸಿಡುವುದು ಹಾಗೂ ಮಹಾಲೇಖಪಾಲಕರು ಮತ್ತು ಸರ್ಕಾರವು ಸಮೀಕ್ಷೆಗಾಗಿ ಕೋರಿದಲ್ಲಿ ತಪ್ಪದೇ ಒದಗಿಸುವುದು. ಈ ಯೋಜನೆಗೆ ಅನುಗುಣವಾಗಿ ಪ್ರತ್ಯೇಕ ದಾಖಲೆ ಪುಸ್ತಕ ಸಹ ನಿರ್ವಹಿಸಬೇಕೆಂದು ಕೋರುತ್ತೇನೆ.

ಹೆಚ್ಚಿನ ಮಾಹಿತಿಗಾಗಿ ಶ್ರೀಮತಿ ಶ್ರೀರಂಜನಿ. ಕೆ. ವೈಜ್ಞಾನಿಕ ಕ್ಷೇತ್ರಾಧಿಕಾರಿ, ಕರ್ನಾಟಕ ವಿಜ್ಞಾನ ಮತ್ತು ತಂತ್ರಜ್ಞಾನ ಪ್ರೋತ್ಸಾಹಕ ಸೊಸೈಟಿ (ಕೆಸ್ಫೆಸ್) (ದೂರವಾಣಿ: 080-26711166; ಇ-ಮೇಲ್: srivgst.ksteps@gmail.com) ಇವರನ್ನು ಸಂಪರ್ಕಿಸಬಹುದು.

ವಂದನೆಗಳೊಂದಿಗೆ,

ತಮ್ಮ ವಿಶ್ವಾಸಿ



(ವ್ಯವಸ್ಥಾಪಕ ನಿರ್ದೇಶಕರು)

ಇವರಿಗೆ,

**The Finance Officer,
Center for PG Studies, VTU,
Jnana Sangama, Machhe,
Belgaum – 590 018**

✓ **ಪ್ರತಿ: Dr. Meghana Kulkarni, Programme Co-ordinator, Dept. of VLSI Design and Embedded Systems, Center for PG Studies, VTU, Jnana Sangama, Machhe, Belgaum – 590 018**



Visvesvaraya Technological University

CPG, Belagavi

Workshop Proposal

On

ARM Cortex-M4 Microcontroller

Workshop on ARM Cortex-M4 Microcontroller

8/16-bit processors run on old architectures; which make it tend towards slowness. It also has a low limit on supported RAM/other storage. Whereas 32-bit microcontroller architectures can replace 8/16-bit systems without a cost increase for embedded solution with a boost in RAM size and performance. The ARM Cortex™-M0 processor is the smallest ARM processor available; which will be the main stream product for next 1~2 decade with exceptionally small silicon area and low power required to achieve 32-bit performance at an 8/16-bit price point for similar application. On the one hand compared to 8/16-bit microcontrollers 32-bit ARM Cortex™-M0 microcontroller has up to 50 percent higher code density to perform typical task. NuMicro™ is Nuvoton's brand-new 32-bit Microcontroller (MCU) family powered by the ARM® Cortex™-M0 processor - the smallest, lowest power and most energy-efficient ARM processor optimized for a variety of MCU applications. Nuvoton's NuMicro™ family includes NUC100/200 series, NUC120/122/ 123/220 series with USB 2.0 FS device, NUC130/140 series embedded with Controller Area Network (CAN) 2.0B licensed from BOSCH, M051 series, Mini51 series, and Nano100 Ultra-low Power series targeting at battery powered applications. With a variety of product offerings, the NuMicro™ family is ideal for use in industrial control systems, industrial automation, consumer products, embedded network control, energy, power systems, motor control, and many more. Furthermore, with the integration of the industry leading ARM® Cortex™-M0 microprocessor, the NuMicro™ family brings 32-bit performance at a cost equivalent to traditional 8-bit MCU.

The objective of this workshop is to introduce the participants to the world of ARM Microcontrollers and give an insight on how and where they can be used. This workshop will be useful to learn the fundamentals of ARM Cortex-M4 Microcontroller in detail which inturn help the students to do their projects in the Embedded system domain using ARM Cortex-M4 Microcontrollers as a part of the project.

Hands on exercises with Keilµvision IDE software will open a door for programming in embedded C for other ARM series microcontrollers also.

Workshop Highlights:

- Introduction to Embedded systems & Microcontrollers.
- Introduction to ARM Cortex-M4 Microcontroller architecture.
- ARM Cortex-M4 instruction set.
- Keil μ vision IDE software environment.
- Hands on working on Nuvoton's NUC 100 series ARM Cortex-M4 Microcontrollers.
- Interaction with Visvesvaraya Technological University VLSI Design and Embedded system faculty members

About Nuvoton Technology Corporation:

Nuvoton's main product lines are Microcontroller Application IC, Audio Application IC, Cloud & Computing IC, and foundry service. Its consumer electronics ICs focus mainly on microcontroller ICs and voice and speech ICs. Its ARM Cortex-M4 microcontroller IC NuMicro Family is well known for its density and functionality. Its computer IC product line designs and manufactures the key chips for PC motherboards, notebook computers and servers, offering complete Super I/O solutions, clock generators, hardware monitoring IC, power management IC, TPM security IC, notebook keyboard controller, and mobile platform embedded controller (EC).

Nuvoton operates a six-inch wafer fab which provides foundry service for the company's own branded IC products, as well as for selected manufacturing partners.

Who should attend?

The workshop is aimed at the multi-faceted audience from Academics, Research Scholars and Post Graduate Students from Engineering Colleges and universities. Participants limited to only 40 and selection will be on first come first served basis.

Outcome of the Workshop:

The content of the workshop is tailored to introduce the new technology and provide hands-on training in programming the microcontroller with appropriate tools and interfacing with other peripherals which helps the participants in developing embedded applications.

Resource Persons:

DR. Meghana Kulkarni

Tentative Schedule

Session 1: (Day 1 Forenoon)

Introduction to Embedded systems

What is an Embedded System?

Essential characteristics of embedded system

Hard Real Time System & soft Real Time System

μ P Vs μ C and different Architectures

Classification and selection of microcontrollers for embedded applications

8-bit Vs 16-bit Vs 32-bit Vs 64-bit

CISC Vs RISC

Session 2: (Day 1 Afternoon)

Lab Session 1

Installing latest version of Keil μ vision IDE tool

Project creation for different targets in Keil μ vision IDE tool

Understanding the features available in μ vision IDE tool

Session 3: (Day 2 Forenoon)

Introduction to ARM Cortex Microcontroller series

Why to use ARM microcontroller

ARM processor family

Byte, Word and Half-word

ARM Cortex architecture

ARM ARCHITECTURE

Session 4: (Day 2 Afternoon)

REGISTER AND MEMORY OF ARM CORTEX M4

ARM Register Set

32 bit CPU registers

ARM Pipeline

Cortex M series

Session 5: (Day 3 Forenoon)

Overview of ARM Instruction set

32-bit instruction set

16-bit instruction set

8-bit instruction set

Session 6: (Day 3 Afternoon)

Introduction to Embedded C programming and Lab session 2

Introduction to Pre-processor Directives

Difference between C and Embedded C

Compiler handling

Basic Embedded programs structure

Getting your programs into a compiler, writing your programs

Hands on practice of writing few simple embedded C programming for ARM

Session 7: (Day 4 Forenoon)

Lab session 3

Basic data storage and data movement programs in Embedded C

Delay Programs in Embedded C

Counters and Timers Programs

Session 8: (Day 4 Afternoon)

Understanding the GPIO Architecture of ARM & Lab session 4

Introduction to real world interface

GPIO's Architecture

Understanding Interface modules and components

LED Program to understand interface

Session 9: (Day 5 Forenoon)

Lab session 5

Drivers installation for real time interface

Interfacing LED with Controller

Interfacing switch (push button) with controller

Interfacing ADC with controllers

Session 10: (Day 5 Afternoon)

Lab session 6 & Valedictory

Practical exam based on the previously developed programs

Technical Quiz on ARM Cortex Architecture

Interaction with VTU's VLSI Design and embedded systems department faculty

Certificate Distribution

Requirements:

Participants are supposed to bring their laptops in order to install design software.

A well-equipped seminar hall with mic, projector, writing board and seating arrangement for participants

Deliverables to participants:

Soft copy of important information

Keil μ vision IDE tool

Participation certificate

Merit certificate for the participants to winning team of Lab session 6

TECHNOLOGY RELATED INNOVATIVE PROJECTS
(TRIP - 2015-16)

TRIP - PROPOSAL FORMAT

A. PROJECT DETAILS :					
1	<u>TRIP Title :-</u>	Smart Food Serving System			
2	Broad Project Area	All Branches of Engineering, Science & including Medical, Agriculture & Pharmacy			
B. STUDENT DETAILS (TRIP Applicant) :					
3	Name of the Students (Maximum of 2 Students are allowed)	Sl. No.	Name	Semester	Contact No.
		1	Santosh Sanjeev Kulkarni	3rd	9481322678
		2	Manjunath Savadatti	3rd	8904536620
4	Course: Undergraduate / Post Graduate Mark (✓) at appropriate place]	UG			
		PG	✓		
C. PROJECT SUPERVISOR DETAILS :					
5	Name of the Project Supervisor	Prof. Dr. Meghana Kulkarni			
6	Designation of the Project Supervisor	Associate Professor			
7	Department	VLSI Design and Embedded Systems			
8	College Name	Department of PG Studies, Visvesvaraya Technological University, Belagavi			
9	Address	Department of VLSI Design and Embedded Systems, Department of PG Studies, 'Jnana Sangama', Visvesvaraya Technological University, Santibastwad, Macche, Belagavi-590014			
	Telephone	0831-2498251			
	Mobile	+91-9480398197			
	Fax				
	E-mail	meghanak@vtu.ac.in			

Centre for PG Studies,
VISVESVARAYA TECHNOLOGICAL UNIVERSITY,
“Jnana Sangama”, Machhe, Belagavi- 590018.
Ph No: 0831-2498251 / 195. FAX: 0831 - 2498253.



A Proposal for

**Karnataka Fund for Infrastructure Strengthening in
Science & Technology (K-FIST Level-1)**

Entitled

VTU-Chip Design Laboratory (VTU-CDL)

Submitted to



Government of Karnataka
Vision Group on Science and Technology
Department of Information Technology, Biotechnology & Science and Technology

By

Dr. Meghana Kulkarni
Associate Professor
Center for PG Studies, VLSI Design and Embedded Systems
Visvesvaraya Technological University, .
Belagavi

TECHNOLOGY RELATED INNOVATIVE PROJECTS
(TRIP - 2015-16)

TRIP - PROPOSAL FORMAT

A. PROJECT DETAILS :

1	TRIP Title :-	ANTI RAILWAY TRACK TRESPASSING & EARLY ALARM SYSTEM
2	Broad Project Area	All Branches of Engineering, Science & including Medical, Agriculture & Pharmacy

B. STUDENT DETAILS (TRIP Applicant) :

3	Name of the Students (Maximum of 2 Students are allowed)	Sl. No.	Name	Semester	Contact No.
		1	Avinash Kadam	3 rd	+91-8105007749
		2	Raghumanohar A	3 rd	+91-7676995890
4	Course: Undergraduate / Post Graduate Mark (✓) at appropriate place]	UG			
		PG			

C. PROJECT SUPERVISOR DETAILS :

5	Name of the Project Supervisor	Dr.Meghana Kulkarni
6	Designation of the Project Supervisor	Associate Professor
7	Department	Department of VLSI Design & Embedded Systems
8	College Name	Centre for P.G. Studies, VTU Belagavi
9	Address	Centre for P.G. Studies, Visvesvaraya Technological University, "Jnana Sangama", Belagavi, Karnataka - 590018
	Telephone	+91-831-2498251
	Mobile	+91-9480398197
	Fax	
	E-mail	

FILE NO. YSS/2015/001930
SCIENCE & ENGINEERING RESEARCH BOARD(SERB)
(a statutory body of the Department of Science & Technology, government of India)

5 & 5A, Lower Ground Floor
Vasant Square Mall
Plot No. A, Community Centre
Sector-B, Pocket-5, Vasant Kunj
New Delhi-110070

Dated: 02-Jul-2018

ORDER

Subject: Research project entitled "DEVELOPMENT NOVEL QUINAZOLINES AS ANTI-TUMOR AND ANTI-ANGIOGENIC AGENTS" under the guidance of Dr. Prasanna D Shivaramu, Nanotechnology, Visvesvaraya Technological University, Bengaluru region, Department Of Nanotechnology Visvesvaraya Institute Of Advanced Technology Visvesvaraya Technological University, Bengaluru Region Muddenahalli, Chikkaballapur - 562 101 India., Chikkaballapur District, Karnataka-562101.

1. This is in continuation of SERB's sanction order No. "YSS/2015/001930" dated "09 February, 2016" of Science and Engineering Research Board (SERB).

2. Sanction of the competent authority is hereby accorded to the payment of a sum of Rs. 500000/- (Rupees Five Lakh only) under 'Grants-in-aid General' to REGISTRAR, Visvesvaraya Technological University, Bengaluru Region, Department Of Nanotechnology Visvesvaraya Institute Of Advanced Technology Visvesvaraya Technological University, Bengaluru Region Muddenahalli, Chikkaballapur - 562 101 India. being the 3rd grant for the financial year 2018-2019 for implementation of the above said project.

3. Sanction of the competent authority is also accorded to the carry forward of unspent balance of Rs. 209873/- (Rupees Two Lakh Nine Thousand Eight Hundred and Seventy Three only) (Recurring Rs. 107573 and Non-Recurring Rs. 102300) to Visvesvaraya Technological University, Bengaluru region, Department of Nanotechnology Visvesvaraya Institute of Advanced Technology Visvesvaraya Technological University, Bengaluru region Muddenahalli, Chikkaballapur - 562 101 India. from FY 2017-2018 to FY 2018-2019 for the same purpose for which it was sanctioned

4. Sanction of the grant is subject to the conditions as detailed in Terms & Conditions available at the website (www.serb.gov.in).

5. It is certified that provision of GFR 212 relating to Utilization Certificates (Ucs) for the funds released under the grant have been satisfied and the UC/s is/are enclosed herewith.

6. The expenditure involved is debitable to Fund for Science & Engineering Research (FSER) This release is being made under Start Up Research Grant (Young Scientist). (EC Chemical Sciences) (GEN)

7. The Sanction has been issued to Visvesvaraya Technological University, Bengaluru Region, Department Of Nanotechnology Visvesvaraya Institute Of Advanced Technology Visvesvaraya Technological University, Bengaluru Region Muddenahalli, Chikkaballapur - 562 101 India. with the approval of the competent authority under delegated powers on 18 June, 2018 and vide Diary No. SERB/F/2918/2018-2019 dated 28 June, 2018

8. The release amount of Rs. 500000/- (Rupees Five Lakh only) will be drawn by the Under Secretary of the SERB and will be disbursed by means of RTGS transaction as per their Bank details given below:

Account Name	FINANCE OFFICER, VTU, BELGAUM
Account Number	64202589534
Bank Name & Branch	STATE BANK OF INDIA STATE BANK OF INDIA, VTU CAMPUS BRANCH, BELAGAVI - 590018
IFSC/RTGS Code	SBIN0040649
Email id of A/C Holder	registrar@vtu.ac.in
Email id of PI	prasuds@gmail.com

9. The institute will maintain separate audited accounts for the project. A part or whole of the grant must be kept in an interest earning bank account which is to be reported to SERB. The interest thus