CBCS SCHEME

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18CB34

Third Semester B.Tech. Degree Examination, Feb./Mar. 2022
Computer Organization

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Explain with a neat diagram the connection between the processor and the computer memory. **(08 Marks)**

b. Define performance measurement. Explain overall SPEC rating for computer. **(06 Marks)**

c. Explain Big and Little endian. Explain the memory operations. **(06 Marks)**

OR

2 a. If Register R1 and R2 of a computer contains the decimal values 1200 and 4600. What is the effective-address of the memory operand in each of the following instructions? Identify and explain the addressing modes of given instructions.
(i) Load 20(R1), R5
(ii) Move #3000, R5
(iii) Store R5, 30(R1, R2)
(iv) Add –(R2), R5 **(08 Marks)**

b. What is subroutine? Analyze the use of call or return instruction in a subroutine with assembly language program code. **(06 Marks)**

c. Write an assembly language program for the expression S = (H + A) ∗ (R + E), using three, two and one address instructions. **(06 Marks)**

Module-2

3 a. What is bus arbitration? With neat diagrams, describe centralized and distributed arbitration process. **(08 Marks)**

b. Explain the I/O Interface with modules diagram with I/O memory mapped. **(06 Marks)**

c. Explain how simultaneous interrupt requests from several I/O devices can be handled by processor through a single INTR line. **(06 Marks)**

OR

4 a. Describe the general 8-bit parallel interface in brief. **(08 Marks)**

b. Explain the data transfer operations in PCI. **(06 Marks)**

c. Explain the Bus signal operation of SCSI Bus from hardware point of view. **(06 Marks)**

Module-3

5 a. Describe the static RAM cell with an example of CMOS memory cell in brief. **(08 Marks)**

b. Explain EPROM and flash memory. **(06 Marks)**

c. Define the terms:
(i) Memory Access Time and Memory Cycle Time
(ii) Memory Latency and Memory Bandwidth
(iii) Double Data Rate SDRAM. **(06 Marks)**

OR

6 a. Describe asynchronous dynamic ram with the internal organization of 2M * 8 dynamic memory chip. **(08 Marks)**

b. Explain the terms of the following:
(i) LRU Replacement algorithm
(ii) Interleaving **(06 Marks)**

c. Define Cache Memory. Mention the effectiveness of cache mechanism with use of a cache memory. **(06 Marks)**

Module-4

7 a. Describe 4 bit carry lookahead adder in detail with logic operations. **(08 Marks)**

b. Explain binary addition/subtraction logic circuit and mention the purpose of fast adder design. **(06 Marks)**

c. Explain n-bit Ripple carry adder. **(06 Marks)**

OR

8 a. Explain sequential circuit binary multiplier of 13 × 11 with register configuration. **(08 Marks)**

b. Describe the importance of carry-save addition with multiplication example. **(06 Marks)**

c. Explain the procedure of restoring division. **(06 Marks)**

Module-5

9 a. Explain with the flowchart for determining a minimum sum of products using a Karnaugh map. **(08 Marks)**

b. Plot Karnaugh maps for product terms f(a, b, c) = abc′ + b′c + a′ **(06 Marks)**

c. Mention other uses of Kernaugh maps. **(06 Marks)**

OR

10 a. Explain J-K flip flop with master-slave arrangement. **(08 Marks)**

b. Describe the purpose of T flip-flop. **(06 Marks)**

c. Explain derivation of Q^+ for an S-R latch and also switch debouncing with an S-R latch. **(06 Marks)**

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