CBCS SCHEME

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18CS733

Seventh Semester B.E. Degree Examination, July/August 2022
Advanced Computer Architectures

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Explain the elements of modern computer system with neat diagram. **(10 Marks)**

b. Describe with a neat diagram, different shared memory multiprocessor models. **(10 Marks)**

OR

2 a. Define the types of data dependence. Also compute the dependence graph for the following code segment

S_1 : Load R_1, A
S_2 : ADD R_2, R_1
S_3 : MOVE R_1, R_3
S_4 : Store B, R_1 **(10 Marks)**

b. Explain the characteristics of the following static connection networks with diagram:

(i) Linear array
(ii) Chordal ring of degree 4
(iii) Binary tree
(iv) Mesh
(v) Torus **(10 Marks)**

Module-2

3 a. Distinguish between RISC and CISC processor architectures with block diagram. **(10 Marks)**

b. Explain VLIW processor architecture and its pipeline operations. **(10 Marks)**

OR

4 a. Explain in detail inclusion, coherence and locality properties. **(10 Marks)**

b. Illustrate the four level memory hierarchy. **(04 Marks)**

c. Define the various page replacement policies. **(06 Marks)**

Module-3

5 a. What is arbitration? Describe central arbitration and distributed arbitration with relevant sketches. **(10 Marks)**

b. Discuss physical address models and virtual address models for unified and split caches. **(10 Marks)**

OR

6 a. Explain two-models of linear pipeline units and the corresponding reservation table. **(05 Marks)**

b. Explain the features of non-linear pipeline processor with feed forward and feed backward connections. **(05 Marks)**

c. Consider the following pipeline reservation table:

Time →

Stages		1	2	3	4	5	6	7	8
	S_1	X					X		X
	S_2		X		X				
	S_3			X		X		X	

(i) What are the forbidden latencies?
(ii) What is the initial collision vector?
(iii) Draw the state transition diagram.
(iv) List all the simple cycles.
(v) List all the greedy cycles. **(10 Marks)**

Module-4

7 a. With a neat diagram, explain the bus systems at board level, backplane and I/O level. **(10 Marks)**

b. Define the two apporoaches of snoopy bus cache coherence protocol. Also write the state transition graphs for write through and write back cache. **(10 Marks)**

OR

8 a. Explain the flow control methods for resolving a collision between two packets requesting the same outgoing channel. **(10 Marks)**

b. Explain vector-access memory schemes with neat diagrams. **(10 Marks)**

Module-5

9 a. Describe language features for parallelism. **(10 Marks)**

b. Describe the compilation phases in parallel code generation. **(10 Marks)**

OR

10 a. Describe in brief the structure of the reorder buffer and how the use of reorder buffer addresses the various types of dependencies in the program. **(10 Marks)**

b. With the help of a block diagram, explain the role of reservation stations used in Tomasulo's algorithm. **(10 Marks)**

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