CBCS SCHEME

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18EC753

Seventh Semester B.E. Degree Examination, July/August 2022
ARM Embedded System

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Sketch a neat ARM core data flow model. **(08 Marks)**

b. List the applications of ARM processor. **(04 Marks)**

c. Explain pipeline mechanism for RISC processor to execute instructions. **(08 Marks)**

OR

2 a. With the help of bit layout diagram, explain current program status register of ARM. **(08 Marks)**

b. Define peripheral devices. Explain memory controllers and interrupt controllers. **(07 Marks)**

c. Define banked register and explain the same. **(05 Marks)**

Module-2

3 a. Explain conditional execution with an example. **(05 Marks)**

b. Discuss the load – store instruction with respect to the single register transfer. **(07 Marks)**

c. Predict the operation performed by the execution of each compare instruction and logical instruction. **(08 Marks)**

OR

4 a. Explain the ARM SWAP instruction with an example code. **(05 Marks)**

b. Explain Barrel shifter with a neat sketch. **(07 Marks)**

c. Test whether the following instruction are pre or post indexed addressing mode and update "r1+"

(i) LDR r_0, [r_1,#0 X4]!

(ii) STRH r_0, [r_1], r_2

(iii) STRH r_0, [r_1, R_2]

(iv) LDR r_0, [r_1], r_2, LSR # 0 X4 **(08 Marks)**

Module-3

5 a. Explain Thumb stack instruction with syntax and example. **(07 Marks)**

b. Explain ARM-Thumb interworking using BX and BLX instruction. **(08 Marks)**

c. Compare ARM and Thumb instructions. **(05 Marks)**

OR

6 a. Explain Thumb software Interrupt instruction with an example. **(06 Marks)**

b. Explain register usage in Thumb. **(06 Marks)**

c. Write description for the given Thumb mnemonics.
MVN, TST, STR, LDR, BL, ASR, ADC, POP **(08 Marks)**

Module-4

7	a.	Write code for enabling and disabling IRQ and FIQ interrupts.	**(08 Marks)**
	b.	Explain ARM processor exceptions and modes along with block diagram.	**(08 Marks)**
	c.	List function of the instructions used in the vector tables. Explain.	**(04 Marks)**

OR

8	a.	Explain Non-nested interrupt handler with a neat sketch.	**(10 Marks)**
	b.	Demonstrate the methods used by software handlers to minimize interrupt latency.	**(06 Marks)**
	c.	List the various issues that one may encounter when porting "C" code to the ARM.	**(04 Marks)**

Module-5

9	a.	Explain different firmware implementation or firmware execution flow.	**(10 Marks)**
	b.	Show where a cache and write buffer fit in the memory hierarchy.	**(10 Marks)**

OR

10	a.	With the help of neat block diagram, differentiate between logical and physical caches.	**(10 Marks)**
	b.	Illustrate the relationship that cache has between processor core and main memory.	**(10 Marks)**

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