CBCS SCHEME

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18EC734

Seventh Semester B.E. Degree Examination, July/August 2022
DSP Algorithms and Architecture

Time: 3 hrs. Max. Marks: 100

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. With the help of neat block diagram and typical signals, explain DSP System. **(10 Marks)**

b. Obtain the transfer function of the IIR filter whose difference equation is given by $y(n) = 0.1\,x(n) + 0.9\,y(n-1)$. **(04 Marks)**

c. The signal sequence $x(n) = \{0, 3, 6, 9, 12\}$ is interpolated by the interpolation factor of 3 using filter coefficients $b_k = [\frac{1}{3}, \frac{2}{3}, \frac{3}{3}, \frac{2}{3}, \frac{1}{3}]$. Find the interpolated sequence y(m). **(06 Marks)**

OR

2 a. Define Dynamic range and Resolution. **(04 Marks)**

b. Interpret the DAC error due to zero order hold at its output. **(07 Marks)**

c. Calculate the dynamic range and percentage resolution of each of the following number representation formats :
   i) 24 – bit , single precision , fixed point format.
   ii) 48 – bit, double precision , fixed point format.
   iii) A floating point format with a 16 – bit mantissa and an 8 – bit exponent. **(09 Marks)**

Module-2

3 a. Build the structure of 4 × 4 Brawn Multiplier. **(08 Marks)**

b. Consider a MAC unit whose inputs are 16-bit numbers. If 256 products are to be summed up in this MAC, how many guard bits should be provided for the accumulator to prevent overflow condition from occurring? Explain with neat diagram. **(06 Marks)**

c. A DSP has a circular buffer with the start and the end addresses as 0200H and 020FH respectively. What would be the new values of the address pointer of the buffer if , in the case of address computation, it gets updated to i) 0212 H ii) 01 F C H. Show the different cases with structures. **(06 Marks)**

OR

4 a. Build the block diagram of an address generation unit and explain in brief. **(08 Marks)**

b. Develop the conceptual diagram of a program sequences. **(06 Marks)**

c. Explain the importance of parallelism and pipelining used in programmable DSP with the help of 8 – tap FIR fitter. **(06 Marks)**

Module-3

5 a. Distinguish the architectural features of three fixed point DSPs. **(10 Marks)**

b. Sketch and explain functional diagram of the barrel shifter of the TMS 320C 54XX processor. **(10 Marks)**

OR

6 a. Describe the operation of hardware timer with a neat diagram. **(10 Marks)**

b. Write an ALP of TMS 320 C54XX processor to compute the sum of three product terms given by an equation. $y(n) = h_0\, x(n) + h_1\, x(n-1) + h_2\, x(n-2)$. Using MAC instruction. **(10 Marks)**

Module-4

7 a. Implement the block diagram of FIR filter and briefly explain. **(06 Marks)**

b. Sketch the block diagram for second order I I R filter and briefly explain. **(06 Marks)**

c. Write a program to multiply two Q_{15} numbers. **(08 Marks)**

OR

8 a. Determine the following for a 128 point FFT computation :

i) Number of stages ii) Number of butterflies in each stage

iii) Number of butterflies needed for the entire computation.

iv) Number of butterflies that need no twiddle factors.

v) Number of butterflies that require real twiddle factors.

vi) Number of butterflies that require complex twiddle factors. **(12 Marks)**

b. Write the subroutine for bit reversed order. **(04 Marks)**

c. Develop the subroutine to implement butterfly computation. **(04 Marks)**

Module-5

9 a. Describe DMA with respect to TMS 320 C54XX processor. **(10 Marks)**

b. Interface data memory system with the address range 000800H – 000FFF H for TMS320C5416 DSP processor. Use 2K X8 SRAM memory chips. **(10 Marks)**

OR

10 a. With neat block diagram, explain the synchronous serial interface between TMS320C54XX and CODEC device. **(10 Marks)**

b. Explain the DSP based biotelemetry receiver system with a neat block diagram. **(10 Marks)**

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