CBCS SCHEME

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18EC754

Seventh Semester B.E. Degree Examination, July/August 2022
Digital System Design using VHDL

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Explain the four ways of simplifying a logic expression using the laws and theorems of Boolean Algebra. **(10 Marks)**

b. Derive a Mealy state graph and state table for BCD to Excess-3 code converter. **(10 Marks)**

OR

2 a. Explain the 4 different coding schemes used for serial data transmission in Moore sequential network. Represent the following bit sequence transmission in all the code schemes: 01110010. **(10 Marks)**

b. Using state equivalence theorem and state reduction technique solve for the final reduced table of the given state table. **(10 Marks)**

Present state	Next state		Present output	
	X = 0	X = 1	X = 0	X = 1
a	c	f	0	0
b	d	e	0	0
c	h	g	0	0
d	b	g	0	0
e	e	b	0	1
f	f	a	0	1
g	c	g	0	1
h	c	f	0	0

Module-2

3 a. Using VHDL process, write the VHDL program to model a JK flipflop that has active low direct set (SN) and direct reset (RN) inputs to change the state in the falling edge of the clock. **(10 Marks)**

b. List and explain the predefined VHDL operators. **(10 Marks)**

OR

4 a. Write the VHDL program using single VHDL process with wait statement to model the behavior of BCD to Excess-3 mealy sequential network. **(10 Marks)**

b. With the syntax, explain the entity-architecture pairs used to write the VHDL program. Write the VHDL program for full adder. **(10 Marks)**

Module-3

5 a. List and explain the scalar type VHDL data types. **(10 Marks)**

b. List and explain the different styles of descriptions used to write a VHDL program. **(10 Marks)**

OR

6 a. With a neat logic symbol, logic diagram and truth table, write the data flow description of half adder. **(08 Marks)**

b. Design a 2 × 2 unsigned combinational array multiplier and write the data flow description for the same. **(12 Marks)**

Module-4

7 a. With a neat diagram, explain the basic ROM structure. **(06 Marks)**

b. Realize AND-OR array [PLA] for the given functions and also write the PLA table for the same.

Functions → $F_0 = A'B' + AC'$ | $F_2 = A'B' + BC'$

$F_1 = B + AC'$ | $F_3 = AC + B$

(07 Marks)

c. With a neat diagram, explain combinational PAL segment. **(07 Marks)**

OR

8 a. With a neat block diagram, state graph and state table, explain the design of serial adder with accumulator. **(10 Marks)**

b. With a neat block diagram and state graph, explain the design of a binary multiplier. **(10 Marks)**

Module-5

9 a. For the given logic symbol, write the truth table, logic diagram and VHDL code for the signal assignment statement y = 2 * x + 3. **(10 Marks)**

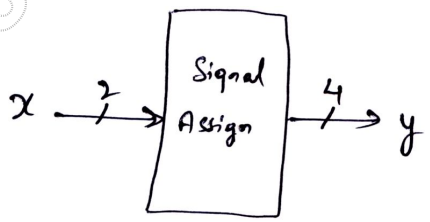

Fig.Q.9(a)

b. With the example, explain the following VHDL statements:
i) If Statement ii) For Loop Statement. **(10 Marks)**

OR

10 a. With a neat diagram, explain the following:
i) Testing AND and OR gates for stuck-at faults
ii) Testing AND-OR network (2 level). **(10 Marks)**

b. With a neat diagram, explain the standard Mealy sequential network and the corresponding iterative network. **(10 Marks)**

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