CBCS SCHEME

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18EI/BM/ML33

Third Semester B.E. Degree Examination, July/August 2022
Analog Electronic Circuits

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Obtain the expressions for I_B and V_{CE} of BJT fixed bias configuration. **(06 Marks)**

b. Derive base current and collector to emitter voltage for BJT emitter-follower configuration. **(06 Marks)**

c. A BJT voltage-divider configuration has V_{CC} = 22 V, R_1 = 39 KΩ, R_2 = 3.9 KΩ, R_E = 1.5 KΩ, R_C = 10 KΩ, β = 100, $C_1 = C_2$ = 10 μF, C_E = 50 μF.
(i) Determine dc bias voltage V_{CE} and current I_C using exact analysis.
(ii) Determine I_{CQ} and V_{CEQ} using appropriate technique.
(iii) Compare solutions for I_{CQ} and V_{CEQ}. **(08 Marks)**

OR

2 a. Derive the expressions for V_{GS} and V_{DS} of FET voltage-divider bias circuit. Sketch the network equation and show the effect of R_s on operating point. **(12 Marks)**

b. Determine the following parameter for network in Fig.Q2(b):
(i) V_{GSQ} (ii) I_{DQ} (iii) V_{DS} (iv) V_D (v) V_G (vi) V_S

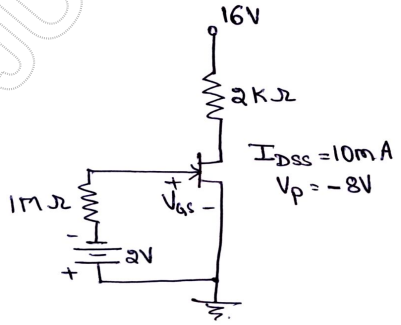

Fig.Q2(b) **(08 Marks)**

Module-2

3 a. Define a model. Summarize the steps to obtain the ac equivalent of transistor network. **(05 Marks)**

b. Give the r_e equivalent circuit for CE emitter-bias configuration. Derive the equations for Z_i, Z_o and A_v without considering the effect of r_o for unbypassed configuration. **(10 Marks)**

c. For the network in Fig.Q3(c): (i) Determine r_e (ii) Find Z_i (with $r_0 = \infty\Omega$)
(iii) Calculate Z_o (with $r_0 = \infty\Omega$) (iv) Determine A_v (with $r_0 = \infty\Omega$)

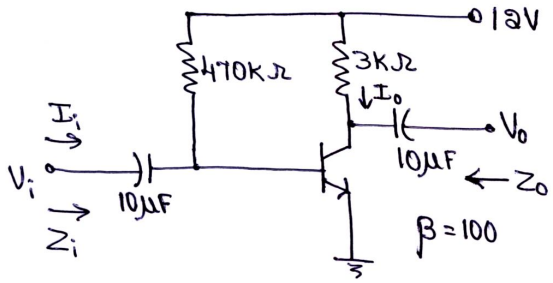

Fig.Q3(c) **(05 Marks)**

OR

4 a. Derive the h-parameters of a two-port system. **(10 Marks)**

b. Explain hybrid π model with circuit and expressions. **(10 Marks)**

Module-3

5 a. With necessary expressions, give the mathematical definition of g_m. **(08 Marks)**

b. Determine input impedance, output impedance and voltage gain of JFET source-follower configuration. **(12 Marks)**

OR

6 a. Explain the gain response curves for the following amplifiers:
(i) RC-coupled amplifiers
(ii) Transformer-coupled amplifier
(iii) Direct-coupled amplifier **(10 Marks)**

b. Describe the Miller effect capacitance with necessary expressions. **(10 Marks)**

Module-4

7 a. Define power amplifier. Explain the various classes of power amplifier. **(06 Marks)**

b. Obtain expressions for input power, output power and maximum efficiency of class B push-pull amplifier. **(08 Marks)**

c. Calculate the maximum efficiency of a transformer coupled class A amplifier for a supply of 12 V and outputs of (i) $V_{(p)}$ = 12 V (ii) $V_{(p)}$ = 6 V (iii) $V_{(p)}$ = 2V **(06 Marks)**

OR

8 a. Explain the working of complementary-symmetry push-pull circuit. Add a note on crossover distortion. **(08 Marks)**

b. With a block diagram, explain class D amplifier. **(06 Marks)**

c. Calculate harmonic distortion components and total harmonic distortion of an output signal having fundamental amplitude of 2.5 V, second harmonic amplitude of 0.25V, third harmonic amplitude of 0.1V and fourth harmonic amplitude of 0.05V. **(06 Marks)**

Module-5

9 a. Describe a feedback amplifier with block diagram. List the benefits of negative feedback. **(06 Marks)**

b. Explain FET based voltage-series feedback with circuit and expressions. **(08 Marks)**

c. Calculate the voltage gain with and without feedback for the circuit given in Fig.Q9(c).

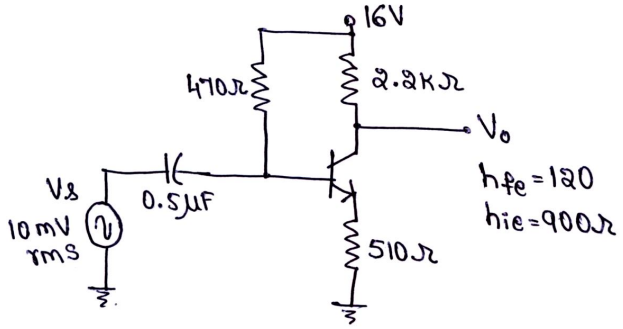

Fig.Q9(c) **(06 Marks)**

OR

10 a. What is Barkhausen criteria? Explain. **(06 Marks)**

b. With circuit and waveforms, explain unijunction oscillator. **(08 Marks)**

c. Explain the transistor Hartley oscillator circuit with expressions and circuit. **(06 Marks)**

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