CBCS SCHEME

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18EI72

Seventh Semester B.E. Degree Examination, Feb./Mar. 2022
ARM Processor

Time: 3 hrs. Max. Marks: 100

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. Differentiate between RISC and CISC Architecture. **(06 Marks)**

b. Explain various AMBA bus protocol used in ARM processor highlighting their performance characteristics. **(06 Marks)**

c. With neat diagram, explain the ARM core data flow model. **(08 Marks)**

OR

2 a. What is Instruction Pipelining? Explain with an example. And also compare the performance of ARM7, ARM9 and ARM10 processor with different pipelining stages. **(08 Marks)**

b. With neat block diagrams, explain Von – Nuemann and Harvard architectures with cache and tightly coupled memories. **(08 Marks)**

c. Discuss the significance of R13, R14, R15 and CPSR register in ARM processor. **(04 Marks)**

Module-2

3 a. With an example and block diagram, discuss the Barrel shifter operation of ARM processor and list various barrel shifter operations. **(08 Marks)**

b. Describe the operation of following instructions by considering suitable data :
i) ADD r_0, r_1, r_2, LSL # 1 ii) BIC r_0, r_1, r_2 iii) UMULL r_0, r_1, r_2, r_3. **(06 Marks)**

c. Write an assembly language program to add two 64 bit numbers and store the result in result variable. **(06 Marks)**

OR

4 a. With an examples discuss the various addressing modes supported by single register load and store instructions. **(06 Marks)**

b. List the various branch instructions available in ARM processor and explain its operation. **(08 Marks)**

c. Write an assembly language program to count number of zero's and one's in two consecutive memory locations. **(06 Marks)**

Module-3

5 a. With an example justify that the thumb code is more efficient than ARM code. **(06 Marks)**

b. Examine the operation of following thumb mode instructions by considering suitable data :
i) STMIA r_4! , {r_1, r_2, r_3} ii) PUSH {r_1, ℓ_r} iii) LDR r_0, [r_1, r_4]
iv) SWI 0×45 v) BLX R_m. **(10 Marks)**

c. Explain the usage of general purpose register in thumb mode. **(04 Marks)**

OR

6 a. With an example justify that use of C data type int will increase the ARM processor performance and reduces code size than using type char and short. **(06 Marks)**

b. Discuss the efficient use of C data types. **(06 Marks)**

c. Explain the working of loops with a fixed number of iteration with an example and mention the efficient use of loops. **(08 Marks)**

Module-4

7 a. Define Exception. Explain the various exceptions handled by ARM processor starting with the highest priority. **(10 Marks)**

b. Discuss IRQ and FIQ exceptions with standard procedure. **(06 Marks)**

c. Write the instructions to disable IRQ and FIQ interrupt. **(04 Marks)**

OR

8 a. List the different interrupt handling schemes and explain the following interrupt handling schemes : i) Nested interrupt handler ii) Prioritized standard interrupt handler. **(12 Marks)**

b. Explain the two stages of context switching. **(08 Marks)**

Module-5

9 a. With neat diagram, explain the memory hierarchy and cache memory. And also explain the non cached and cached system. **(10 Marks)**

b. Explain the relationship between Cache and main memory. Discuss trashing in direct mapped caches. **(10 Marks)**

OR

10 a. Explain mapping a task in virtual memory to physical memory using a relocation register. **(08 Marks)**

b. Explain level 1 page table entry types. **(08 Marks)**

c. Define Page , Page table , Page frame and Translational look aside buffer. **(04 Marks)**

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