CBCS SCHEME

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18EI/BM34

Third Semester B.E. Degree Examination, July/August 2022
Digital Design and HDL

Time: 3 hrs. Max. Marks: 100

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. Define Minterm and Maxterm Canonical form. Give an example for each. **(04 Marks)**

b. Simplify f(A, B, C, D) = Σm (2, 3, 4, 5, 13, 15) + Σd(8, 9, 10, 11) using K – map. Implement the circuit using logic gates. **(08 Marks)**

c. Using QM technique reduce the following Boolean equation
f(a, b, c, d) = Σm(0, 1, 2, 3, 8, 9). **(08 Marks)**

OR

2 a. Define sum of product and product of sum. Give an example for each. **(04 Marks)**

b. Convert f1 = a $\overline{b}$ + a $\overline{c}$ + bc into minterms and canonical form. f2 = (a + $\overline{b}$) ($\overline{b}$ + c) into maxterms, Canonical forms. **(06 Marks)**

c. Simplify the equation using QM technique.
D = f(a, b, c, d) = Σ(0, 1, 2, 3, 6, 7, 8, 9, 14, 15). **(10 Marks)**

Module-2

3 a. Design a full subtractor using logic gates. **(08 Marks)**

b. Implement the following using 74138(3 to 8) decoder. $f_1(a, b, c) = \Sigma m(0, 4, 6, 7,)$,
$f_2(a, b, c) = \pi m(2, 3, 6, 7)$. **(06 Marks)**

c. Realize 4 : 1 MUX using basic gates. **(06 Marks)**

OR

4 a. What is the disadvantages of ripple carry adder? Explain how it can overcome by carry look ahead adder. **(08 Marks)**

b. Construct a 4 to 16 line decoder using two 74138IC. **(06 Marks)**

c. Design a combinational logic circuit using PROM for the following Boolean expression.
$f_1(x_2, x_1, x_0) = \Sigma m(0, 1, 2, 5, 7)$; $f_2(x_2, x_1, x_0) = \Sigma m(1, 2, 4, 6)$. **(06 Marks)**

Module-3

5 a. With neat logic diagram and truth table, explain the working of SR latch. **(08 Marks)**

b. Explain the working of Master slave JK flip flop with functional table and timing diagram. **(08 Marks)**

c. Derive the characteristics equation of D flip flop. **(04 Marks)**

OR

6 a. With neat diagram, explain the working of positive edge triggered D flip flop. **(10 Marks)**

b. With neat circuit and timing diagram, explain the application of SR flip flop as a switch debouncer. **(10 Marks)**

Module-4

7 a. Explain the working of Universal shift register along with its mode control table. **(10 Marks)**

b. With neat logic diagram and timing diagram, explain 4 bit ripple up counter using T flip flop. **(10 Marks)**

OR

8 a. Design a mod 6 counter using JK flip flop to generate the following sequence.
$0 \rightarrow 2 \rightarrow 3 \rightarrow 6 \rightarrow 5 \rightarrow 1 \rightarrow 0$. **(10 Marks)**

b. Design Shift register based ring counter and Johnson counter. **(10 Marks)**

Module-5

9 a. Explain the following verilog operators :
i) Reduction logic operators ii) Relational operators iii) Arithmetic operators
iv) Shift operators v) Boolean logic operators. **(10 Marks)**

b. Explain the following data types in verilog with example :
i) Parameter ii) Arrays. **(04 Marks)**

c. Write the verilog description of full adder using dataflow description. **(06 Marks)**

OR

10 a. Illustrate if and else if sequential statements. **(06 Marks)**

b. Illustrate the any 2 types of loop statements of verilog. **(06 Marks)**

c. Write verilog behavioral description of 4:1 MUX along with its functional table and logic diagram. And also write its simulation waveform. **(08 Marks)**

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