CBCS SCHEME

USN | | | | | | | | | | |

18EI/BM56

Fifth Semester B.E. Degree Examination, Jan./Feb. 2021
VLSI Design

Time: 3 hrs. Max. Marks: 100

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. State and explain Moore's Law. **(06 Marks)**

b. Give the comparison between CMOS and Bipolar technologies. **(06 Marks)**

c. With a neat diagram, explain fabrication steps in nMOS process. **(08 Marks)**

OR

2 a. Obtain the expression for drain to source current Ids versus voltage Vds for non saturated region of MOS transistor. **(12 Marks)**

b. Define transconductance. Obtain the expression for MOS transistor transconductance (g_m). **(08 Marks)**

Module-2

3 a. Obtain the pull-up to pull-down ratio for or nMOS inverter driven through one/more pass transistors. **(12 Marks)**

b. Discuss the alternative forms of pull-up transistor. **(08 Marks)**

OR

4 a. Define sheet resistance Rs. How the sheet resistance can be calculated for the MOS transistor and inverter. **(10 Marks)**

b. Estimate the CMOS inverter delay using rise-time and fall-time model. **(10 Marks)**

Module-3

5 a. Name the four basic layers of MOS circuits. **(02 Marks)**

b. What is lambda–based design rules for the wires and transistors in nMOS and CMOS technology? **(08 Marks)**

c. Draw the tick diagrams for the following :
   i) P-well CMOS inverter
   ii) Simple n-well based BICMOS inverter
   iii) 4 : 1 nMOS inverter. **(10 Marks)**

OR

6 a. Give the scaling factor for the following parameters.
   i) Gate capacitance per unit area Cg
   ii) Channel resistance Ron
   iii) Maximum Operating Frequency f_0
   iv) Switching energy per gate Eg
   v) Power dissipation per gate Pg. **(10 Marks)**

b. Discuss limitations of scaling with respect to following parameters
   i) Substrate doping
   ii) Limits due to subthreshold currents. **(10 Marks)**

Module-4

7 a. With circuit and equations, discuss the Pseudo – nMOS logic. **(10 Marks)**

b. Explain a four-line gray code to binary code converter. **(10 Marks)**

OR

8 a. Discuss nMOS and CMOS per charged bus. **(10 Marks)**

b. Describe nMOS four–bit dynamic shift register. Give the stick drag rams of nMOS and CMOS shift register cell. **(10 Marks)**

Module-5

9 a. Explain the implementation of ALU functions using an adder. **(12 Marks)**

b. Discuss 4-bit serial parallel multipher. **(08 Marks)**

OR

10 a. Define regularity. **(02 Marks)**

b. Describe the operation of three transistor dynamic RAM cell and write its stick diagram. **(08 Marks)**

c. What are to be considered in the designer's tool box for the chip design in CAD tools and explain simulation? **(10 Marks)**

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