Visvesvaraya Technological University, Belagavi.
PhD Coursework Courses – 2018 (Electronics and Communication Engineering)
As per 2017 Regulation

GROUP-1		
Sl. No.	**Course Code**	**Course Name**
1	16ECS14	ADVANCED DIGITAL COMMUNICATION
2	16ECS21	ADVANCED DSP
3	16ESP14	Modern DSP
4	16ELD14	DIGITAL CIRCUITS AND LOGIC DESIGN
5	16ELD41	Synthesis and Optimization of Digital Circuits
6	16EIE252	Sensors and Transducers
7	16ELD251	Automotive Electronics
8	16EIE12	ADVANCED CONTROL SYSTEMS

GROUP-2		
Sl. No.	**Course Code**	**Course Name**
1	16ECS23	WIRELESS COMMUNICATION
2	16ECS422	Advances in Image Processing
3	16ESP22	DSP System Design
4	16ESP23	Digital Signal Copmression
5	16EVE12	DIGITAL VLSI DESIGN
6	16ELD424	Reconfigurable Computing
7	16EVE152	NANOELECTRONICS
8	16EIE23	Process Control Instrumentation

GROUP-3		
Sl. No.	**Course Code**	**Course Name**
1	16ECS22	ERROR CONTROL CODING
2	16ESP254	CHANNEL CODING
3	16ESP21	Image Processing and Machine Vision
4	16ESP421	Array Signal Processing
5	16EVE151	DIGITAL SYSTEM DESIGN USING VERILOG
6	16ELD154	ADVANCED COMPUTER ARCHITECTURE
7	16EVE251	System Verilog
8	16ELD253	Micro Electro Mechanical Systems
9	16EIE151	PLCS AND INDUSTRIAL AUTOMATION

Visvesvaraya Technological University, Belagavi.

PhD Coursework Courses – 2018 (Electronics and Communication Engineering)

As per 2017 Regulation

GROUP-4		
Sl. No.	**Course Code**	**Course Name**
1	16ECS12	ANTENNA THEORY AND DESIGN
2	16ESP422	Speech and Audio Processing
3	16ESP12	Statistical Signal Processing
4	16ESP251	Detection and Estimation
5	16EVE21	Design of Analog and Mixed Mode VLSI Circuits
6	16EVE23	Advances in VLSI Design
7	16EIE22	Design of Power Converters

GROUP-5		
Sl. No.	**Course Code**	**Course Name**
1	16ECS153	OPTICAL COMMUNICATION AND NETWORKING
2	16ECS151	ADVANCED COMPUTER NETWORKS
3	16ECS254	CRYPTOGRAPHY AND NETWORK SECURITY
4	16ESP24	Biomedical Signal Processing
5	16ESP253	Pattern Recognition
6	16EVE24	Real Time Operating System
7	16ECS424	Real Time Systems
8	16EVE153	ASIC DESIGN
9	16EVE13	ADVANCED EMBEDDED SYSTEM
10	16EVE14	LOW POWER VLSI DESIGN
11	16EIE424	Industrial Drive

GROUP-6		
Sl. No.	**Course Code**	**Course Name**
1	16ECS252	MULTIMEDIA OVER COMMUNICATION LINKS
2	16ECS24	RF AND MICROWAVE CIRCUIT DESIGN
3	16ESP41	Adaptive Signal Processing
4	16ESP152	Multirate Systems and Filter Banks
5	16ESP153	MODERN SPECTRAL ANALYSIS & ESTIMATION
6	16ECS423	Communication System Design using DSP Algorithms
7	16ECS154	SIMULATION, MODELLING AND ANALYSIS
8	16EVE22	VLSI Testing
9	16EVE254	SoC Design
10	16EVE423	High Speed VLSI Design
11	16EVE421	CMOS RF Circuit Design
12	16EVE252	VLSI Design for Signal Processing
13	16EIE423	Medical Imaging
14	16EIE421	Advanced Power Electronic Converters and Applications
15	16ELD11	ADVANCED ENGINEERING MATHEMATICS

Visvesvaraya Technological University, Belagavi.
PhD Coursework Courses – 2018 (Electronics and Communication Engineering)
As per 2017 Regulation

01	16ECS14	Group-1	ADVANCED DIGITAL COMMUNICATION
Exam Hours:03		**Exam Marks:100**	

Module -1 Digital Modulation Schemes: Representation of Digitally Modulated Signals, Memoryless Modulation Methods-PAM, Phase Modulation, QAM, Multidimensional Signalling, Signalling Schemes with memory: CPFSK, CPM, MSK, OQPSK. Transmit PSD for Modulation Schemes (Chapter 3: 3.1,3.2,3.3, 3.4.1 and 3.4.2 of Text).

Module -2 Optimum Receivers for AWGN channels: Waveform and Vector channel models, Waveform and Vector AWGN channels- Optimal detection, Implementation, Optimal Detection and Error Probability for Band limited signaling, Optimal detection and error probability for power limited signaling. Non Coherent Detection (without derivations) (Chapter 4: 4.1, 4.2 - 4.2.1, 4.2.2, 4.3, 4.4, 4.5.1, 4.5.2, eqn 4.5.45 to 4.5.47, 4.5.5 up to eqn 4.5.62 of Text).

Module -3 Multichannel and Multicarrier Signaling: Multichannel Communications in an AWGN channel, Multicarrier Communications in AWGN channel (Chapter 11- 11.1, 11.2-1 to 11.2-5 of Text).
Synchronization: Signal Parameter estimation, Carrier Phase Estimation, Symbol Timing Recovery (Chapter 5- 5.1 to 5.3 of Text).

Module -4 Digital Communication through band-limited channels: Characterization of Band-limited channels, Optimum Receiver for channels with ISI and AWGN, Linear equalization, Decision feedback equalization (Chapter 9: 9.1,9.3- 9.3.1, 9.3.2, 9.4- 9.4.1, 9.4.2, 9.4.4, 9.4.5, 9.5- 9.5.1, 9.5.3 of Text).
Adaptive equalization: Adaptive linear equalizer, adaptive decision feedback equalizer, Adaptive equalization of Trellis - coded signals (Chapter 10: 10.1, 10.2, 10.3 of Text).

Module -5 Spread spectrum signals for digital communication:
Model of spread spectrum digital communication system, Direct sequence spread spectrum signals, Frequency hopped spread spectrum signals, CDMA, Time hopping SS, Synchronization of SS systems (Chapter 12 of Text).

Question paper pattern:

- The question paper will have ten questions.
- Each full question consists of 20 marks.
- There will be 2 full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub questions covering all the topics under a module.

The students will have to answer 5 full questions, selecting one full question from each module.

Reference: Book:

1. Bernard Sklar, "Digital Communication - Fundamental and applications", Pearson education (Asia), Pvt. Ltd., 2nd edition, 2001.

Text Book:

1. John G. Proakis, Masoud Salehi, "Digital Communications", McGraw Hill, 5th Edition, 2008.

Visvesvaraya Technological University, Belagavi.
PhD Coursework Courses – 2018 (Electronics and Communication Engineering)
As per 2017 Regulation

02	16ECS21	Group-1	ADVANCED DSP
Exam Hours:03		**Exam Marks:100**	

Module -1 Multirate Digital Signal Processing: Introduction, decimation by a factor 'D', Interpolation by a factor 'I', sampling rate conversion by a factor 'I/D', Implementation of sampling rate conversion, Multistage implementation of sampling rate conversion, Applications of multirate signal processing, Digital filter banks, two channel quadrature mirror filter banks, M-channel QMF bank. (Text 1)

Module -2 Linear prediction and Optimum Linear Filters: Random signals, Correlation Functions and Power Spectra, Innovations Representation of a Stationary Random Process. Forward and Backward Linear Prediction. Solution of the Normal Equations The Levinson-Durbin Algorithm. Properties of the Linear Prediction-Error Filters. (Text 1)

Module -3 Adaptive filters: Applications of adaptive filters- Adaptive channel equalization,, Adaptive noise cancellation, Linear Predictive coding of Speech Signals, Adaptive direct form FIR filters-The LMS algorithm, Properties of LMS algorithm.
Adaptive direct form filters- RLS algorithm. (Text 1)

Module -4 Power Spectrum Estimation: Non parametric Methods for Power Spectrum Estimation - Bartlett Method, Welch Method, Blackman and Tukey Methods.
Parametric Methods for Power Spectrum Estimation: Relationship between the auto correlation and the model parameters, Yule and Walker methods for the AR Model Parameters, Burg Method for the AR Model parameters, Unconstrained least-squares method for the AR Model parameters, Sequential estimation methods for the AR Model parameters, ARMA Model for Power Spectrum Estimation. (Text 1)

Module -5 WAVELET TRANSFORMS: The Age of Wavelets, The origin of Wavelets, Wavelets and other reality transforms, History of wavelets, Wavelets of the future.
Continuous Wavelet and Short Time Fourier Transform: Wavelet Transform, Mathematical preliminaries, Properties of wavelets.
Discrete Wavelet Transform: Haar scaling functions, Haar wavelet function, Daubechies Wavelets. (Chapters 1, 3 & 4 of Text 2)

Question paper pattern:

- The question paper will have ten questions.
- Each full question consists of 20 marks.
- There will be 2 full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub questions covering all the topics under a module.

The students will have to answer 5 full questions, selecting one full question from each module.

Reference Books

1. "Modern Digital signal processing", Robert. O. Cristi, Cengage Publishers, India, 2003.
2. "Digital signal processing: A Practitioner's approach", E.C. Ifeachor, and B. W. Jarvis, , Second Edition, Pearson Education, India, 2002, Reprint.
3. "Wavelet Transforms, Introduction to Theory and applications", Raghuveer. M. Rao, Ajit S.Bopardikar, Pearson Education, Asia, 2000.

Text Books:

1. "Digital Signal Processing, Principles, Algorithms and Applications", John G.Proakis, Dimitris G.Manolakis, Fourth edition, Pearson-2007.
2. Insight into Wavelets- from Theory to Practice", K.P Soman, Ramachandran, Resmi- PHI Third Edition-2010.

Visvesvaraya Technological University, Belagavi.
PhD Coursework Courses – 2018 (Electronics and Communication Engineering)
As per 2017 Regulation

Visvesvaraya Technological University, Belagavi.

PhD Coursework Courses – 2018 (Electronics and Communication Engineering)

As per 2017 Regulation

03	16ESP14	Group-1	Modern DSP
Exam Hours:03		**Exam Marks:100**	

Module -1 Introduction:

Multirate Digital Signal Processing: Introduction, Decimation by a factor 'D', Interpolation by a factor 'I', Sampling rate Conversion by a factor 'I/D', implementation of Sampling rate conversion, Multistage implementation of Sampling rate conversion, Sampling rate conversion of Band Pass Signals, Sampling rate conversion by an arbitrary factor, Applications of Multirate Signal Processing, Digital Filter banks, Two Channel Quadrature Mirror Filter banks, M-Channel QMF bank (Text 1).

Module -2 Transform Analysis of LTI systems: The frequency response of LTI systems, System functions for systems characterized by linear constant coefficient difference equations, frequency response for rational system functions, Relationship between magnitude and phase, All pass systems, minimum phase systems, linear systems with generalized linear phase (Text 2).

Module -3 Linear Prediction and Optimum Linear Filters:

Representation of a random process, Forward and backward linear prediction, Solution of normal equations, Properties of the linear error-prediction filters, AR lattice and ARMA lattice-ladder filters, Wiener filters for filtering and prediction (Text 1).

Module -4 Time frequency transformation: The Fourier Transform: Its Power and Limitations, The short Time Fourier Transform, The Gabor transform, The wavelet transform, Perfect reconstruction Filter Banks and Wavelets, Recursive Multi resolution Decomposition, Haar Wavelet (Text 3).

Module -5 Hardware and Software for Digital Signal Processors: Digital signal processor architecture, Digital signal processor hardware units, Fixed- point and floating-point formats (Text 4).

Question paper pattern:

- The question paper will have ten questions.
- Each full question consists of 20 marks.
- There will be 2 full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub questions covering all the topics under a module.

The students will have to answer 5 full questions, selecting one full question from each module.

Text Books:

1. Proakis and Manolakis, "Digital Signal Processing", Prentice Hall, 4th edition, 1996.
2. Alan V. Oppenheim and Ronald W.Schafer, "Discrete-Time signal Processing", PHI Learning, 2003.
3. Roberto Cristi, "Modern Digital Signal Processing", Cengage Publishers, India, Eerstwhile Thompson Publications, 2003.
4. Li Tan, "Digital Signal Processing – Fundamentals and Applications", Elsevier, 2008.

Reference Book:

1. S.K.Mitra, "Digital Signal Processing: A Computer Based Approach", 3rd edition, Tata McGraw Hill, India, 2007.

Visvesvaraya Technological University, Belagavi.
PhD Coursework Courses – 2018 (Electronics and Communication Engineering)
As per 2017 Regulation

04	16ELD14	Group-1	DIGITAL CIRCUITS AND LOGIC DESIGN
Exam Hours:03		**Exam Marks:100**	

Module -1 Threshold Logic: Introductory Concepts, Synthesis of Threshold Networks, Capabilities, Minimization, and Transformation of Sequential Machines: The Finite- State Model, Further Definitions, Capabilities.

Module -2 Fault Detection by Path Sensitizing, Detection of Multiple Faults, Failure-Tolerant Design, Quadded Logic, Reliable Design and Fault Diagnosis Hazards: Fault Detection in Combinational Circuits.

Module -3 Fault-Location Experiments, Boolean Differences, Limitations of Finite – State Machines, State Equivalence and Machine Minimization, Simplification of Incompletely Specified Machines.

Module -4 Structure of Sequential Machines: Introductory Example, State Assignments Using Partitions, The Lattice of closed Partitions, Reductions of the Output Dependency, Input Independence and Autonomous Clocks, Covers and Generation of closed Partitions by state splitting, Information Flow in Sequential Machines, ELDecompositions, Synthesis of Multiple Machines.

Module -5 State Identifications and Fault-Detection Experiments: Homing Experiments, Distinguishing Experiments, Machine Identification, Fault Detection Experiments, Design of Diagnosable Machines, Second Algorithm for the Design of Fault Detection Experiments, Fault-Detection.

Question paper pattern:

- The question paper will have ten questions.
- Each full question consists of 20 marks.
- There will be 2 full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub questions covering all the topics under a module.

The students will have to answer 5 full questions, selecting one full question from each module.

Text Book:

1.Zvi Kohavi, “Switching and Finite Automata Theory”, 2nd Edition, TMH.

Reference Books:

1. Charles Roth Jr., “Digital Circuits and logic Design”, 7th edn, Cengage Learning, 2014.
2. Parag K Lala, “Fault Tolerant And Fault Testable Hardware Design”, Prentice Hall Inc. 1985.
3. E. V. Krishnamurthy, “Introductory Theory of Computer”, Macmillan Press Ltd, 1983
4. Mishra & Chandrasekaran, “Theory of computer science – Automata, Languages and Computation”, 2nd Edition, PHI, 2004.

Visvesvaraya Technological University, Belagavi.
PhD Coursework Courses – 2018 (Electronics and Communication Engineering)
As per 2017 Regulation

05	16ELD41	Group-1	Synthesis and Optimization of Digital Circuits
Exam Hours:03		**Exam Marks:100**	

Module -1 Introduction to Synthesis and optimization: Design of Microelectronics circuits, Computer aided Synthesis and Optimization.
Hardware Modeling: HDLs for Synthesis, Abstract models, Compilation and Behavioral Optimization. (Text1: Topics from Chap. 1,3).

Module -2 Graph theory for CAD for VLSI: Graphs, Combinatorial Optimization, Graph Optimization problems and Algorithms, Boolean Algebra and Applications.
Architectural Synthesis and Optimization: Fundamental Architectural Synthesis problems, Area and Performance Estimation, Strategies for Architectural Optimization, Datapath Synthesis, Control Path Synthesis.(Text1: Topics From Chap. 2,4).

Module -3 Two level Combinational Logic Optimization: Introduction, Logic Optimizations, Operations on Two level Logic Covers, Algorithms for Logic Minimization, Symbolic Minimization and Encoding Problems.
Multiple Level Combinational Logic Optimization: Introduction, Models and Transformations for Combinational Networks, The Algebraic Model, The Boolean Model. (Text1: Chap. 7, 8).

Module -4 Sequential Logic Optimization:
Introduction, Sequential Logic Optimization using State based Models, Sequential Logic Optimization using Network Models, Implicit FSM Traversal Methods, Testability concerns for Synchronous Circuits. (Text 1: Chap. 9).

Module -5 Scheduling Algorithms: Introduction, A Model for Scheduling problems, Scheduling with Resource Constraints, Scheduling without Resource Constraints, Scheduling Algorithms for Extended Sequencing Models, Scheduling Pipelined Circuits.
Resource Sharing and Binding: Sharing and Binding for Resource dominated circuits, Sharing and Binding for General Circuits, Concurrent Binding and Scheduling, Resource sharing and Binding for Non – Scheduled Sequencing Graphs. (Text1: Chap. 5,6)**.**

Question paper pattern:

- The question paper will have ten questions.
- Each full question consists of 20 marks.
- There will be 2 full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub questions covering all the topics under a module.

The students will have to answer 5 full questions, selecting one full question from each module.

Text Book:
Giovanni De Micheli, ―Synthesis and Optimization of Digital Circuits‖, Tata McGraw-Hill, 2003.
Reference Book:
Edwars M.D., Automatic Logic synthesis Techniques for Digital Systems, Macmillan New Electronic Series, 1992.

Visvesvaraya Technological University, Belagavi.

PhD Coursework Courses – 2018 (Electronics and Communication Engineering)

As per 2017 Regulation

06	16EIE252	Group-1	Sensors and Transducers
Exam Hours:03		**Exam Marks:100**	

Module -1 Measurements and Instrumentation of Transducers: Measurements, Basic method of measurement, Generalized scheme for measurement systems, Errors, Classification of errors, error analysis, Statistical methods, Sensor, Transducer, Classification of transducers, Basic requirement of transducers. (Text 1).

Module -2 Measurement of Strain: Introduction, Factors affecting strain measurements, Types of Strain Gauges, Theory of operation of resistance strain gauges, Types of Electrical Strain Gauges – Wire gauges, unbounded strain gauges, foil gauges, semiconductor strain gauges principle, types, Materials for Strain Gauges, Strain gauge Circuits – Wheatstone bride circuit, Applications. (Text 1 & 2).

Module -3 Measurement of Force & Torque: Introduction, Force measuring sensor – Load cells – column types devices, proving rings, cantilever beam, pressductor. Hydraulic load cell, Electronic weighing system. Torque measurement: Absorption type, transmission type, stress type & deflection type. (Text 2)

Module -4 Measurement of Pressure: Introduction, Diaphragms, Other elastic elements, Transduction methods – potentiometric device, strain gauge transducer, variable reluctance, LVDT type, variable capacitance device, force balance transducer with analysis, thin-film pressure transducers, piezoelectric pressure transducer, pressure multiplexer, pressure calibration. (Text 2).

Module -5 Miscellaneous Sensors and Transducers: Noise (sound) Sensors, Speed Sensors, Thickness Measurement, Weather stations. Piezoelectric transducer, Hall Effect transducers, Smart sensors, Fiber optic sensors, Film sensors, MEMS, Nano sensors, Digital transducers. (Text 1 & 3)**.**

Question paper pattern:

- The question paper will have ten questions.
- Each full question consists of 20 marks.
- There will be 2 full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub questions covering all the topics under a module.

The students will have to answer 5 full questions, selecting one full question from each module.

Text Books:

1. Sawhney. A.K, ―A Course in Electrical and Electronics Measurements and Instrumentation‖, 18th Edition, Dhanpat Rai & Company Private Limited, 2007.
2. C. S. Rangan, G. R. Sarma, V. S. V. Mani , ―Instrumentation: Devices and Systems‖, 2nd Edition (32nd Reprint), McGraw Hill Education (India), 2014.
3. Bela G. Liptak, ―Process Measurement Instrument Engineers Handbook‖, Revised Edition, Chilton Book Company, 1982.

Reference Books:

1. John. P, Bentley, ―Principles of Measurement Systems‖, III Edition, Pearson Education, 2000.
2. Murthy. D. V. S, ―Transducers and Instrumentation‖, Prentice Hall of India, 2001.
3. Doebelin. E.A, ―Measurement Systems – Applications and Design‖, Tata McGraw Hill, New York, 2000.
4. Patranabis. D, ―Sensors and Transducers‖, Prentice Hall of India, 1999.

Visvesvaraya Technological University, Belagavi.
PhD Coursework Courses – 2018 (Electronics and Communication Engineering)
As per 2017 Regulation

07	16ELD251	Group-1	Automotive Electronics
Exam Hours:03		**Exam Marks:100**	

Module -1 Automotive Fundamentals, the Systems Approach to Control and Instrumentation:
Use Of Electronics In The Automobile, Antilock Brake Systems, (ABS), Electronic steering control, Power steering, Traction control, Electronically controlled suspension. (Chap.1 and 2 of Text)

Module -2 Automotive instrumentation Control: Sampling, Measurement and signal conversion of various parameters. (Chap. 4 of Text)

Module -3 The basics of Electronic Engine control: Integrated body: Climate controls, Motivation for Electronic Engine Control, Concept of An Electronic Engine Control System, Definition of General Terms, Definition of Engine Performance Terms, Electronic fuel control system, Engine control sequence, Electronic Ignition, Sensors and Actuators, Applications of sensors and actuators, air flow rate
sensor, Indirect measurement of mass air flow, Engine crankshaft angular position sensor, Automotive engine control actuators, Digital engine control, Engine speed sensor ,Timing sensor for ignition and fuel delivery, Electronic ignition control systems, Safety systems, Interior safety, Lighting, Entertainment systems.(Chap. 5 and 6 of Text).

Module -4 Vehicle Motion Control and Automotive diagnostics: Cruise control system, Digital cruise control, Timing light, Engine analyzer, On-board and off-board diagnostics, Expert systems. Stepper motorbased actuator, Cruise control electronics, Vacuum – antilock braking system, Electronic suspension system Electronic steering control, Computer-based instrumentation system, Sampling and Input\output signal conversion, Fuel quantity measurement, Coolant temperature measurement, Oil pressure measurement, Vehicle speed measurement, Display devices, Trip-Information-Computer, Occupant protection systems. (Chap. 8 and 10 of Text)

Module -5 Future automotive electronic systems: Alternative Fuel Engines, Collision Wide Range Air/Fuel Sensor, Alternative Engine, Low Tire Pressure Warning System, Collision avoidance Radar Warning Systems, Low Tire Pressure Warning System, Radio Navigation, Advance Driver information System. Alternative-Fuel Engines, Transmission Control , Collision Avoidance Radar Warning System, Low Tire Pressure Warning System, Speech Synthesis Multiplexing in Automobiles, Control Signal Multiplexing, Navigation Sensors, Radio Navigation, Sign post Navigation , Dead Reckoning Navigation Future Technology, Voice Recognition Cell Phone Dialing Advanced Driver information System, Automatic Driving Control. (Chap. 11 of Text)

Question paper pattern:

- The question paper will have ten questions.
- Each full question consists of 20 marks.
- There will be 2 full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub questions covering all the topics under a module.

The students will have to answer 5 full questions, selecting one full question from each module.

Text Book:

1. William B. Ribbens, "Understanding Automotive Electronics", SAMS/Elsevier publishing, 6th Edition, 1997.

Reference Book:

1. Robert Bosch Gmbh,"Automotive Electrics and Automotive Electronics- Systems and Components, Networking and Hybrid Drive", Springer Vieweg, 5th Edition, 2007.

Visvesvaraya Technological University, Belagavi.
PhD Coursework Courses – 2018 (Electronics and Communication Engineering)
As per 2017 Regulation

08	16EIE12	Group-1	ADVANCED CONTROL SYSTEMS
Exam Hours:03		**Exam Marks:100**	

Module -1 Digital Control Systems: Review of Difference equations, Z — transforms and Inverse Z transforms, The Z-transfer function (Pulse transfer function), The Z -Transform Analysis of Sampled data Control Systems, The Z and S - domain relationship, Stability analysis (Jury's Stability Test and Bilinear Transformation)(Text 1, Text 2).

Module -2 State Models& Solution of State equations: State models for Linear Continuous Time and Linear Discrete Time systems, Diagonalization, Solution of State Equations (for both Continuous and Discrete Time systems), Relevant problems (Text1).

Module -3 State Feedback Systems: Concepts of Controllability and Observability (for both Continuous and Discrete Time systems), Pole Placement by State Feedback (for both continuous and discrete Time systems), Observer System (Full order and Reduced order observers for both Continuous and Discrete Time systems),
Relevant problems(Text 1, Text 2).

Module -4 Regulators: Dead beat Control by State Feedback, Optimal control
problems using State Variable approach, State regulator and Output regulator, Concepts of Model Reference Adaptive Control (MRAC)(Text 1, Text 2).

Module -5 Nonlinear Control Systems: Behavior of Nonlinear Systems, Common Physical Nonlinearities, Describing Function Method, Stability Analysis by Describing Function Method, Phase Plane Method, Stability Analysis by Phase Plane Method (Text 1).

Question paper pattern:

- The question paper will have ten questions.
- Each full question consists of 20 marks.
- There will be 2 full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub questions covering all the topics under a module.

The students will have to answer 5 full questions, selecting one full question from each module.

Text Books:

1. I.J. Nagrath & M.Gopal, "Control Systems Engineering", New Age International Publishers, Fifth edition, 2007.
2. K. Ogata, "Discrete Time Control Systems", 2nd edition, PHI, 2009.

Reference Books:

1. K. Ogata, "Modern Control Engineering", 5thEdition, PHI, 2010.
2. 2. M. Gopal ,—Modern Control System Theory", New Age International, 2012.
3. M. Gopal, "Digital Control and State Variable methods", 4th edition, Tata McGraw Hill, 2012.
4. A. Nagoorkani, —Advanced Control Theory‖, RBA publications, 2006.

Visvesvaraya Technological University, Belagavi.

PhD Coursework Courses – 2018 (Electronics and Communication Engineering)

As per 2017 Regulation

01	16ECS23	Group-2	WIRELESS COMMUNICATION

Exam Hours:03 | **Exam Marks:100**

Module -1 The Wireless channel: Physical modeling for wireless channels, Input/output model of wireless channels, Time and frequency response, Statistical models. (Text 1)..

Module -2 Point-to-Point Communication, Detection diversity and channel uncertainty: Detection in Rayleigh fading channels, Time diversity, Antenna diversity, Frequency diversity, Impact of the channel uncertainty. (Text 1).

Module -3 Diversity: Introduction Micro-diversity, Micro-diversity and Simulcast combination of signals, Error probability in fading channels with diversity reception, Transmit diversity. (Chap. 13 of Text2).

Module -4 Capacity of wireless channel: AWGN channel capacity, Resources of AWGN channel, Linear time invariant Gaussian channel, Capacity of fading channels. (Text 1).

Module -5 MIMO Systems: Introduction, Space diversity and system based on space diversity, Smart antenna systems and MIMO, MIMO based system architecture; MIMO exploits multipath, Space time processing, Antenna considerations for MIMO. MIMO channel modeling, MIMO channel measurements, MIMO channel capacity, CDD, Space time coding, advantages and applications of MIMO, MIMO application in 3G.(Chap. 15 of Text 3).

Question paper pattern:

- The question paper will have ten questions.
- Each full question consists of 20 marks.
- There will be 2 full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub questions covering all the topics under a module.

The students will have to answer 5 full questions, selecting one full question from each module.

Reference Book:

1.Ke-Lin Du, ad M.N.S. Swamy, "Wireless communication systems-From RF subsystems to 4G enabling Technologies", Cambridge.

Text Books:

1. David Tse, P. Vishwanath, “Fundamentals of Wireless Communication”, Cambridge University press, 2006.
2. Andreas F.Molisch “Wireless Communications” 2nd Edition John Wiley & Sons.
3. Upena Dalal, “Wireless communication”, Oxford, 2009.

Visvesvaraya Technological University, Belagavi.
PhD Coursework Courses – 2018 (Electronics and Communication Engineering)
As per 2017 Regulation

02	16ECS422	Group-2	Advances in Image Processing
Exam Hours:03		**Exam Marks:100**	

Module -1 The image, its representations and properties: Image representations a few concepts, Image digitization, Digital image properties, Color images.

Module -2 Image Pre-processing: Pixel brightness transformations, geometric transformations, local pre-processing.

Module -3 Segmentation: Thresholding; Edge-based segmentation – Edge image thresholding, Edge relaxation, Border tracing, Hough transforms; Region – based segmentation – Region merging, Region splitting, Splitting and merging, Watershed segmentation, Region growing post-processing.

Module -4 Shape representation and description: Region identification; Contour-based shape representation and description – Chain codes, Simple geometric border representation, Fourier transforms of boundaries, Boundary description using segment sequences, B-spline representation; Region-based shape representation and description – Simple scalar region descriptors, Moments, Convex hull.

Module -5 Mathematical Morphology: Basic morphological concepts, Four morphological principles, Binary dilation and erosion, Skeletons and object marking, Morphological segmentations and watersheds.

Question paper pattern:

- The question paper will have ten questions.
- Each full question consists of 20 marks.
- There will be 2 full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub questions covering all the topics under a module.

The students will have to answer 5 full questions, selecting one full question from each module.

Reference Books:

1. Geoff Doughertry, Digital Image Processing for Medical Applications, Cambridge university Press, 2010
2. S.Jayaraman, S Esakkirajan, T.Veerakumar, Digital Image Processing, Tata McGraw Hill, 2011

Text Book:

1. Milan Sonka, Vaclav Hlavac, Roger Boyle, “Image Processing, Analysis, and Machine Vision”, Cengage Learning, 2013, ISBN: 978-81-315-1883-0.

Visvesvaraya Technological University, Belagavi.

PhD Coursework Courses – 2018 (Electronics and Communication Engineering)

As per 2017 Regulation

03	16ESP22	Group-2	DSP System Design
Exam Hours:03		**Exam Marks:100**	

Module -1 Introduction t o popular DSP CPU Architecture –CPU Data Paths and Control-Timers-Internal Data/Program Memory-External Memory Interface-Programming –Instruction set and Addressing Modes-Code Composer Studio-Code Generation Tools –Code Composer Studio Debugtools –Simulator (Text 1)

Module -2 Sharc Digital Signal Processor- A popular DSP from Analog Devices - Sharc/ Tiger Sharc/ Blackfin (one of them) - Architecture – IOP Registers - Peripherals - Synchronous Serial Port Interrupts - Internal/External/Multiprocessor Memory Space - Multiprocessing - Host Interface - Link Ports. (Text 2)

Module -3 Digital Signal Processing Applications-FIR and IIR Digital Filter Design, Filter Design Programs using MATLAB- Fourier Transform: DFT, FFT programs using MATLAB (Text 1)

Module -4 Real Time Implementation –Implementation of Real Time Digital Filters using DSP-Implementation of FFT Applications using DSP – DTMF Tone Generation and Detection (Text 1)

Module -5 Current trends- Current trend in Digital Signal Processor or DSP Controller- Architecture and their applications. (Text 1)

Question paper pattern:

- The question paper will have ten questions.
- Each full question consists of 20 marks.
- There will be 2 full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub questions covering all the topics under a module.

The students will have to answer 5 full questions, selecting one full question from each module.

Text Books:

1) Rulf Chassaing, “Digital Signal Processing and Application with C6713 and C6416 DSK”, Wiley-Interscience Publication

2) T.J. TerrelandLik- Kwan Shark, “Digital Signal Processing- A Student Guide‖, 1st Edition; Macmillan Press Ltd.

Reference Books:

1) David. J Defatta. J,Lucas Joseph.G & Hodkiss William S, “Digital Signal Processing: A System Design Approach‖,1st Edition, John Wiley.

2) Steven K Smith, Newnes, “Digital Signal Processing-A Practical Guide for Engineers and Scientists”, Elsevier Science.

3) Rulph Chassaing, “DSP Applications using 'C' and the TMS320C6X DSK”, 1stEdition.

4) Andrew Bateman, Warren Yates, “Digital Signal Processing Design”, 1st Edition

5) Naim Dahnoun, “Digital Signal Processing Implementation using the TMS320C6000 DSP Platform”, 1st Edition.

Visvesvaraya Technological University, Belagavi.

PhD Coursework Courses – 2018 (Electronics and Communication Engineering)

As per 2017 Regulation

04	16ESP23	Group-2	Digital Signal Copmression
Exam Hours:03		**Exam Marks:100**	

Module -1 Introduction: Compression techniques, Modeling & coding, Distortion criteria, Differential Entropy, Rate Distortion Theory, Vector Spaces, Information theory, Models for sources, Coding–uniquely decodable codes, Prefix codes, Kraft McMillan Inequality. Quantization: Quantization problem, Uniform Quantizer, Adaptive Quantization, Non-uniform Quantization; Entropy coded Quantization, Vector Quantization, LBG algorithm, Tree structured VQ, Structured VQ, Variations of VQ–Gain shape VQ, Mean removed VQ, Classified VQ, Multistage VQ, Adaptive VQ, Trellis coded quantization.

Module -2 Differential Encoding: Basic algorithm, Prediction in DPCM, Adaptive DPCM, Delta Modulation, Speech coding–G.726, Image coding. Transform Coding: Transforms–KLT, DCT, DST, DWHT; Quantization and coding of transform coefficients, Application to Image compression–JPEG, Application to audio compression

Module -3 Sub-band Coding: Filters, Sub-band coding algorithm, Design of filter banks, Perfect reconstruction using two channel filter banks, M-band QMF filter banks, Poly-phase decomposition, Bit allocation, Speech coding– G.722, Audio coding–MPEG audio, Image compression.

Module -4 Wavelet Based Compression: Wavelets, Multi resolution analysis & scaling function, Implementation using filters, Image compression–EZW, SPIHT, JPEG 2000. Analysis/Synthesis Schemes: Speech compression–LPC-10, CELP, MELP, Image Compression–Fractal compression. Video Compression: Motion compensation, Video signal representation, Algorithms for video conferencing & video phones–H.261, H.263, Asymmetric applications–MPEG 1, MPEG 2, MPEG 4, MPEG 7, Packet video.

Module -5 Loss less Coding: Huffman coding, Adaptive Huffman coding, Golomb codes, Rice codes, Tunstall codes, Applications of Huffman coding, Arithmetic coding, Algorithm implementation, Applications of Arithmetic coding, Dictionary techniques–LZ77, LZ78, Applications of LZ78– JBIG, JBIG2, Predictive coding– Prediction with partial match, Burrows Wheeler Transform, Applications– CALIC, JPEG-LS, Facsimile coding– T.4, T.6

Question paper pattern:

- The question paper will have ten questions.
- Each full question consists of 20 marks.
- There will be 2 full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub questions covering all the topics under a module.

The students will have to answer 5 full questions, selecting one full question from each module.

Text Book:

1) K.Sayood, “Introduction to Data Compression”, Harcourt India Pvt. Ltd. & Morgan Kaufmann Publishers, 1996.

Reference Books:

1) N.Jayantand P.Noll, “Digital Coding of Waveforms: Principles and Applications to Speech and Video”, Prentice Hall, USA, 1984.

2) D.Salomon, “Data Compression: The Complete Reference”, Springer, 2000.

3) Z.Liand M.S.Drew, “Fundamentals of Multimedia”, Pearson Education (Asia) Pvt. Ltd., 2004.

Visvesvaraya Technological University, Belagavi.
PhD Coursework Courses – 2018 (Electronics and Communication Engineering)
As per 2017 Regulation

05	16EVE12	Group-2	DIGITAL VLSI DESIGN
Exam Hours:03		**Exam Marks:100**	

Module -1 MOS Transistor: The Metal Oxide Semiconductor (MOS) Structure, The MOS System under External Bias, Structure and Operation of MOS Transistor, MOSFET Current-Voltage Characteristics, MOSFET Scaling and Small-Geometry Effects.
MOS Inverters-Static Characteristics: Introduction, Resistive-Load Inverter, Inverters with n_Type MOSFET Load.

Module -2 MOS Inverters-Static Characteristics: CMOS Inverter.
MOS Inverters: Switching Characteristics and Interconnect Effects: Introduction, Delay-Time
Definition, Calculation of Delay Times, Inverter Design with Delay Constraints, Esimation of Interconnect Parasitics, Calculation of Interconnect Delay, Switching Power Dissipation of CMOS Inverters.

Module -3 Semiconductor Memories: Introduction, Dynamic Random Access Memory (DRAM), Static Random Access Memory (SRAM), Nonvolatile Memory, Flash Memory, Ferroelectric Random Access Memory (FRAM).

Module -4 Dynamic Logic Circuits: Introduction, Basic Principles of Pass Transistor Circuits, Voltage Bootstrapping, Synchronous Dynamic Circuit Techniques, Dynamic CMOS Circuit Techniques, High Performance Dynamic CMOS Circuits.
BiCMOS Logic Circuits: Introduction, Bipolar Junction Transistor (BJT): Structure and Operation, DynamicBehavior of BJTs, Basic BiCMOS Circuits: Static Behavior, Switching Delay in BiCMOS Logic Circuits, BiCMOS Applications.

Module -5 Chip Input and Output (I/O) Circuits: Introduction, ESD Protection, Input Circuits, Output Circuits and L(di/dt) Noise, On-Chip Clock Generation and Distribution, Latch-Up and Its Prevention.
Design for Manufacturability: Introduction, Process Variations, Basic Concepts and Definitions, Design of Experiments and Performance Modeling.

Question paper pattern:

- The question paper will have ten questions.
- Each full question consists of 20 marks.
- There will be 2 full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub questions covering all the topics under a module.

The students will have to answer 5 full questions, selecting one full question from each module.

Text Books:
Sung Mo Kang & Yosuf Leblebici, “CMOS Digital Integrated Circuits: Analysis and Design”, Tata McGraw-Hill, Third Edition.

Reference Books:
1. Neil Weste and K. Eshragian, “Principles of CMOS VLSI Design: A System Perspective”, Second Edition, Pearson Education (Asia) Pvt. Ltd. 2000.
2. Wayne, Wolf, “Modern VLSI Design: System on Silicon” Prentice Hall PTR/Pearson Education, Second Edition, 1998.
3. Douglas A Pucknell & Kamran Eshragian , “Basic VLSI Design” PHI 3rd Edition (original Edition – 1994).

Visvesvaraya Technological University, Belagavi.
PhD Coursework Courses – 2018 (Electronics and Communication Engineering)
As per 2017 Regulation

06	16ELD424	Group-2	Reconfigurable Computing
Exam Hours:03		**Exam Marks:100**	

Module -1 Introduction : History, Reconfigurable Vs Processor based system, RC Architecture. **Reconfigurable Logic Devices**: Field Programmable Gate Array, Coarse Grained Reconfigurable Arrays.
Reconfigurable Computing System: Parallel Processing on Reconfigurable Computers, A survey of Reconfigurable Computing System.

Module -2 Languages and Compilation: Design Cycle, Languages, HDL, High Level Compilation, Low level Design flow, Debugging Reconfigurable Computing Applications.

Module -3 Implementation: Integration, FPGA Design flow, Logic Synthesis.
High Level Synthesis for Reconfigurable Devices: Modelling, Temporal Partitioning Algorithms.

Module -4 Partial Reconfiguration Design: Partial Reconfiguration Design, Bitstream Manipulation with JBits, The modular Design flow, The Early Access Design Flow, Creating Partially Reconfigurable Designs, Partial Reconfiguration using Hansel-C Designs, Platform Design.

Module -5 Signal Processing Applications: Reconfigurable computing for DSP, DSP application building blocks, Examples: Beamforming, Software Radio, Image and video processing, Local Neighbourhood functions, Convolution. (Text 1).
System on a Programmable Chip: Introduction to SoPC, Adaptive Multiprocessing on Chip. (Text 2)**.**

Question paper pattern:

- The question paper will have ten questions.
- Each full question consists of 20 marks.
- There will be 2 full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub questions covering all the topics under a module.

The students will have to answer 5 full questions, selecting one full question from each module.

Text Books:

1. M. Gokhale and P. Graham, ―Reconfigurable Computing: Accelerating Computation with Field-Programmable Gate Arrays‖, Springer, 2005.
2. C. Bobda, ―Introduction to Reconfigurable Computing: Architectures, Algorithms and Applications‖, Springer, 2007.

Reference Books:

1. D. Pellerin and S. Thibault, ―Practical FPGA Programming in C‖, Prentice-Hall, 2005.
2. W. Wolf, ―FPGA Based System Design‖, Prentice-Hall, 2004.
3. R. Cofer and B. Harding, ―Rapid System Prototyping with FPGAs: Accelerating the Design Process‖, Newnes, 2005.

Visvesvaraya Technological University, Belagavi.

PhD Coursework Courses – 2018 (Electronics and Communication Engineering)

As per 2017 Regulation

07	16EVE152	Group-2	NANOELECTRONICS
Exam Hours:03		**Exam Marks:100**	

Module -1 Introduction: Overview of nanoscience and engineering. Development milestones in microfabrication and electronic industry. Moores' law and continued miniaturization, Classification of Nanostructures, Electronic properties of atoms and solids: Isolated atom, Bonding between atoms, Giant molecular solids, Free electron models and energy bands, crystalline solids, Periodicity of crystal lattices, Electronic conduction, effects of nanometer length scale, Fabrication methods: Top down processes, Bottom up processes methods for templating the growth of nanomaterials, ordering of nanosystems (Text 1).

Module -2Characterization: Classification, Microscopic techniques, Field ion microscopy, scanning probe techniques, diffraction techniques: bulk and surface diffraction techniques (Text1).

Module -3 Characterization: spectroscopy techniques: photon, radiofrequency, electron, surface analysis and dept profiling: electron, mass, Ion beam, Reflectrometry, Techniques for property measurement: mechanical, electron, magnetic, thermal properties.

Inorganic semiconductor nanostructures: overview of semiconductor physics. Quantum confinement in semiconductor nanostructures: quantum wells, quantum wires, quantum dots, super-lattices, band offsets, electronic density of states (Text1).

Module -4 Fabrication techniques: requirements of ideal semiconductor, epitaxial growth of quantum wells, lithography and etching, cleaved-edge over growth, growth of vicinal substrates, strain induced dots and wires, electrostatically induced dots and wires, Quantum well width fluctuations, thermally annealed quantum wells, semiconductor nanocrystals, collidal quantum dots, self assembly techniques.

Physical processes: modulation doping, quantum hall effect, resonant tunneling, charging effects, ballistic carrier transport, Inter band absorption, intraband absorption, Light emission processes, phonon bottleneck, quantum confined stark effect, nonlinear effects, coherence and dephasing, characterization of semiconductor nanostructures: optical electrical and structural (Text1).

Module -5 Methods of measuring properties: Atomic, crystollography, microscopy, spectroscopy (Text 2).

Applications: Injection lasers, quantum cascade lasers, singlephoton sources, biological tagging, optical memories, coulomb blockade devices, photonic structures, QWIP's, NEMS, MEMS (Text 1).

Question paper pattern:

- The question paper will have ten questions.
- Each full question consists of 20 marks.
- There will be 2 full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub questions covering all the topics under a module.

The students will have to answer 5 full questions, selecting one full question from each module.

Text Books:

1. Ed Robert Kelsall, Ian Hamley, Mark Geoghegan, ―Nanoscale Science and Technology‖, John Wiley, 2007.
2. Charles P Poole, Jr, Frank J Owens, ―Introduction to Nanotechnology‖, John Wiley, Copyright 2006, Reprint 2011.

Reference Book:

1.Ed William A Goddard III, Donald W Brenner, Sergey E. Lyshevski, Gerald J Iafrate, ―Hand Book of Nanoscience Engineering and Technology‖, CRC press, 2003.

Visvesvaraya Technological University, Belagavi.

PhD Coursework Courses – 2018 (Electronics and Communication Engineering)

As per 2017 Regulation

08	16EIE23	Group-2	Process Control Instrumentation
Exam Hours:03		**Exam Marks:100**	

Module -1 UTOMATION – NEED AND BENEFIT: Instrumentation subsystems- Structure, Signal Interface Standards, Input data reliability enhancement, Isolation and Protection, human interface subsystems - Operation panel, Construction, control subsystems – Structure, interfacing, automation strategies-
Basic and advanced strategies.

Module -2 DATA ACQUISITION AND CONTROL UNIT: Hardware and Software- Basic modules, functional modules, DACU capacity expansion, system cables, Integrated assemblies, DACU construction, Data exchange on bus, Software structure, application programming, Programmable control subsystems, Types of automation systems.

Module -3 DATA COMMUNICATION AND NETWORKING: Communication network, signal and data transmission, Data communication protocol, Inter process communication, cyber security, Safe and redundant network

Module -4 FIELDBUS TECHNOLOGY & SAFETY SYSTEMS: Centralized, remote- input-output, Field bus- input-output, communication, device integration, Other networks. Safety systems introduction, Process and Machine safety management.

Module -5 MANAGEMENT AND INFORMATION TECHNOLOGY IN INDUSTRIAL PROCESSES: Introduction, Classification of industrial processes, Manufacturing and utility processes, industrial robotics, operation technology and IT, before and convergence, ISA 95 standard, new developments.

Question paper pattern:

- The question paper will have ten questions.
- Each full question consists of 20 marks.
- There will be 2 full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub questions covering all the topics under a module.

The students will have to answer 5 full questions, selecting one full question from each module.

Text Book:

K L S Sharma, Overview of Industrial Process Automation, 2nd edition, ELSEVIER, 2016.

Reference Books:

1. M. Chidambaram, Computer control of processes, Narosa publishing, 2002.
2. Krishna Kant, Computer Based Industrial control, 2nd Edition, Prentice Hall of India,2010.
3. B G Liptak, Instrument Engineers Handbook- (Vol 1 & 2),Chilton Book Company.

Visvesvaraya Technological University, Belagavi.

PhD Coursework Courses – 2018 (Electronics and Communication Engineering)

As per 2017 Regulation

01	16ECS22	Group-3	ERROR CONTROL CODING

Exam Hours:03 **Exam Marks:100**

Module -1 Information theory: Introduction, Entropy, Source coding theorem, discrete memoryless channel, Mutual Information, Channel Capacity Channel coding theorem.(Chap. 5 of Text 1)

Introduction to algebra: Groups, Fields, binary field arithmetic, Construction of Galois Fields GF (2m) and its properties, (Only statements of theorems without proof) Computation using Galois filed GF (2m) arithmetic, Vector spaces and Matrices. (Chap. 2 of Text 2).

Module -2 Linear block codes: Generator and parity check matrices, Encoding circuits, Syndrome and error detection, Minimum distance considerations, Error detecting and error correcting capabilities, Standard array and syndrome decoding, Single Parity Check Codes(SPC),Repetition codes, Self dual codes, Hamming codes, Reed-Muller codes. Product codes and Interleaved codes. (Chap. 3 of Text 2)

Module -3 Cyclic codes: Introduction, Generator and parity check polynomials, Encoding of cyclic codes, Syndrome computing and error detection, Decoding of cyclic codes, Error trapping Decoding, Cyclic hamming codes, Shortened cyclic codes.(Chap. 4 of Text2)

Module -4 BCH codes: Binary primitive BCH codes, Decoding procedures, Implementation of Galois field arithmetic, Implementation of error correction. (Chap. 6 of Text 2)

Reed -Solomon codes. (Chap. 7 of Text 2)

Majority Logic decodable codes: One -step majority logic decoding, One-step majority logic decodable codes, Two-step majority logic, decoding, Multiple-step majority logic. (Chap. 8 of Text 2)

Module -5 Convolution codes: Convolutional Encoding, Convolutional Encoder Representation, Formulation of the Convolutional Decoding Problem, Properties of Convolutional Codes: Distance property of convolutional codes, Systematic and Nonsystematic Convolutional Codes, Performance Bounds for Convolutional Codes, Coding Gain. Other Convolutional Decoding Algorithms: Sequential Decoding, Feedback Decoding.(Chap. 7 of Text 3)

Question paper pattern:

- The question paper will have ten questions.
- Each full question consists of 20 marks.
- There will be 2 full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub questions covering all the topics under a module.

The students will have to answer 5 full questions, selecting one full question from each module.

Reference Books:

1. Blahut. R. E, "Theory and practice of error control codes", Addison Wesley, 1984.
2. Salvatore Gravano, “Introduction to Error control coding”, Oxford university press,2007.

Text Books:

1. Simon Haykin, ”Digital Communication systems”, First edition, Wiley India Private. Ltd, 2014. ISBN 978-81-265-4231-4
2. Shu Lin and Daniel J. Costello. Jr, "Error control coding", Pearson, Prentice Hall, 2nd edition, 2004.
3. Bernard Sklar, ”Digital Communications - Fundamentals and Applications”, 2nd Edition Pearson Education (Asia) Ptv. Ltd, 2001.

Visvesvaraya Technological University, Belagavi.

PhD Coursework Courses – 2018 (Electronics and Communication Engineering)

As per 2017 Regulation

02	16ESP254	Group-3	CHANNEL CODING
Exam Hours:03		**Exam Marks:100**	

Module -1 Introduction to Algebra: Groups, Fields, Binary Field Arithmetic, Construction of Galois Field GF (2m) and its basic properties, Computation using Galois Field GF (2m) Arithmetic, Vector spaces and Matrices. Linear Block Codes: Generator and Parity check Matrices, Encoding circuits, Syndrome and Error Detection, Minimum Distance Considerations, Error detecting and Error correcting capabilities, Standard array and Syndrome decoding, Decoding circuits, Reed–Muller codes, Product codes and Inter leaved codes.

Module -2 Cyclic Codes: Introduction, Generator and Parity check Polynomials, Encoding of cyclic codes, Generator matrix for Cyclic codes, Syndrome computation and Error detection, Meggitt decoder, Error trapping decoding, Cyclic Hamming codes, The (23, 12) Golay code, Shortened cyclic codes.

Module -3 BCH Codes: 4. Binary primitive BCH codes, Decoding procedures, Implementation of Galois field Arithmetic, Implementation of Error correction. Non–binary BCH codes: q– ary Linear Block Codes, Primitive BCH codes over GF (q), Reed–Solomon Codes, Decoding of Non –Binary BCH and RS codes: The Berlekamp-Massey Algorithm.

Module -4 Majority Logic Decodable Codes: One–Step Majority logic decoding, one–step Majority logic decodable Codes, Multiple–step Majority logic decoding.

Convolutional Codes: Encoding of Convolutional codes, Structural properties, Distance properties, Viterbi Decoding Algorithm for decoding, Soft – output Viterbi Algorithm, Stack and Fano sequential decoding Algorithms, Majority logic decoding.

Module -5 Concatenated Codes & Turbo Codes: Single level Concatenated codes, Multilevel Concatenated codes, Soft decision Multi stage decoding, Concatenated coding schemes with Convolutional Inner codes, Introduction to Turbo coding and their distance properties, Design of Turbo codes. Burst–Error–Correcting Codes: Burst and Random error correcting codes, Concept of Inter–leaving, cyclic codes for Burst Error correction–Fire codes, Convolutional codes for Burst Error correction.

Question paper pattern:

- The question paper will have ten questions.
- Each full question consists of 20 marks.
- There will be 2 full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub questions covering all the topics under a module.

The students will have to answer 5 full questions, selecting one full question from each module.

Text Book:

1. Shu Lin &Daniel J. Costello, Jr. “Error Control Coding”, Pearson/ Prentice Hall, Second Edition, 2004.

Reference Book:

1. Blahut, R.E. “Theory and Practice of Error Control Codes”, Addison Wesley, 1984.

Visvesvaraya Technological University, Belagavi.

PhD Coursework Courses – 2018 (Electronics and Communication Engineering)

As per 2017 Regulation

03	16ESP21	Group-3	Image Processing and Machine Vision

Exam Hours:03 **Exam Marks:100**

Module -1 The image mathematical and physical background: Linearity, The Dirac distribution and convolution, Linear integral transforms, Images as linear systems,

Introduction to linear integral transforms: 2D Fourier transform, Sampling and the Shannon constraint, Discrete cosine transform, Wavelet transform, Eigen-analysis, Singular value decomposition

Principal component analysis, Other orthogonal image transforms,

Module -2 Image pre-processing: Scale in image processing, Canny edge detection, Parametric edge models, Edges in multi-spectral images, Pre-processing in frequency domain, Line detection, Corner detection, Maximally stable extremal regions, Image restoration: Degradations that are easy to restore, Inverse filtration, Wiener filtration

Module -3 Image segmentation: Threshold detection methods, Optimal thresholding, Multi-spectral thresholding, Edge-based segmentation, Edge image thresholding, Edge relaxation, Border tracing, Border detection as graph searching, Border detection as dynamic programming, Hough transforms, Border detection using border location information, Region construction from borders, Region-based segmentation, Region merging, Region splitting, Splitting and merging, Watershed segmentation, Region growing post-processing. Matching : Matching criteria, Control strategies of matching Evaluation issues in segmentation: Supervised evaluation, Unsupervised evaluation

Module -4 Advanced segmentation: Mean Shift Segmentation, Active contour models-snakes, Traditional snakes and balloons, Extensions, Gradient vector flow snakes, Geometric deformable models-level sets and geodesic active contours, Fuzzy Connectivity, Contour-based shape representation and description: Chain codes, Simple geometric border representation, Fourier transforms of boundaries, Boundary description using segment sequences, B-spline representation, Other contour-based shape description approaches, Shape invariants.

Module -5 Knowledge representation: Statistical pattern recognition, Classification principles, Classifier setting, Classifier learning, Support Vector Machines, Cluster analysis Neural nets: Feed-forward networks, Unsupervised learning, Hopfield neural nets Optimization techniques in recognition: Genetic algorithms, Simulated annealing Fuzzy systems: Fuzzy sets and fuzzy membership functions, Fuzzy set operators, Fuzzy reasoning, Fuzzy system design and training

Question paper pattern:

- The question paper will have ten questions.
- Each full question consists of 20 marks.
- There will be 2 full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub questions covering all the topics under a module.

The students will have to answer 5 full questions, selecting one full question from each module.

Text Book:

Milan Sonka, Vaclav Hlavac , Roger Boyle “Image Processing, Analysis, and Machine Vision”, Cengage Learning, 2014 or 3rd Edition, 2008ISBN:049508252X

Reference Books:

1) Scott.E.Umbaugh, “Computer Vision and Image Processing”, Prentice Hall, 1997.
2) A. K.Jain, “Fundamentals of Digital Image Processing”, Pearson, 2004.
3) S.Jayaraman, S.Esakkirajan, T. Veerakumar, “Digital Image Processing”, Tata McGraw Hill, 2004.

Visvesvaraya Technological University, Belagavi.

PhD Coursework Courses – 2018 (Electronics and Communication Engineering)

As per 2017 Regulation

04	16ESP421	Group-3	Array Signal Processing
Exam Hours:03		**Exam Marks:100**	

Module -1 Spatial Signals: Signals in space and time, Spatial Frequency Vs Temporal Frequency, Review of Co-ordinate Systems, Maxwell's Equation, Wave Equation. Solution to Wave equation in Cartesian Co-ordinate system –Wave number vector, Slowness vector.

Module -2 Wave number-Frequency Space Spatial Sampling: Spatial Sampling Theorem-Nyquist Criteria, Aliasing in Spatial frequency domain, Spatial sampling of multidimensional signals.

Module -3 Sensor Arrays: Linear Arrays, Planar Arrays, Frequency – Wave number Response and Beam pattern, Array manifold vector, Conventional Beam former, Narrowband beam former.

Module -4 Uniform Linear Arrays: Beam pattern in θ, u and ψ -space, Uniformly Weighted Linear Arrays. Beam Pattern Parameters: Half Power Beam Width, Distance to First Null, Location of side lobes and Rate of Decrease, Grating Lobes, Array Steering.

Module -5 Array Design Methods: Visible region, Duality between Time - Domain and Space -Domain Signal Processing, Schelkunoff's Zero Placement Method, Fourier Series Method with windowing, Woodward -Lawson Frequency-Sampling Design. Non parametric method -Beam forming, Delay and sum Method, Capons Method.

Question paper pattern:

- The question paper will have ten questions.
- Each full question consists of 20 marks.
- There will be 2 full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub questions covering all the topics under a module.

The students will have to answer 5 full questions, selecting one full question from each module.

Text Book:

1. Harry L. Van Trees ―Optimum Array Processing Part IV of Detection, Estimation, and Modulation Theory‖ John Wiley & Sons, 2002, ISBN: 9780471093909.

Reference Books:

1. Don H. Johnson Dan E. Dugeon, ―Array Signal Processing: Concepts and Techniques, Prentice Hall Signal Processing Series, 1st Edition ,ISBN-13: 978-0130485137.

2. Petre Stoica and Randolph L. Moses ―Spectral Analysis of Signals, Prentice Hall, 2005, ISBN: 0-13-113956-8.

3. Sophocles J. Orfanidis, ―Electromagnetic Waves and Antennas, ECE Department Rutgers University, 94 Brett Road Piscataway, NJ 08854- 8058. http://www.ece.rutgers.edu/~orfanidi/ewa/

Visvesvaraya Technological University, Belagavi.
PhD Coursework Courses – 2018 (Electronics and Communication Engineering)
As per 2017 Regulation

05	16EVE151	Group-3	DIGITAL SYSTEM DESIGN USING VERILOG
Exam Hours:03		**Exam Marks:100**	
Module -1Introduction and Methodology: Digital Systems and Embedded Systems, Binary representation and Circuit Elements, Real-World Circuits, Models, Design Methodology.			
Module -2. **Number Basics**: Unsigned and Signed Integers, Fixed and Floating-point Numbers. **Sequential Basics**: Storage elements, Counters, Sequential Data paths and Control, Clocked Synchronous Timing Methodology.			
Module -3Memories: Concepts, Memory Types, Error Detection and Correction. **Implementation Fabrics**: ICs, PLDs, Packaging and Circuit Boards, Interconnection and Signal Integrity.			
Module -4 Processor Basics: Embedded Computer Organization, Instruction and Data, Interfacing with memory. **I/O interfacing**: I/O devices, I/O controllers, Parallel Buses, Serial Transmission, I/O software.			
Module -5 Accelerators: Concepts, case study, Verification of accelerators. **Design Methodology**: Design flow, Design optimization, Design for test.			
Question paper pattern: • The question paper will have ten questions. • Each full question consists of 20 marks. • There will be 2 full questions (with a maximum of four sub questions) from each module. • Each full question will have sub questions covering all the topics under a module. The students will have to answer 5 full questions, selecting one full question from each module.			
Text Book: **1.** Peter J. Ashenden, "Digital Design: An Embedded Systems Approach Using VERILOG", Elesvier, 2010. **Reference Book:** 1. Verilog HDL: A Guide to Digital Design and Synthesis, Second Edition by Samir Palnitkar.			

Visvesvaraya Technological University, Belagavi.

PhD Coursework Courses – 2018 (Electronics and Communication Engineering)

As per 2017 Regulation

06	16ELD154	Group-3	ADVANCED COMPUTER ARCHITECTURE

Exam Hours:03 **Exam Marks:100**

Module -1 Parallel Computer Models: Classification of parallel computers, Multiprocessors and multicomputers, Multivector and SIMD computers. Program and Network Properties, Conditions of parallelism, Data and resource Dependences, Hardware and software parallelism.

Module -2. Program partitioning and scheduling, Grain Size and latency, Program flow mechanisms, Control flow versus data flow, Data flow Architecture, Demand driven mechanisms, Comparisons of flow mechanisms, Principles of Scalable Performance, Performance Metrics and Measures, Parallel Processing Applications, Speedup Performance Laws, Scalability Analysis and Approaches.

Module -3Advanced Processors: Advanced processor technology, Instruction-set Architectures, CISC Scalar Processors, RISC Scalar Processors, Superscalar Processors, VLIW Architectures, Pipelining, Linear pipeline processor, nonlinear pipeline processor, Instruction pipeline design.

Module -4 Mechanisms for instruction pipelining, Dynamic instruction scheduling, Branch Handling techniques, branch prediction, Arithmetic Pipeline Design, Computer arithmetic principles, Static Arithmetic pipeline, Multifunctional arithmetic pipelines.

Module -5 Multithread and Dataflow Architecture: Principles of Multithreading, Scalable and Multithreaded Architecture, Data flow Architecture, Symmetric shared memory architecture, distributed shared memory architecture.

Question paper pattern:

- The question paper will have ten questions.
- Each full question consists of 20 marks.
- There will be 2 full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub questions covering all the topics under a module.

The students will have to answer 5 full questions, selecting one full question from each module.

Text Books:

1. Kai Hwang, “Advanced computer architecture”, TMH. 2007.
2. Kai Hwang and Zu, “Scalable Parallel Computers Architecture”, MGH, 2008.

Reference Books:

1. M.J. Flynn, “Computer Architecture, Pipelined and Parallel Processor Design”, Narosa Publishing, 2002.
2. D.A.Patterson, J.L.Hennessy, “Computer Architecture: A quantitative approach”, Morgan Kauffmann feb, 2002.

Visvesvaraya Technological University, Belagavi.
PhD Coursework Courses – 2018 (Electronics and Communication Engineering)
As per 2017 Regulation

07	16EVE251	Group-3	System Verilog
Exam Hours:03		**Exam Marks:100**	

Module -1 Verification Guidelines:
The verification process, basic test bench functionality, directed testing, methodology basics, constrained random stimulus, randomization, functional coverage, test bench components.

Data Types:
Built in Data types, fixed and dynamic arrays, Queues, associative arrays, linked lists, array methods, choosing a storage type, creating new types with type def, creating user defined structures, type conversion, Enumerated types, constants and strings, Expression width.

Module -2. Procedural Statements and Routines:
Procedural statements, Tasks, Functions and void functions, Task and function overview, Routine arguments, returning from a routine, Local data storage, time values.

Converting the test bench and design:
Separating the test bench and design, The interface construct, Stimulus timing, Interface driving and sampling, System Verilog assertions.

Module -3Randomization:
Introduction, Randomization in System Verilog, Constraint details, Solution probabilities, Valid constraints, In-line constraints, Random number functions, Common randomization problems, Iterative and array constraints, Random control.

Module -4 Threads and Interprocess Communication:
Working with threads, Disabling threads, Interprocess communication, Events, semaphores, Mailboxes, Building a test bench with threads and Interprocess Communication.

Module -5 Functional Coverage:
Coverage types, Coverage strategies, Simple coverage example, Anatomy of Cover group and Triggering a Cover group, Data sampling, Cross coverage, Generic Cover groups, Coverage options, Analyzing coverage data, measuring coverage statistics during simulation.

Question paper pattern:

- The question paper will have ten questions.
- Each full question consists of 20 marks.
- There will be 2 full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub questions covering all the topics under a module.

The students will have to answer 5 full questions, selecting one full question from each module.

Text Book:

1. Chris Spear, _System Verilog for Verification – A guide to learning the Test bench language features‘, Springer Publications, 2nd Edition, 2010.

Reference Book:

1. Stuart Sutherland, Simon Davidmann, Peter Flake, ―System Verilog for Design- A guide to using system verilog for Hardware design and modelingl, Springer Pulications, 2nd Edition, 2006.

Visvesvaraya Technological University, Belagavi.

PhD Coursework Courses – 2018 (Electronics and Communication Engineering)

As per 2017 Regulation

08	16ELD253	Group-3	Micro Electro Mechanical Systems
Exam Hours:03		**Exam Marks:100**	

Module -1 Overview of MEMS and Microsystems: MEMS and Microsystem, Typical MEMS and Microsystems Products, Evolution of Microfabrication, Microsystems and Microelectronics, Multidisciplinary Nature of Microsystems, Miniaturization. Applications and Markets.

Module -2. **Working Principles of Microsystems:** Introduction, Microsensors, Microactuation, MEMS with Microactuators, Microaccelerometers, Microfluidics.

Engineering Science for Microsystems Design and

Fabrication: Introduction, Atomic Structure of Matters, Ions and Ionization, Molecular Theory of Matter and Inter-molecular Forces, Doping of emiconductors, The Diffusion Process, Plasma Physics, Electrochemistry.

Module -3Engineering Mechanics for Microsystems Design: Introduction, Static Bending of Thin Plates, Mechanical Vibration, Thermomechanics, Fracture Mechanics, Thin Film Mechanics, Overview on Finite Element Stress Analysis.

Module -4 Scaling Laws in Miniaturization: Introduction, Scaling in Geometry, Scaling in Rigid-Body Dynamics, Scaling in Electrostatic Forces, Scaling of lectromagnetic Forces, Scaling in Electricity, Scaling in Fluid Mechanics, Scaling in Heat ransfer.

Module -5 Overview of Micromanufacturing: Introduction, Bulk Micromanufacturing, Surface Micromachining, The LIGA Process, Summary on Micromanufacturing.

Microsystem Design: Introduction, Design Considerations, Process Design, Mechanical Design, Using Finite Element Method.

Question paper pattern:

- The question paper will have ten questions.
- Each full question consists of 20 marks.
- There will be 2 full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub questions covering all the topics under a module.

The students will have to answer 5 full questions, selecting one full question from each module.

Text Book:

Tai-Ran Hsu, MEMS and Micro systems: Design, Manufacture and Nanoscale Engineering, 2nd Ed, Wiley.

Reference Books:

1. Hans H. Gatzen, Volker Saile, Jurg Leuthold, Micro and Nano Fabrication: Tools and Processes, Springer, 2015.
2. Dilip Kumar Bhattacharya, Brajesh Kumar Kaushik, Microelectromechanical Systems (MEMS), Cenage Learning.

Visvesvaraya Technological University, Belagavi.

PhD Coursework Courses – 2018 (Electronics and Communication Engineering)

As per 2017 Regulation

09	16EIE151	Group-3	PLCS AND INDUSTRIAL AUTOMATION
Exam Hours:03		**Exam Marks:100**	

Module -1 Introduction to PLC

Technical Definition , Advantages, Characteristic Functions, Chronological Evolution, Types, Unitary PLC, Modular PLC, SMEEl PLC, Medium PLC, Large PLC, Block Diagram Of PLC, Input / Output Section, Processor Section, Power Supply, Memory, Central Processing Unit, Processor Software / Executive Software, Multitasking, Languages, Ladder Language.

Bit Logic Instructions: Introduction, Input And Output Contact Program, Symbols, Numbering System Of Inputs And Outputs, Program Format, Introduction To Logic, Equivalent Ladder Diagram Of - AND Gate, OR Gate, NOT Gate, XOR Gate, NAND Gate, NOR Gate, Equivalent Ladder Diagram To Demonstrate De Morgan Theorem, Ladder Design.

Module -2. PLC Timers And Counters

Timer And Its Classification, Characteristics Of PLC Timer, Functions In Timer, Resetting – Retentive And Non-Retentive, Classification Of PLC Timer, On Delay, And Off Delay Timers, Timer-On Delay, Timer Off Delay, Retentive And Non-Retentive Timers, Format of a Timer Instruction. PLC Counter, Operation Of PLC Counter, Counter Parameters, Counter Instructions. Overview, Count Up (CTU), Count Down (CTD).

Advanced Instructions

Comparison Instructions, Addressing Data Files, Format Of Logical Address, Addressing Format for Micrologic System, Different Addressing Types. Data Movement Instructions.

Module -3Logical Instructions

Mathematical Instructions and its Features, Special Mathematical Instructions, Scale with Parameters or SCP Instruction. Data Handling Instructions and its Features, Program Flow Control Instructions, Proportional Integral Derivative (PID) Instruction.

PLC I/O Modules And Power Supply

Classification Of I/O, I/O System Overview, Practical I/O System and its mapping, Addressing Local and Expansion I/O, Input-Output Systems, Direct I/O Parallel I/O Systems Serial I/O Systems, Sinking And Sourcing, Sourcing and Sinking in PLC Interfacing, Discrete Input Module, Discrete DC Input Module, Discrete AC Input Module, Rectifier with Filter, Threshold Detection, Isolation, Logic Section, Discrete Output Modules, Advantages and Disadvantages Of Output Modules, Types of Analog Input Module.

Module -4 Industrial Communication

Introduction, Evolution Of Industrial Control Process, Types Of Communication Interface, Types Of Networking Channels, Parallel Communication Interface. Serial Communication Interface, communication mode, Synchronous And Asynchronous Transmissions , Standard Interface RS 232C, RS 422, EIA 485, Comparison, Software Protocol, Industrial Network. Network Topology, Media Access Methods.

Module -5 Industrial Networking

Open System Interconnection (OSI), Network Model, Network Components, Control Network Issues, Advantage of Standardized Industrial Network, Intelligent Devices, Industrial Network Bus Network, Device Bus Network Vs. Process Bus Network, Controller Area Network (CAN), Devicenet, Controlnet, Ethernet Protocol, AS-I Interface, OUNDATION FIEAEBUS, Application of Profibus for Real PLC Communication.

Industrial Automation

Introduction, Utility Of Automation, General Structure of a Automated Process, Examples of Simple Automated Systems, Selection Of PLC.

Question paper pattern:

- The question paper will have ten questions.
- Each full question consists of 20 marks.
- There will be 2 full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub questions covering all the topics under a module.

The students will have to answer 5 full questions, selecting one full question from each module.

Text Book:

1.Madhuchhanda Mitra and Samarjit Sen Gupta, ―Programmable Logic Controllers and Industrial Automation‖, Penram International Publishing (India) Pvt. Ltd., 2007. ISBN: 81-87972-17-3.

Reference Books:

1. Garry Dunning, ―Introduction to Programmable Logic Controllers‖, 2nd Edition, Delmar Thomson Learning, 2001. ISBN: 981-240-625-5.

2. M. Chidambaram, ―Computer Control of Processes‖, CRC Press, 2002. ISBN:0849310105.

Visvesvaraya Technological University, Belagavi.

PhD Coursework Courses – 2018 (Electronics and Communication Engineering)

As per 2017 Regulation

01	16ECS12	Group-4	ANTENNA THEORY AND DESIGN
Exam Hours:03		**Exam Marks:100**	

Module -1

Antenna Fundamentals and Definitions: Radiation Mechanisms, Overview, EM Fundamentals, Solution of Maxwell's Equations for Radiation Problems, Ideal Dipole, Radiation patterns, Directivity and Gain, Antenna impedance, Radiation efficiency, Antenna polarization.

Module -2

Arrays: Array factor for linear arrays, Uniformly excited equally spaced linear arrays, Pattern multiplication, Directivity of linear arrays, Non-uniformly excited equally spaced linear arrays, Mutual coupling.

Antenna Synthesis: Formulation of the synthesis problem, Synthesis principles, Line sources shaped beam synthesis, Linear array shaped beam synthesis, Fourier series, Woodward - Lawson sampling method, Comparison of shaped beam synthesis methods, low side lobe narrow main beam synthesis methods, Dolph Chebyshev linear array, Taylor line source method.

Module -3

Resonant Antennas: Wires and Patches, Dipole antenna, Yagi-Uda antennas, Micro-strip antenna. **Broadband antennas:** Traveling wave antennas Helical antennas, Biconical antennas, Sleeve antennas, and Principles of frequency independent antennas, Spiral antennas, and Log - periodic antennas.

Module -4

Aperture antennas: Techniques for evaluating gain, Reflector antennas- Parabolic reflector antenna principles, Axi-symmetric parabolic reflector antenna, Offset parabolic reflectors, Dual reflector antennas, Gain calculations for reflector antennas, Feed antennas for reflectors, Field representations, Matching the feed to the reflector, General feed model, Feed antennas used in practice.

Module -5

CEM for antennas: The method of moments: Introduction of the methods moments, Pocklington's integral equation, Integral equation and Kirchhoff's networking equations, Source modeling weighted residual formulations and computational consideration, Calculation of antenna and scatter characteristics.

Question paper pattern:

- The question paper will have ten questions.
- Each full question consists of 20 marks.
- There will be 2 full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub questions covering all the topics under a module.
- The students will have to answer 5 full questions, selecting one full question from each module.

Text Book: Stutzman and Thiele, "Antenna Theory and Design", 2nd Edition, John Wiley, 2010.

Reference Books:

1. C. A. Balanis, "Antenna Theory Analysis and Design", John Wiley, 2nd Edition 2007.
2. J. D. Krauss, "Antennas and Wave Propagation", McGraw Hill TMH, 4th Edition, 2010. 3. A.R.Harish, M. Sachidanada, "Antennas and propagation", Pearson Education, 2015.

Visvesvaraya Technological University, Belagavi.

PhD Coursework Courses – 2018 (Electronics and Communication Engineering)

As per 2017 Regulation

02	16ESP422	Group-4	Speech and Audio Processing
Exam Hours:03		**Exam Marks:100**	

Module -1

Digital Models For The Speech Signal: Process of speech production, Acoustic theory of speech production, Lossless tube models, and Digital models for speech signals. (Text 1)

Time Domain Models for Speech Processing: Time dependent processing of speech, Short time energy and average magnitude, Short time average zero crossing rate, Speech vs silence discrimination using energy & zero crossings, Pitch period estimation, Short time autocorrelation function, Short time average magnitude difference function, Pitch period estimation using autocorrelation function, Median smoothing. (Text 1)

Module -2

Digital Representations of the Speech Waveform: Sampling speech signals, Instantaneous quantization, Adaptive quantization, Differential quantization, Delta Modulation, Differential PCM, Comparison of systems, direct digital code conversion.(Text 1)

Short Time Fourier Analysis: Linear Filtering interpretation, Filter bank summation method, Overlap addition method, Design of digital filter banks, Implementation using FFT, Spectrographic displays, Pitch detection, Analysis by synthesis, Analysis synthesis systems. (Text 1)

Module -3

Homomorphic Speech Processing: Homomorphic systems for convolution, Complex cepstrum, Pitch detection, Formant estimation, Homomorphic vocoder. Linear Predictive Coding of Speech: Basic principles of linear predictive analysis, Solution of LPC equations, Prediction error signal, Frequency domain interpretation, Relation between the various speech parameters, Synthesis of speech from linear predictive parameters, Applications. (Text 1)

Module -4

Speech Enhancement: Spectral subtraction & filtering, Harmonic filtering, parametric re-synthesis, Adaptive noise cancellation. Speech Synthesis: Principles of speech synthesis, Synthesizer methods, Synthesis of intonation, Speech synthesis for different speakers, Speech synthesis in other languages, Evaluation, Practical speech synthesis. (Text 1)

Module -5

Automatic Speech Recognition: Introduction, Speech recognition vs. Speaker recognition, Signal processing and analysis methods, Pattern comparison techniques, Hidden Markov Models, Artificial Neural Networks. (Text 2)

Audio Processing: Auditory perception and psychoacoustics - Masking, frequency and loudness perception, spatial perception, Digital Audio, Audio Coding - High quality, low-bit-rate audio coding standards, MPEG, AC- 3, Multichannel audio - Stereo, 3D binaural and Multichannel surround sound. (Text 3)

Question paper pattern:

- The question paper will have ten questions.
- Each full question consists of 20 marks.
- There will be 2 full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub questions covering all the topics under a module.
- The students will have to answer 5 full questions, selecting one full question from each module.

Text Books:

1. L. R. Rabiner and R. W. Schafer, “Digital Processing of Speech Signals", Pearson Education (Asia) Pvt. Ltd., 2004.
2. L. R. Rabiner and B. Juang, “Fundamentals of Speech Recognition”, Pearson Education (Asia) Pvt. Ltd., 2004.
3. Z. Li and M.S. Drew, ―Fundamentals of Multimedia‖, Pearson Education (Asia) Pvt. Ltd., 2004.

Reference Book:

D. O‘Shaughnessy, “Speech Communications: Human and Machine”, Universities Press, 2001.

Visvesvaraya Technological University, Belagavi.

PhD Coursework Courses – 2018 (Electronics and Communication Engineering)

As per 2017 Regulation

03	16ESP12	Group-4	Statistical Signal Processing
Exam Hours:03		**Exam Marks:100**	

Module -1

Random Processes: Random variables, random processes, white noise, filtering random processes, spectral factorization, ARMA, AR and MA processes (Text 1).

Module -2

Signal Modeling: Least squares method, Padé approximation, Prony's method, finite data records, stochastic models, Levinson-Durbin recursion; Schur recursion; Levinson recursion(Text 1).

Module -3

Spectrum Estimation: Nonparametric methods, minimum-variance spectrum estimation, maximum entropy method, parametric methods, frequency estimation, principal components spectrum estimation(Text 1).

Module -4

Optimal and Adaptive Filtering: FIR and IIR Wiener filters, Discrete Kalman filter, FIR Adaptive filters: Steepest descent, LMS, LMS-based algorithms, adaptive recursive filters, RLS algorithm (Text 1).

Module -5

Array Processing: Array fundamentals, beam-forming, optimum array processing, performance considerations, adaptive beam-forming, linearly constrained minimum-variance beam-formers, side-lobe cancellers, space-time adaptive processing (Text 2).

Question paper pattern:

- The question paper will have ten questions.
- Each full question consists of 20 marks.
- There will be 2 full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub questions covering all the topics under a module.
- The students will have to answer 5 full questions, selecting one full question from each module.

Text Books:

1. Monson H.Hayes, ―Statistical Digital Signal Processing and Modeling‖, John Wiley & Sons (Asia) Pvt.Ltd., 2002.
2. Dimitris G. Manolakis, Vinay K. Ingle, and Stephen M. Kogon, "Statistical and Adaptive Signal Processing: Spectral Estimation, Signal Modeling, Adaptive Filtering and Array Processing‖, McGraw Hill International Edition,2000.

Reference Books:

1. Bernard Widrowand Samuel D.Stearns, "Adaptive Signal Processing‖, Pearson Education (Asia) Pvt. Ltd., 2001.
2. Simon Haykin, "Adaptive Filters‖, Pearson Education (Asia) Pvt. Ltd, 4th edition, 2002.
3. J.G. Proakis, C.M. Rader, F. Ling, C.L. Nikias, M. Moonen and I.K. Proudler, "Algorithms for Statistical Signal Processing‖, Prentice Hall, 2001, ISBN-0130622192.

Visvesvaraya Technological University, Belagavi.

PhD Coursework Courses – 2018 (Electronics and Communication Engineering)

As per 2017 Regulation

04	16ESP251	Group-4	Detection and Estimation
Exam Hours:03		**Exam Marks:100**	

Module -1

Classical Detection and Estimation Theory: Introduction, simple binary hypothesis tests, M Hypotheses, estimation theory, composite hypotheses, general Gaussian problem, performance bounds and approximations. (Text 1)

Module -2

Representations of Random Processes: Introduction, orthogonal representations, random process characterization, homogenous integral equations and eigen functions, periodic processes, spectral decomposition, vector random processes. (Text 2)

Module -3

Detection of Signals – Estimation of Signal Parameters: Introduction, detection and estimation in white Gaussian noise, detection and estimation in nonwhite Gaussian noise, signals with unwanted parameters, multiple channels and multiple parameter estimation. (Text 1)

Module -4

Estimation of Continuous Waveforms: Introduction, derivation of estimator equations, lower bound on the mean-square estimation error, multidimensional waveform estimation, nonrandom waveform estimation. . (Text 1)

Module -5

Linear Estimation: Properties of optimum processors, realizable linear filters, Kalman-Bucy filters, fundamental role of optimum linear filters. (Text 1)

Question paper pattern:

- The question paper will have ten questions.
- Each full question consists of 20 marks.
- There will be 2 full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub questions covering all the topics under a module.
- The students will have to answer 5 full questions, selecting one full question from each module.

Text Books:

1) Harry L. Van Trees, ―Detection, Estimation, and Modulation Theory‖, Part I, John Wiley & Sons, USA, 2001.
2) K Sam Shanmugam, Arthur M Breipohl, ―Random Signals: Detection, Estimation and Data Analysis", John Wiley & Sons, 1998.

Reference Books:

1) M.D. Srinath, P.K. Rajasekaran and R. Viswanathan, "Introduction to Statistical Signal Processing with Applications‖, Pearson Education (Asia) Pvt. Ltd. /Prentice Hall of India, 2003.
2) Steven M. Kay, "Fundamentals of Statistical Signal Processing," Volume I: "Estimation Theory", Prentice Hall, USA, 1998.
3) Steven M. Kay, "Fundamentals of Statistical Signal Processing", Volume II: "Detection Theory," Prentice Hall, USA, 1998.

Visvesvaraya Technological University, Belagavi.

PhD Coursework Courses – 2018 (Electronics and Communication Engineering)

As per 2017 Regulation

05	16EVE21	Group-4	Design of Analog and Mixed Mode VLSI Circuits
Exam Hours:03		**Exam Marks:100**	

Module -1

Basic MOS Device Physics: General considerations, MOS I/V Characteristics, second order effects, MOS device models.

Single stage Amplifier: Basic Concepts, Common Source stage.(Text 1)

Module -2

Single stage Amplifier: Source follower, common-gate stage, Cascode Stage, choice of device models. **Differential Amplifiers:** Single ended and differential operation, Basic differential pair, Common mode response, Differential pair with MOS loads, Gilbert cell. (Text 1)

Module -3

Passive and Active Current Mirrors: Basic current mirrors, Cascode Current mirrors, Active Current mirrors. **Operational Amplifiers (part-1):** General Considerations, One Stage OP-Amp, Two Stage OP-Amp, Gain boosting. (Text 1)

Module -4

Operational Amplifiers (part-2): Common Mode Feedback, Slew rate, Power Supply Rejection.

Phase Locked Loops: Simple PLL, Charge pump PLLs, Non-ideal effects in PLLs, Delay-Locked Loops, Applications. (Text 1)

Module -5

Data Converter Architectures: DAC & ADC Specifications, Current Steering DAC, Charge Scaling DAC, Cyclic DAC, Pipeline DAC, Flash ADC, Pipeline ADC, Integrating ADC, Successive Approximation ADC. (Text 2)

Question paper pattern:

- The question paper will have ten questions.
- Each full question consists of 20 marks.
- There will be 2 full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub questions covering all the topics under a module.
- The students will have to answer 5 full questions, selecting one full question from each module.

Text Books:

1. Behzad Razavi, ―Design of Analog CMOS Integrated Circuits‖, TMH, 2007.
2. R. Jacob Baker, ―CMOS Circuit Design, Layout, and Simulation‖, Second Edition, Wiley.

Reference Book:

Phillip E. Allen, Douglas R. Holberg, ―CMOS Analog Circuit Design‖, Second Edition, Oxford University Press.

Visvesvaraya Technological University, Belagavi.

PhD Coursework Courses – 2018 (Electronics and Communication Engineering)

As per 2017 Regulation

06	16EVE23	Group-4	Advances in VLSI Design
Exam Hours:03		**Exam Marks:100**	

Module -1

Implementation Strategies For Digital ICS: Introduction, From Custom to Semicustom and Structured Array Design Approaches, Custom Circuit Design, Cell-Based Design Methodology, Standard Cell, Compiled Cells, Macrocells, Megacells and Intellectual Property, Semi-Custom Design Flow, Array-Based Implementation Approaches, Pre-diffused (or Mask-Programmable) Arrays, Pre-wired Arrays, Perspective-The Implementation Platform of the Future.

Module -2

Coping With Interconnect: Introduction, Capacitive Parasitics, Capacitance and Reliability-Cross Talk, Capacitance and Performance in CMOS, Resistive Parasitics, Resistance and Reliability-Ohmic Voltage Drop, Electromigration, Resistance and Performance-RC Delay, Inductive Parasitics, Inductance and Reliability-Voltage Drop, Inductance and Performance-Transmission Line Effects, Advanced Interconnect Techniques, Reduced-Swing Circuits, Current-Mode Transmission Techniques, Perspective: Networks-on-a-Chip.

Module -3

Timing Issues In Digital Circuits: Introduction, Timing Classification of Digital Systems, Synchronous Interconnect, Mesochronous interconnect, Plesiochronous Interconnect, Asynchronous Interconnect, Synchronous Design — An In-depth Perspective, Synchronous Timing Basics, Sources of Skew and Jitter, Clock-Distribution Techniques, Latch-Based Clocking, SelfTimed Circuit Design, Self-Timed Logic - An Asynchronous Technique, Completion-Signal Generation, Self-Timed Signaling, Practical Examples of Self-Timed Logic, Synchronizers and Arbiters, Synchronizers-Concept and Implementation, Arbiters, Clock Synthesis and Synchronization Using a Phase-Locked Loop, Basic Concept, Building Blocks of a PLL.

Module -4

Designing Memory and Array Structures: Introduction, Memory Classification, Memory Architectures and Building Blocks, The Memory Core, Read-Only Memories, Nonvolatile Read-Write Memories, Read-Write Memories (RAM), Contents-Addressable or Associative Memory (CAM), Memory Peripheral Circuitry, The Address Decoders, Sense Amplifiers, Voltage References, Drivers/Buffers, Timing and Control.

Module -5

Designing Memory and Array Structures: Memory Reliability and Yield, Signal-to-Noise Ratio, Memory yield, Power Dissipation in Memories, Sources of Power Dissipation in Memories, Partitioning of the memory, Addressing the Active Power Dissipation, Dataretention dissipation, Case Studies in Memory Design: The Programmable Logic Array (PLA), A 4 Mbit SRAM, A 1 Gbit NAND Flash Memory, Perspective: Semiconductor Memory Trends and Evolutions.

Question paper pattern:

- The question paper will have ten questions.
- Each full question consists of 20 marks.
- There will be 2 full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub questions covering all the topics under a module.
- The students will have to answer 5 full questions, selecting one full question from each module.

Text Book:

Jan M Rabey, Anantha Chandrakasan, Borivoje Nikolic, ―Digital Integrated Circuits-A Design Perspective‖, PHI, 2nd Edition.

Reference Books:

1. M. Smith, ―Application Specific Integrated circuits‖, Addison Wesley, 1997
2. H. Veendrick, ―MOS IC‘s: From Basics to ASICs, Wiley-VCH, 1992.
3. Anantha P. Chandrakasan , Robert W. Brodersen, ―Low Power Digital CMOS Design‖, Kluwer Academic Publisher, 1995.

Visvesvaraya Technological University, Belagavi.

PhD Coursework Courses – 2018 (Electronics and Communication Engineering)

As per 2017 Regulation

07	16EIE22	Group-4	Design of Power Converters
Exam Hours:03		**Exam Marks:100**	

Module -1

Introduction to Control characteristics of power semiconductor devices: SCR, BJT, MOSFET, GTO, MCT, SITH, IGBT. Comparison of controllable switches. AC to Controlled DC Converter: Thyristor circuits and their control, Gate Triggering, Single phase converters, Three phase converters.(Text 1)

Module -2

DC to DC converters: Introduction, control of DC-DC converters, Buck, Boost, Buck-Boost, Cuk converter. Inverters: Introduction, principle of operation, single phase inverters, three phase inverters-120 and 180 modes of operation. (Text 1)

Module -3

Switching DC power supplies: linear power supply, overview of switching power supply, DC - DC converters with electrical isolation, flyback converter, forward converter, push-pull converter, Half and Full bridge converter, current mode control, power supply protection. (Text 1)

Module -4

Magnetics for switched mode converters: Power Handling capacity of a transformer, Area product, window utilization factor. Transformer designs – forward converter, half and Full Bridge converter, Push-pull converter, Flyback converter. Design of Inductors, problems. (Text 2)

Module -5

PWM controlling Techniques: single PWM, Multiple, sinusoidal, modified, phase displacement control. Power electronic applications: UPS, control of motor drives, criteria for selecting drive components, High frequency fluorescent lighting. Industrial applications: Induction heating, Electric welding.(Text 1)

Question paper pattern:

- The question paper will have ten questions.
- Each full question consists of 20 marks.
- There will be 2 full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub questions covering all the topics under a module.
- The students will have to answer 5 full questions, selecting one full question from each module.

Text Books:

1. M.Ned Mohan Tore, Undeland and William. P. Robbins; ―Power Electronics: Converters, Applications and Design‖, 3rd Edition, John Wiley and Sons, 2003

2. Umanand. L. & S.R.Bhat. ―Design of Magnetic Components for Switched Mode Power Converters‖, Wiley Eastern Publication, 1992.

Reference Books:

M. H. Rashid, ―Power Electronics‖ 3rd edition, PHI / Pearson publisher 2004.

Visvesvaraya Technological University, Belagavi.

PhD Coursework Courses – 2018 (Electronics and Communication Engineering)

As per 2017 Regulation

01	16ECS153	Group-5	OPTICAL COMMUNICATION AND NETWORKING

Exam Hours:03 **Exam Marks:100**

Module -1 Introduction to optical networking: Propagation of signals in optical fiber, Different losses, Nonlinear effects, Solutions, Optical sources, Detectors.
Optical Components (Part-1): Couplers, Isolators, Circulators and Multiplexers.

Module -2Optical Components (Part-2): Filters, Gratings, Interferometers, Amplifiers.
Modulation - Demodulation: Formats, Ideal receivers, Practical detection receivers, Optical preamplifiers, Noise considerations, Bit error rates, Coherent detection.

Module -3 Transmission System Engineering: System model, Power penalty, Transmitter, Receiver, Different optical amplifiers
Client Layers: Client layers of optical layer, SONET/SDH, Multiplexing, layers, Frame structure, ATM functions, Adaptation layers, Quality of Service (QoS) and flow control, ESCON, HIPPI.

Module -4WDM network elements: Optical line terminal, Optical line amplifiers, Optical Add/ Drop Multiplexors, Optical cross connectors.
WDM Network Design: WDM network design, Cost tradeoffs, LTD and RWA problems, Routing and wavelength assignment, Wavelength conversion.

Module -5. **Control and Management (Part-1**): Network management functions, management framework, Information model, management protocols, Layers within optical layer.
Control and Management (Part-2): Performance and fault management, Impact of transparency, BER measurement, Optical trace, Alarm management, Configuration management.

Question paper pattern:

- The question paper will have ten questions.
- Each full question consists of 20 marks.
- There will be 2 full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub questions covering all the topics under a module.

The students will have to answer 5 full questions, selecting one full question from each module.

Text Book:

1. Rajiv Ramswami and K. N. Sivarajan, "Optical Networks", Morgon Kauffman Publishers, 3rd edition, 2010.

Reference Books:

1. John M. Senior, "Optical fiber communication", Pearson edition, 2000.
2. Gerd Kaiser, "Optical fiber Communication Systems", John Wiley, New York, 1997.
3. P. E. Green, "Optical Networks", Prentice Hall, 1994.

Visvesvaraya Technological University, Belagavi.
PhD Coursework Courses – 2018 (Electronics and Communication Engineering)
As per 2017 Regulation

02	16ECS151	Group-5	ADVANCED COMPUTER NETWORKS
Exam Hours:03		**Exam Marks:100**	

Module -1 Introduction to networks: Computer network, Telephone networks, Networking principles (Text 1), Protocol layering (Text 2), Multiplexing- TDM, FDM, SM, WDM (Text 1).
Multiple Access: Introduction, Choices and constraints, base technologies, centralized and distributed access schemes (Text 2).

Module -2. **Local Area Networks**: Ethernet - Physical layer, MAC, LLC, LAN interconnection, Token ring- Physical layer, MAC, LLC, FDDI (Text 1). Switching- introduction, circuit switching, packet switching, multicasting (Text 2).
Scheduling: Introduction, requirements, choices, performance bounds, best- effort techniques. Naming and addressing (Text 2).

Module -3 SONET, SDH (Text 2), ATM Networks- features, signaling and routing, header and adaptation layers (Text 1), virtual circuits, SSCOP, Internet- addressing, routing, end point control (Text 2).
Internet protocols- IP, TCP, UDP, ICMP, HTTP (Text 2).

Module -4 Traffic Management: Introduction, framework for traffic management, traffic models, traffic classes, traffic scheduling (Text 2).
Control of Networks: Objectives and methods of control, routing optimization in circuit and datagram networks, Markov chains, Queuing models in circuit and datagram networks (Text 1).

Module -5 Congestion and flow control: Window congestion control, rate congestion control, control in ATM Networks (Text 1), flow control model, open loop flow control, closed loop flow control (Text 2).

Question paper pattern:

- The question paper will have ten questions.
- Each full question consists of 20 marks.
- There will be 2 full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub questions covering all the topics under a module.

The students will have to answer 5 full questions, selecting one full question from each module.

Text Books:

1. J. Walrand and P. Varaya, "High performance communication networks", Harcourt Asia (Morgan Kaufmann), 2000.
2. S. Keshav, "An Engineering approach to Computer Networking", Pearson Education, 1997.

Reference Books:

1. Leon-Garcia, and I. Widjaja, "Communication network: Fundamental concepts and key architectures", TMH, 2000.
2. J. F. Kurose, and K. W. Ross, "Computer networking: A top down approach featuring the Internet", Pearson Education, 2001.

Visvesvaraya Technological University, Belagavi.
PhD Coursework Courses – 2018 (Electronics and Communication Engineering)
As per 2017 Regulation

03	16ECS254	Group-5	CRYPTOGRAPHY AND NETWORK SECURITY

Exam Hours:03 **Exam Marks:100**

Module -1 Foundations: Terminology, Steganography, substitution ciphers and transpositions ciphers, Simple XOR, One-Time Pads, Computer Algorithms (Text 2: Chapter 1: Section 1.1 to 1.6)
SYMMETRIC CIPHERS: Traditional Block Cipher structure, Data encryption standard (DES), The AES Cipher. (Text 1: Chapter 2: Section2.1, 2.2, Chapter 4)

Module -2 Introduction to modular arithmetic, Prime Numbers, Fermat's and Euler's theorem, primality testing, Chinese Remainder theorem, discrete logarithm. (Text 1: Chapter 7: Section 1, 2, 3, 4, 5)
Principles of Public-Key Cryptosystems, The RSA algorithm, Diffie - Hellman Key Exchange, Elliptic Curve Arithmetic, Elliptic Curve Cryptography (Text 1: Chapter 8, Chapter 9: Section 9.1, 9.3, 9.4)

Module -3 Pseudo-Random-Sequence Generators and Stream Ciphers: Linear Congruential Generators, Linear Feedback Shift Registers, Design and analysis of stream ciphers, Stream ciphers using LFSRs, A5, Hughes XPD/KPD, Nanoteq, Rambutan, Additive generators, Gifford, Algorithm M, PKZIP (Text 2: Chapter 16)

Module -4 One-Way Hash Functions: Background, Snefru, N-Hash, MD4, MD5, Secure Hash Algorithm [SHA],One way hash functions using symmetric block algorithms, Using public key algorithms, Choosing a one-way hash functions, Message Authentication Codes. Digital Signature Algorithm, Discrete Logarithm Signature Scheme (Text 2: Chapter 18: Section 18.1 to 18.5, 18.7, 18.11 to 18.14 and Chapter 20: Section 20.1, 20.4)

Module -5 E-mail Security: Pretty Good Privacy-S/MIME (Text 1: Chapter 17: Section 17.1, 17.2).
IP Security: IP Security Overview, IP Security Policy, Encapsulation Security Payload (ESP), Combining security Associations. (Text 1: Chapter 18: Section 18.1 to 18.4).
Web Security: Web Security Considerations, SSL (Text 1: Chapter 15: Section 15.1, 15.2).

Question paper pattern:

- The question paper will have ten questions.
- Each full question consists of 20 marks.
- There will be 2 full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub questions covering all the topics under a module.

The students will have to answer 5 full questions, selecting one full question from each module.

Text Books:

1. William Stallings , "Cryptography and Network Security Principles and Practice", Pearson Education Inc., 6th Edition, 2014, ISBN: 978-93-325-1877-3
2. Bruce Schneier, "Applied Cryptography Protocols, Algorithms, and Source code in C", Wiley Publications, 2nd Edition, ISBN: 9971-51-348-X

Reference Books:

1. Cryptography and Network Security, Behrouz A. Forouzan, TMH, 2007.
2. Cryptography and Network Security, Atul Kahate, TMH, 2003.

Visvesvaraya Technological University, Belagavi.

PhD Coursework Courses – 2018 (Electronics and Communication Engineering)

As per 2017 Regulation

04	16ESP24	Group-5	Biomedical Signal Processing
Exam Hours:03		**Exam Marks:100**	

Module -1 Introduction-Genesis and significance of bio electric potentials, ECG, EOG, EMG and their monitoring and measurement, Spectral analysis.

Module -2 Filtering- digital and analog filtering, correlation and estimation techniques, AR / ARMA models, Adaptive Filters.

Module -3ECG-Pre-processing, Measurements of amplitude and time intervals, Classification, QRS detection, ST segment analysis, Base line wander removal, waveform recognition, morphological studies and rhythm analysis, automated diagnosis based on decision theory ECT compression, Evoked potential estimation.

Module -4 EEG: Evoked responses, Epilepsy detection, Spike detection, Hjorth parameters, averaging techniques, removal of Artifacts by averaging and adaptive algorithms, pattern recognition of alpha, beta, theta and delta waves in EEG waves, sleep stages.

Module -5 EMG-Wave pattern studies, bio feedback, Zero crossings, Integrated EMG. Time frequency methods and Wavelets in Biomedical Signal Processing.

Question paper pattern:

- The question paper will have ten questions.
- Each full question consists of 20 marks.
- There will be 2 full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub questions covering all the topics under a module.

The students will have to answer 5 full questions, selecting one full question from each module.

Text Book:

1. Willis J Tompkins, ED, “Biomedical Digital Signal Processing”, Prentice-Hall of India, 1996.

Reference Books:

1) R E Chellis and RI Kitney, “Biomedical Signal Processing”, in IV parts, Medical and Biological Engg. and current computing, 1990-91.

2) Special issue on “Biological Signal Processing”, Proc. IEEE 1972

3) Arnon Kohen, “Biomedical Signal Processing”, Volumes I &I I, CRC Press.

4) Metin Aray, “Time frequency and Wavelets in Biomedical Signal Processing”, IEEE Press, 1999.Current Published literature.

Visvesvaraya Technological University, Belagavi.

PhD Coursework Courses – 2018 (Electronics and Communication Engineering)

As per 2017 Regulation

05	16ESP253	Group-5	Pattern Recognition
Exam Hours:03		**Exam Marks:100**	

Module -1 Introduction: Applications of pattern recognition, statistical decision theory, image processing and analysis. Probability: Introduction, probability of events, random variables, Joint distributions and densities, moments of random variables, estimation of parameters from samples, minimum risk estimators Statistical Decision Making: Introduction, Baye‘s Theorem, multiple features, conditionally independent features, decision boundaries, unequal costs of error, estimation of error rates, the leaving-one—out technique. Characteristic curves, estimating the composition of populations.

Module -2 Nonparametric Decision Making: Introduction, histograms, Kernel and window estimators, nearest neighbor classification techniques, adaptive Decision boundaries, adaptive discriminate Functions, minimum squared error discriminate functions, choosing a decision making technique.

Module -3 Unsupervised Classification: Clustering, Hierarchical Clustering, Graph Based Method, Sum of Squared Error Technique ,Iterative Optimization clustering.

Module -4 Neural Network Classifier: Single and Multilayer Perceptron, Back Propagation Learning, Hopfield Network, Fuzzy Neural Network

Module -5 Time Varying Pattern Recognition, First Order Hidden Markov Model Evaluation, Decoding, Learning.

Question paper pattern:

- The question paper will have ten questions.
- Each full question consists of 20 marks.
- There will be 2 full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub questions covering all the topics under a module.

The students will have to answer 5 full questions, selecting one full question from each module.

Text Book:

1. Richard O. Duda, Peter E. Hart, David G. Stork, ―Pattern Classification‖, Wiley, 2nd edition, 2001.

Reference Books:

1. Eart Gose, Richard Johnsonburg and Steve Joust, ―Pattern Recognition and Image Analysis‖, Prentice-Hall ofIndia-2003.

2. Robert J Schalkoff, ―Pattern recognition: Statistical, Structural and neural approaches‖, John Wiley.

Visvesvaraya Technological University, Belagavi.
PhD Coursework Courses – 2018 (Electronics and Communication Engineering)
As per 2017 Regulation

06	16EVE24	Group-5	Real Time Operating System
Exam Hours:03		**Exam Marks:100**	

Module -1 Real-Time Systems and Resources: Brief history of Real Time Systems, A brief history of Embedded Systems. System Resources, Resource Analysis, Real-Time Service Utility, Scheduler concepts, Real-Time OS, State transition diagram and tables, Thread Safe Reentrant Functions. (Text 1: Selected sections from Chap. 1, 2)

Module -2Processing with Real Time Scheduling: Scheduler Concepts, Preemptive Fixed Priority Scheduling Policies with timing diagrams and problems and issues, Feasibility, Rate Monotonic least upper bound, Necessary and Sufficient feasibility, Deadline –Monotonic Policy, Dynamic priority policies, Alternative to RM policy. (Text 1: Chap. 2,3,7)

Module -3Memory and I/O: Worst case execution time, Intermediate I/O, Shared Memory, ECC Memory, Flash file systems. Multi-resource Services, Blocking, Deadlock and live lock, Critical sections to protect shared resources, Missed deadline, QoS, Reliability and Availability, Similarities and differences, Reliable software, Available software.(Text 1: Selected topics from Chap. 4,5,6,7,11)

Module -4 Firmware Components: The 3 firmware components, RTOS system software mechanisms, Software application components. Debugging Components, Exceptions, assert, Checking return codes, Singlestep debugging, kernel scheduler traces, Test access ports, Trace Ports, External test equipment. (Text 1: Selected topics from Chap. 8,9)

Module -5 Process and Threads: Process and thread creations, Simple Programs, Programs related to semaphores, message queue, shared buffer applications involving inter task/thread communication using multiple threads. (Text 2: Chap. 11)

Question paper pattern:

- The question paper will have ten questions.
- Each full question consists of 20 marks.
- There will be 2 full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub questions covering all the topics under a module.

The students will have to answer 5 full questions, selecting one full question from each module.

Text Books:

1. Sam Siewert, ―Real-Time Embedded Systems and Components‖, Cengage Learning India Edition, 2007.
2. Dr. K.V.K.K Prasad, Embedded/Real Time Systems, Concepts, Design and Programming, Black Book, DreamTech Press, New edition, 2010

Reference Books:

1. James W S Liu, ―Real Time System‖, Pearson education, 2008.
2. DreamTech Software Team, ―Programming for Embedded Systems , John Wiley, India Pvt. Ltd., 2008.

Visvesvaraya Technological University, Belagavi.
PhD Coursework Courses – 2018 (Electronics and Communication Engineering)
As per 2017 Regulation

07	16ECS424	Group-5	Real Time Systems
Exam Hours:03		**Exam Marks:100**	

Module -1 Introduction to Real-Time Embedded Systems: Brief history of Real Time Systems, A brief history of Embedded Systems.
System Resources: Resource Analysis, Real-Time Service Utility, Scheduling Classes, The Cyclic Executive, Scheduler Concepts, Preemptive Fixed Priority Scheduling Policies, Real-Time OS, Thread Safe Re-entrant Functions.

Module -2Processing: Preemptive Fixed-Priority Policy, Feasibility, Rate Montonic least upper bound, Necessary and Sufficient feasibility, Deadline – Monotonic Policy, Dynamic priority policies.
I/O Resources: Worst-case Execution time, Intermediate I/O, Execution efficiency, I/O Architecture.
Memory: Physical hierarchy, Capacity and allocation, Shared Memory, ECC Memory, Flash file systems.

Module -3 Multi-resource Services: Blocking, Deadlock and livestock, Critical sections to protect shared resources, priority inversion.
Soft Real-Time Services: Missed Deadlines, QoS, Alternatives to rate monotonic policy, Mixed hard and soft real-time services.

Module -4 Embedded System Components: Firmware components, RTOS system software mechanisms, Software application components.
Debugging Components: Exceptions assert, Checking return codes, Single-step debugging, kernel scheduler traces, Test access ports, Trace ports, Power-On self test and diagnostics.

Module -5 Performance Tuning: Basic concepts of drill-down tuning,
hardware – supported profiling and tracing, Building performance monitoring into software, Path length.
High availability and Reliability Design: Reliability and Availability, Similarities and differences, Reliability, Reliable software, Available software, Design tradeoffs, Hierarchical applications for Fail-safe design.

Question paper pattern:

- The question paper will have ten questions.
- Each full question consists of 20 marks.
- There will be 2 full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub questions covering all the topics under a module.

The students will have to answer 5 full questions, selecting one full question from each module.

Text Book:

Sam Siewert, "Real-Time Embedded Systems and Components", Cengage Learning India Edition, 2007.

Reference Books:

1. Krishna CM and Kang Singh G, "Real time systems", Tata McGraw Hill, 2003, ISBN: 0-07-114243-64
2. Qing Li and Carolyn Yao, "Real-Time Concepts for Embedded Systems", CMP Books, 2003, ISBN:1578201241
3. Jane W. S. Liu, "Real Time Systems", Prentice Hall, 2000, ISBN: 0130996513
4. Phillip A. Laplante, "Real-Time Systems Design and Analysis", John Wiley & Sons, 2004.

Visvesvaraya Technological University, Belagavi.

PhD Coursework Courses – 2018 (Electronics and Communication Engineering)

As per 2017 Regulation

08	16EVE153	Group-5	ASIC DESIGN

Exam Hours:03 | **Exam Marks:100**

Module -1 Introduction to ASICs, Full custom, Semi-custom and Programmable ASICs, ASIC Design flow, ASIC cell libraries.

CMOS Logic: Datapath Logic Cells**:** Data Path Elements, Adders: Carry skip, Carry bypass, Carry save, Carry select, Conditional sum, Multiplier (Booth encoding), Data path Operators, I/O cells.

Module -2ASIC Library Design: Logical effort: Predicting Delay, Logical area and logical efficiency, Logical paths, Multi stage cells, Optimum delay and number of stages.

Programmable ASIC Logic Cells:

MUX as Boolean function generators, Actel ACT: ACT 1, ACT 2 and ACT 3 Logic Modules, Xilinx LCA: XC3000 CLB, Altera FLEX and MAX.

Module -3Programmable ASIC I/O Cells: Xilinx and Altera I/O Block.

Low-level design entry: Schematic entry: Hierarchical design, Netlist screener.

ASIC Construction: Physical Design, CAD Tools.

Partitioning: Goals and objectives, Constructive Partitioning, Iterative Partitioning mprovement, KL, FM and Look Ahead algorithms.

Module -4Floor planning and placement: Goals and objectives, Floor planning tools, Channel definition, I/O and Power planning and Clock planning. Placement**:** Goals and Objectives, Min-cut Placement algorithm, Iterative Placement Improvement, Physical Design Flow.

Module -5 Routing: Global Routing: Goals and objectives, Global Routing Methods, Back-annotation. Detailed Routing: Goals and objectives, Measurement of Channel Density, Left-Edge and Area-Routing Algorithms. Special Routing, Circuit extraction and DRC.

Question paper pattern:

- The question paper will have ten questions.
- Each full question consists of 20 marks.
- There will be 2 full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub questions covering all the topics under a module.

The students will have to answer 5 full questions, selecting one full question from each module.

Text Book:

Michael John Sebastian Smith, "Application - Specific Integrated Circuits" Addison- Wesley Professional; 2005.

Reference Books:

1. Neil H.E. Weste, David Harris, and Ayan Banerjee, "CMOS VLSI Design: A Circuits and Systems Perspective", 3rd edition, Addison Wesley/ Pearson education, 2011.

2. Vikram Arkalgud Chandrasetty, "VLSI Design: A Practical Guide for FPGA and ASIC Implementations", Springer, 2011, ISBN: 978-1-4614-1119-2.

3. Rakesh Chadha**,** Bhasker J., "An ASIC Low Power Primer", Springer, ISBN: 978-1-4614-4270-7.

Visvesvaraya Technological University, Belagavi.

PhD Coursework Courses – 2018 (Electronics and Communication Engineering)

As per 2017 Regulation

09	16EVE13	Group-5	ADVANCED EMBEDDED SYSTEM
Exam Hours:03		**Exam Marks:100**	

Module -1 Embedded System: Embedded vs General computing system, classification, application and purpose of ES. Core of an Embedded System, Memory, Sensors, Actuators, LED, Optocoupler, Communication Interface, Reset circuits, RTC, WDT, Characteristics and Quality Attributes of Embedded Systems (Selected Topics from Ch -1, 2, 3 of Text 1).

Module -2 Hardware Software Co-Design, embedded firmware design approaches, computational models, embedded firmware development languages, Integration and testing of Embedded Hardware and firmware, Components in embedded system development environment (IDE), Files generated during compilation, simulators, emulators and debugging (Selected Topics From Ch-7, 9, 12, 13 of Text 1).

Module -3ARM-32 bit Microcontroller: Thumb-2 technology and applications of ARM, Architecture of ARM Cortex M3, Various Units in the architecture, General Purpose Registers, Special Registers, exceptions, interrupts, stack operation, reset sequence (Ch 1, 2, 3 of Text 2).

Module -4 Instruction Sets: Assembly basics, Instruction list and description, useful instructions, Memory Systems, Memory maps, Cortex M3 implementation overview, pipeline and bus interface (Ch-4, 5, 6 of Text 2).

Module -5 Exceptions, Nested Vector interrupt controller design, Systick Timer, Cortex-M3 Programming using assembly and C language, CMSIS (Ch-7, 8, 10 of Text 2).

Question paper pattern:

- The question paper will have ten questions.
- Each full question consists of 20 marks.
- There will be 2 full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub questions covering all the topics under a module.

The students will have to answer 5 full questions, selecting one full question from each module.

Text Books:

1. K. V. Shibu, "Introduction to embedded systems", TMH education Pvt. Ltd. 2009.
2. Joseph Yiu, “The Definitive Guide to the ARM Cortex-M3”, 2nd edn, Newnes, (Elsevier), 2010.

Reference Book:

1. James K. Peckol, "Embedded systems- A contemporary design tool", John Wiley, 2008.

Visvesvaraya Technological University, Belagavi.
PhD Coursework Courses – 2018 (Electronics and Communication Engineering)
As per 2017 Regulation

10	16EVE14	Group-5	LOW POWER VLSI DESIGN
Exam Hours:03		**Exam Marks:100**	

Module -1 Introduction: Need for low power VLSI chips, charging and discharging capacitance, short circuit current in CMOS leakage current, static current, basic principles of low power design, low power figure of merits.
Simulation power analysis: SPICE circuit simulation, discrete transistor modeling and analysis, gate level logic simulation, architecture level analysis, data correlation analysis in DSP systems, Monte Carlo simulation.

Module -2Probabilistic power analysis: Random logic signals, probability & frequency, probabilistic power analysis techniques, signal entropy.
Circuit: Transistor and gate sizing, equivalent pin ordering, network restructuring and reorganization, special latches and flip flops, low power digital cell library, adjustable device threshold voltage.

Module -3Logic: Gate reorganization, signal gating, logic encoding, state machine encoding, pre-computation logic (Text 1).
Low power Clock Distribution: Power dissipation in clock distribution, single driver Vs distributed buffers, Zero skew Vs tolerable skew, chip & package co design of clock network (Text 2).

Module -4 Low power Architecture & Systems: Power & performance management, switching activity reduction, parallel architecture with voltage reduction, flow graph transformation (Text 1).
Low power arithmetic components: Introduction, circuit design style, adders, multipliers, division (Text 2).

Module -5Low power memory design: Introduction, sources and reductions of power dissipation in memory subsystem, sources of power dissipation in DRAM and SRAM (Text 2).
Algorithm & Architectural Level Methodologies: Introduction, design flow, Algorithmic level analysis & optimization, Architectural level estimation & synthesis (Text 2).
Advanced Techniques: Adiabatic computation, pass transistor, Asynchronous circuits (Text 1).

Question paper pattern:

- The question paper will have ten questions.
- Each full question consists of 20 marks.
- There will be 2 full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub questions covering all the topics under a module.

The students will have to answer 5 full questions, selecting one full question from each module.

Text Books:

1. Gary K. Yeap, “Practical Low Power Digital VLSI Design”, Kluwer Academic, 1998.
2. Jan M.Rabaey, Massoud Pedram, “Low Power Design Methodologies” Kluwer Academic, 2010.

Reference Books:

1. Kaushik Roy, Sharat Prasad, “Low-Power CMOS VLSI Circuit Design” Wiley, 2000
2. A.P.Chandrasekaran and R.W.Broadersen, “Low power digital CMOS design”, Kluwer Academic,1995.
3. A Bellamour and M I Elmasri, “ Low power VLSI CMOS circuit design”, Kluwer Academic,1995.

Visvesvaraya Technological University, Belagavi.

PhD Coursework Courses – 2018 (Electronics and Communication Engineering)

As per 2017 Regulation

11	16EIE424	Group-5	Industrial Drive
Exam Hours:03		**Exam Marks:100**	

Module -1 AN INTRODUCTION TO ELECTRICAL DRIVES & ITS APPLICATIONS: Electrical Drives, Advantages of Electrical Drives, Parts of Electrical Drives, Choice of Electrical Drive, Status of dc and ac Drives, Fundamental Torque Equations, Speed Torque Conventions and Multiquadrant Operation.
Applications: Rolling mill drives, cement mill drives, paper mill drives and textile mill drives.

Module -2SELECTION OF MOTOR POWER RATING: Thermal model of motor for heating and cooling, Classes of motor duty, determination of motor rating.
D C MOTOR DRIVES 1: Starting braking, transient analysis, single phase fully controlled rectifier, control of dc separately excited motor, Single-phase half controlled rectifier: control of dc separately excited motor.

Module -3DC MOTOR DRIVES 2: Three phase fully controlled rectifier: control of dc separately excited motor, three phases half controlled rectifier: control of dc separately excited motor, multiquadrant operation of dc separately excited motor fed form fully controlled rectifier. Rectifier control of dc series motor, chopper controlled dc drives, chopper control of separately excited dc motor. Chopper control of series motor.

Module -4 INDUCTION MOTOR DRIVES:
Operation with unbalanced source voltage and single phasing, operation with unbalanced rotor impedances, analysis of induction motor fed from non-sinusoidal voltage supply, starting braking, transient analysis. Stator voltage control variable voltage frequency control from voltage sources, voltage source inverter control, closed loop control, current source inverter control, current regulated voltage source inverter control.

Module -5 SYNCHRONOUS MOTOR DRIVES: Operation form faced frequency supply, synchronous motor variable speed drives, and variable frequency control of multiple synchronous motors. Self-controlled synchronous motor drive employing load commutated thruster inverter.

Question paper pattern:

- The question paper will have ten questions.
- Each full question consists of 20 marks.
- There will be 2 full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub questions covering all the topics under a module.

The students will have to answer 5 full questions, selecting one full question from each module.

Text Book:

G.K Dubey, **Fundamentals of Electrical Drives,** 2 Edition, 5th reprint, Narosa publishing house.

Reference Books:

1. N.K De and P.K. Sen, **Electrical Drives,** PHI, 2007
2. S.K Pillai**, A First Course On Electric Drives**, S.K Pillai-Wiley Eastern Ltd 1990.
3. V.R. Moorthi, **Power Electronics, Devices, Circuits and Industrial Applications**, Oxford University Press, 2005.

Visvesvaraya Technological University, Belagavi.

PhD Coursework Courses – 2018 (Electronics and Communication Engineering)

As per 2017 Regulation

01	16ECS252	Group-6	MULTIMEDIA OVER COMMUNICATION LINKS

Exam Hours:03 | **Exam Marks:100**

Module -1 Multimedia Communications: Introduction, Multimedia information representation, multimedia networks, multimedia applications, Application and networking terminology.(Chap. 1 of Text1)
Information Representation: Introduction, Text, Images. (Chap. 2- Sections 2.2 and 2.3 of Text 1)

Module -2. **Information Representation**: Audio and Video. (Chap. 2 - Sections 2.4 and 2.5 of Text 1)
Distributed multimedia systems: Introduction, main Features of a DMS, Resource management of DMS, Networking, Multimedia operating systems. (Chap. 4 - Sections 4.1 to 4.5 of Text 2)

Module -3Multimedia Processing in Communication: Introduction, Perceptual coding of digital Audio signals, Transform Audio Coders, Audio Sub band Coders. (Chap. 3 - Sections 3.1, 3.2, 3.6, 3.7 of Text 2)

Module -4 Multimedia Communication Standards: Introduction, MPEG approach to multimedia standardization, MPEG-1, MPEG-2, Overview of MPEG-4. (Chap. 5 - Sections 5.1 to 5.4 and 5.5.1 of Text 2)

Module -5 Multimedia Communication Across Networks: Packet audio/video in the network environment, Video transport across generic networks, Multimedia Transport across ATM Networks. (Chap. 6 - Sections 6.1, 6.2, 6.3 of Text 2)

Question paper pattern:

- The question paper will have ten questions.
- Each full question consists of 20 marks.
- There will be 2 full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub questions covering all the topics under a module.
- The students will have to answer 5 full questions, selecting one full question from each module.

Text Books:

1. Fred Halsall, "Multimedia Communications", Pearson education, 2001, ISBN -9788131709948.
2. K. R. Rao, Zoran S. Bojkovic, Dragorad A. Milovanovic, "Multimedia Communication Systems", Pearson education, 2004. ISBN -9788120321458.

Reference Book:

1. Raif steinmetz, Klara Nahrstedt, "Multimedia: Computing, Communications and Applications", Pearson education, 2002, ISBN -9788177584417.

Visvesvaraya Technological University, Belagavi.
PhD Coursework Courses – 2018 (Electronics and Communication Engineering)
As per 2017 Regulation

02	16ECS24	Group-6	RF AND MICROWAVE CIRCUIT DESIGN
Exam Hours:03		**Exam Marks:100**	

Module -1 Wave propagation in networks: Introduction, Reasons for Using RF/Microwaves, Applications, RF Waves, RF and Microwave circuit design, Introduction to Components Basics, Analysis of Simple Circuit in Phasor Domain, RF Impedance Matching, Transmission Media, High Frequency Parameters, Formulation of S-parameters, Properties of S-Parameters, Transmission Matrix, Generalized S-parameters.

Module -2Smith chart and its Applications: Introduction, Smith Chart, Derivation of Smith Chart, Smith Chart Circular and Radial Scales, Application of Smith chart.

Module -3Basic consideration in active networks: Stability Considerations, Gain Considerations and Noise Considerations.

Module -4 RF/Microwave Amplifiers: Small Signal Design: Introduction, Types of amplifier, Design of different types of amplifiers
RF/Microwave Frequency Conversion: Mixers: Introduction, Mixer Types, Conversion Losses for SSB Mixers, SSB versus DSB mixers, One diode mixers, Two diode Mixers.

Module -5 RF/Microwave Control Circuit Design: Introduction, PN Junction Devices, Phase shifters, Digital phase shifters, Semiconductor phase shifters, PIN diode attenuators.
RF and Microwave IC design: MICs, MIC materials, Types of MICs, Hybrid verses Monolithic ICs, Chip mathematics

Question paper pattern:

- The question paper will have ten questions.
- Each full question consists of 20 marks.
- There will be 2 full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub questions covering all the topics under a module.
- The students will have to answer 5 full questions, selecting one full question from each module.

Text Book:

1. Matthew M. Radmanesh, "RF and Microwave Electronics Illustrated", Pearson Education edition, 2004.

Reference Book:

1. Reinhold Ludwig, and Pavel Bretchko, "RF circuit design theory and applications", Pearson Education edition, 2004.

Visvesvaraya Technological University, Belagavi.

PhD Coursework Courses – 2018 (Electronics and Communication Engineering)

As per 2017 Regulation

03	16ESP41	Group-6	Adaptive Signal Processing
Exam Hours:03		**Exam Marks:100**	

Module -1 Adaptive systems : Definitions and characteristics - applications - properties-examples - adaptive linear combiner input signal and weight vectors - performance function-gradient and minimum mean square error - introduction to filtering-smoothing and prediction - linear optimum filtering-orthogonality – WienerHopf equation- Performance Surface. (Text 1)

Module -2 Searching performance surface-stability and rate of convergence: learning curve-gradient search - Newton's method - method of steepest descent - comparison - gradient estimation - performance penalty - variance - excess MSE and time constants – misadjustments. (Text 1)

Module -3 LMS algorithm convergence of weight vector: LMS/Newton algorithm - properties - sequential regression algorithm – adaptive recursive filters - random-search algorithms - lattice structure - adaptive filters with orthogonal signals. (Text 1)

Module -4 Applications-adaptive modeling: Multipath communication channel, geophysical exploration, FIR digital filter synthesis. (Text 2)

Module -5 System identification-adaptive modeling: Inverse adaptive modeling, equalization, and deconvolution adaptive equalization of telephone channels-adapting poles and zeros for IIR digital filter synthesis. (Text 2)

Question paper pattern:

- The question paper will have ten questions.
- Each full question consists of 20 marks.
- There will be 2 full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub questions covering all the topics under a module.
- The students will have to answer 5 full questions, selecting one full question from each module.

Text Books:

1 Simon Haykin, “Adaptive Filter Theory”, Pearson Education, 2003.

2 Bernard Widrow and Samuel D. Stearns, “Adaptive Signal Processing”, Person Education, 2005.

Reference Books:

1. John R.Treichler, C.Richard Johnson, Michael G.Larimore, “Theory and Design of Adaptive Filters”, Prentice-Hall of India,2002

2. S.Thomas Alexander, “Adaptive Signal Processing-Theory and Application”, Springer-Verlag.

3. D. G. Manolokis, V. K. Ingle and S. M. Kogar, “Statistical and Adaptive Signal Processing”, McGraw Hill International Edition, 2000.

Visvesvaraya Technological University, Belagavi.
PhD Coursework Courses – 2018 (Electronics and Communication Engineering)
As per 2017 Regulation

04	16ESP152	Group-6	Multirate Systems and Filter Banks
Exam Hours:03		**Exam Marks:100**	
Module -1 Fundamentals of Multi-rate Systems: Basic multi-rate operations, interconnection of building blocks, poly-phase representation, multistage implementation, applications of multi-rate systems, special filters and filter banks (Text 1).			
Module -2 Maximally decimated filter banks: Errors created in the QMF bank, alias-free QMF system, power symmetric QMF banks, M-channel filter banks, poly-phase representation, perfect reconstruction systems, alias-free filter banks, tree structured filter banks, trans-multiplexers (Text 1).			
Module -3 Para-unitary Perfect Reconstruction Filter Banks: Lossless transfer matrices, filter bank properties induced by para-unitariness, two channel Para-unitary lattices, M-channel FIR Para-unitary QMF banks, transform coding (Text 1).			
Module -4 Linear Phase Perfect Reconstruction QMF Banks: Necessary conditions, lattice structures for linear phase FIR PR QMF banks, formal synthesis of linear phase FIR PR QMF lattice (Text 1). Cosine Modulated Filter Banks: Pseudo-QMF bank and its design, efficient poly-phase structures, properties of cosine matrices, cosine modulated perfect reconstruction systems (Text 1).			
Module -5 Wavelet Transform: Short-time Fourier transform, Wavelet transform, discrete-time Ortho-normal wavelets, continuous time Ortho-normal wavelets (Text 2).			
Question paper pattern: • The question paper will have ten questions. • Each full question consists of 20 marks. • There will be 2 full questions (with a maximum of four sub questions) from each module. • Each full question will have sub questions covering all the topics under a module. • The students will have to answer 5 full questions, selecting one full question from each module.			
Text Books: 1. P.P.Vaidyanathan,―MultirateSystemsandFilterBanks",PearsonEducation(Asia)Pte.Ltd,2004. 2. Gilbert Strang and Truong Nguyen, "Wavelets and Filter Banks", Wellesley-Cambridge Press, 1996. **Reference Book:** 1. N. J. Fliege, "Multirate Digital Signal Processing‖, John Wiley & Sons, USA,2000.			

Visvesvaraya Technological University, Belagavi.

PhD Coursework Courses – 2018 (Electronics and Communication Engineering)

As per 2017 Regulation

05	16ESP153	Group-6	MODERN SPECTRAL ANALYSIS & ESTIMATION

Exam Hours:03	Exam Marks:100

Module -1 Basic Concepts: Introduction, Energy Spectral Density of deterministic signals, Power Spectral Density of random signals, properties of Power Spectral Densities, The Spectral Estimation problem, Coherence Spectrum (Text 1).

Module -2 Spectrum Estimation: Introduction, Correlogram method, Periodogram Computation of FFT, properties of Periodogram method such as bias analysis, window design considerations. Signals with Rational spectra. ARMA state – space Equation, sub space Parameter Estimation (Text 1).

Module -3 Parametric Methods for line Spectra: Models of sinusoidal Signals in Noise, Non-linear least squares method. High Order Yule Walker method, Min – Norm Method, ESPRIT Method, Forward – Backward Estimation (Text 1).

Module -4 Filter Bank Method: Filter bank Interpretation of the period gram, Refined Filter bank Method, Capon Method, Filter Bank Reinterpretation of the periodogram (Text 1).

Module -5 Optimum Linear Filter : Optimum Signal Estimation, Linear MSE Estimation, Solution of the normal equations optimum FIR and IIR filters. Inverse filtering and deconvolution (Text 2).

Question paper pattern:

- The question paper will have ten questions.
- Each full question consists of 20 marks.
- There will be 2 full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub questions covering all the topics under a module.
- The students will have to answer 5 full questions, selecting one full question from each module.

Text Books:

1. Stoica and Moses, ―Introduction to Spectral Analysis‖, PHI, 1997.
2. Monalakis,IngleandKogen,―StatisticalandAdaptiveSignalProcessing‖, Tata McGraw Hill, 2000.

Visvesvaraya Technological University, Belagavi.
PhD Coursework Courses – 2018 (Electronics and Communication Engineering)
As per 2017 Regulation

06	16ECS423	Group-6	Communication System Design using DSP Algorithms
Exam Hours:03		**Exam Marks:100**	

Module -1 Introduction to the course: Digital filters, Discrete time convolution and frequency responses, FIR filters - Using circular buffers to implement FIR filters in C and using DSP hardware, Interfacing C and assembly functions, Linear assembly code and the assembly optimizer. IIR filters - realization and implementation, FFT and power spectrum estimation: DTFT window function, DFT and IDFT, FFT, Using FFT to implement power spectrum.

Module -2. **Analog modulation scheme:** Amplitude Modulation - Theory, generation and demodulation of AM, Spectrum of AM signal. Envelope detection and square law detection. Hilbert transform and complex envelope, DSP implementation of amplitude modulation and demodulation.
DSBSC: Theory generation of DSBSC, Demodulation, and demodulation using coherent detection and Costas loop. Implementation of DSBSC using DSP hardware.
SSB: Theory, SSB modulators, Coherent demodulator, Frequency translation, Implementation using DSP hardware. (Text 1, 2)

Module -3Frequency modulation: Theory, Single tone FM, Narrow band FM, FM bandwidth, FM demodulation, Discrimination and PLL methods, Implementation using DSP hardware.
Digital Modulation scheme: PRBS, and data scramblers: Generation of PRBS, Self -synchronizing data scramblers, Implementation of PRBS and data scramblers. RS-232C protocol and BER tester: The protocol, error rate for binary signaling on the Gaussian noise channels, Three bit error rate tester and implementation.

Module -4 PAM and QAM: PAM theory, baseband pulse shaping and ISI, Implementation of transmit filter and interpolation filter bank. Simulation and theoretical exercises for PAM, Hardware exercises for PAM.
QAM fundamentals: Basic QAM transmitter, 2 constellation examples, QAM structures using passband shaping filters, Ideal QAM demodulation, QAM experiment. QAM receivers-Clock recovery and other frontend sub-systems. Equalizers and carrier recovery systems.

Module -5 Experiment for QAM receiver frontend. Adaptive equalizer, Phase splitting, Fractionally spaced equalizer. Decision directed carrier tracking, Blind equalization, Complex cross coupled equalizer and carrier tracking experiment. Echo cancellation for full duplex modems: Multicarrier modulation, ADSL architecture, Components of simplified ADSL transmitter, A simplified ADSL receiver, Implementing simple ADSL Transmitter and Receiver.

Question paper pattern:

- The question paper will have ten questions.
- Each full question consists of 20 marks.
- There will be 2 full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub questions covering all the topics under a module.
- The students will have to answer 5 full questions, selecting one full question from each module.

Text Book:

Tretter, Steven A., "**Communication System Design Using DSP Algorithms With Laboratory Experiments for the TMS320C6713™ DSK",** Springer USA, *2008.*

Reference Books:

1. Robert. O. Cristi, **"Modern Digital signal processing",** Cengage Publishers, India, 2003.
2. S. K. Mitra, **"Digital signal processing: A computer based approach",** 3rd edition, TMH, India, 2007.
3. E.C. Ifeachor, and B. W. Jarvis, **"Digital signal processing: A Practitioner's approach",** Second Edition, Pearson Education, India, 2002,
4. Proakis, and Manolakis, **"Digital signal processing"**, 3rd edition, Prentice Hall, 1996.

Visvesvaraya Technological University, Belagavi.
PhD Coursework Courses – 2018 (Electronics and Communication Engineering)
As per 2017 Regulation

07	16ECS154	Group-6	SIMULATION, MODELLING AND ANALYSIS
Exam Hours:03		**Exam Marks:100**	

Module -1 Basic Simulation Modeling:
Nature of simulation, Systems, Models and Simulation, Discrete-Event Simulation, Simulation of Single Server Queuing System, Simulation of inventory system, Parallel and distributed simulation and the high level architecture, Steps in sound simulation study, and Other types of simulation, Advantages and disadvantages.
(1.1, 1.2, 1.3, 1.4, 1.4.1, 1.4.2, 1.4.3, 1.5, 1.5.1, 1.5.2, 1.6, 1.7, 1.8, 1.9 of Text)

Module -2Review of Basic Probability and Statistics
Random Variables and their properties, Simulation Output Data and Stochastic Processes, Estimation of Means, Variances and Correlations, Confidence Intervals and Hypothesis tests for the Mean
Building valid, credible and appropriately detailed simulation models: Introduction and definitions, Guidelines for determining the level of models detail, Management's Role in the Simulation Process, Techniques for increasing model validity and credibility, Statistical procedure for comparing the real world observations and simulation output data.
(4.2, 4.3, 4.4, 4.5, 5.1, 5.2, 5.4, 5.5, 5.6, 5.6.1, 5.6.2 of Text)

Module -3Selecting Input Probability Distributions:
Useful probability distributions, activity I, II and III. Shifted and truncated distributions; Specifying multivariate distribution, correlations, and stochastic processes; Selecting the distribution in the absence of data, Models of arrival process. (6.2, 6.4, 6.5, 6.6, 6.8, 6.10, 6.11, 6.12 of Text).

Module -4 Random Number Generators:
Linear congruential Generators, Other kinds, Testing number generators,
Generating the Random Variates:
General approaches, Generating continuous random variates, Generating discrete random variates, Generating random vectors, and correlated random variants, Generating arrival processes (7.2, 7.3, 7.4, 8.2, 8.3, 8.4, 8.5, 8.6 of Text).

Module -5 Output data analysis for a single system:
Transient and steady state behavior of a stochastic process; Types of simulations with regard to analysis; Statistical analysis for terminating simulation; Statistical analysis for steady state parameters; Statistical analysis for steady state cycle parameters; Multiple measures of performance, Time plots of important variables.
(9.2, 9.3, 9.4, 9.4.1, 9.4.3, 9.5, 9.5.1, 9.5.2, 9.5.3, 9.6, 9.7, 9.8 of Text)

Question paper pattern:

- The question paper will have ten questions.
- Each full question consists of 20 marks.
- There will be 2 full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub questions covering all the topics under a module.
- The students will have to answer 5 full questions, selecting one full question from each module.

Text Book:

1. Averill Law, "Simulation modeling and analysis", McGraw Hill 4th edition, 2007.

Reference Books:

1. Tayfur Altiok and Benjamin Melamed, "Simulation modeling and analysis with ARENA", Elsevier, Academic press, 2007.
2. Jerry Banks, "Discrete event system Simulation", Pearson, 2009
3. Seila Ceric and Tadikamalla, "Applied simulation modeling", Cengage, 2009.
4. George. S. Fishman, "Discrete event simulation", Springer, 2001.
5. Frank L. Severance, "System modeling and simulation", Wiley, 2009.

Visvesvaraya Technological University, Belagavi.

PhD Coursework Courses – 2018 (Electronics and Communication Engineering)

As per 2017 Regulation

08	16EVE22	Group-6	VLSI Testing
Exam Hours:03		**Exam Marks:100**	

Module -1 Faults in digital circuits: Failures and Faults, Modeling of faults, Temporary Faults. (Text 1)
Logic Simulation: Applications, Problems in simulation based design verification, types of simulation, The unknown logic values, compiled simulation, event-driven simulation, Delay models, Element evaluation, Hazard detection, Gate-level event-driven Simulation. (Text 2)

Module -2Test generation for Combinational Logic circuits: Fault Diagnosis of digital circuits, Test generation techniques for combinational circuits, Detection of multiple faults in Combinational logic circuits. (Text 1)
Testable Combinational logic circuit design: The Read-Muller expansion technique, Three level OR-AND-OR design, Automatic synthesis of testable logic.(Text 1)

Module -3Testable Combinational logic circuit design: Testable design of multilevel combinational circuits, Synthesis of random pattern testable combinational circuits, Path delay fault testable combinational logic design, Testable PLA design. (Text 1)
Test generation for Sequential circuits: Testing of sequential circuits as Iterative combinational circuits, state table verification, Test generation based on Circuit Structure, Functional Fault models, test Generation based on Functional Fault models. (Text 1)

Module -4 Design of testable sequential circuits: Controllability and observability, Ad-Hoc design rules for improving testability, design of diagnosable sequential circuits, the scan-path technique for testable sequential circuit design, Level Sensitive Scan Design(LSSD), Random Access Scan Technique, Partial scan, testable sequential circuit design using Nonscan Techniques, Cross check, Boundary Scan. (Text 1)

Module -5 Built-In Self Test: Test pattern generation for BIST, Output response analysis, Circular BIST, BIST Architectures. (Text 1)
Testable Memory Design: RAM Fault Models, Test algorithms for RAMs, Detection of pattern-sensitive faults, BIST techniques for RAM chips, Test generation and BIST for embedded RAMs. (Text1)

Question paper pattern:

- The question paper will have ten questions.
- Each full question consists of 20 marks.
- There will be 2 full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub questions covering all the topics under a module.
- The students will have to answer 5 full questions, selecting one full question from each module.

Text Books:

1. Lala Parag K., Digital Circuit Testing and Testability, New York, Academic Press, 1997.
2. Abramovici M, Breuer M A and Friedman A D, ―Digital Systems Testing and Testable Design‖, Wiley, 1994.

Reference Books:

1. Vishwani D Agarwal, ―Essential of Electronic Testing for Digital, Memory and Mixed Signal Circuits‖, Springer, 2002.
2. Wang, Wu and Wen, ―VLSI Test Principles and Architectures‖, Morgan Kaufmann, 2006.

Visvesvaraya Technological University, Belagavi.

PhD Coursework Courses – 2018 (Electronics and Communication Engineering)

As per 2017 Regulation

09	16EVE254	Group-6	SoC Design
Exam Hours:03		**Exam Marks:100**	

Module -1 ARM Organization and Implementation:3-stage pipeline ARM organization, 5-stage pipeline ARM organization, ARM instruction execution, ARM implementation, The ARM coprocessor interface.

The ARM Instruction Set : Introduction, Exceptions, Conditional execution, Branch and Branch with Link (B, BL),Branch, Branch with Link and eXchange (BX, BLX),Software Interrupt (SWI),Data processing instructions, Multiply instructions, Count leading zeros (CLZ - architecture v5T only), Single word and unsigned byte data transfer instruction, Half-word and signed byte data transfer instructions ,Multiple register transfer instructions, Swap memory and register instructions (SWP), Status register to general register transfer instructions , General register to status register transfer instructions, Coprocessor instructions, Coprocessor data operations, Coprocessor data transfers, Coprocessor register transfers, Breakpoint instruction (BRK - architecture v5T only), Unused instruction space, Memory faults, ARM architecture variants.

Module -2Architectural Support for High-Level Languages: Abstraction in software design, Data types, Floating-point data types, The ARM floating-point architecture, Expressions, Conditional statements, Loops, Functions and procedures, Use of memory, Run-time environment.

Architectural Support for System Development: The ARM memory interface, The Advanced Microcontroller Bus Architecture (AMBA), The ARM reference peripheral specification, Hardware system prototyping tools, The ARMulator, The JTAG boundary scan test architecture, The ARM debug architecture, Embedded Trace, Signal processing support.

Module -3ARM Processor Cores: ARM7TDMI, ARM8,ARM9TDMI, ARM10TDMI ,Discussion ,Example and exercises.

Memory Hierarchy: Memory size and speed, On-chip memory, Caches, Cache design - an example, Memory management, Examples and exercises.

Module -4 Architectural Support for Operating Systems: An introduction to operating systems, The ARM system control coprocessor, CP15 protection unit registers, ARM protection unit,CP15 MMU registers, ARM MMU architecture, Synchronization, Context switching, Input/ Output, Example and exercises.

ARM CPU Cores: The ARM710T, ARM720T and ARM740T, The ARM810,The Strong ARM SA-110,The ARM920T and ARM940T,The ARM946E-S and ARM966E-S,The ARM1020E,Discussion,Example and exercises.

Module -5 Embedded ARM Applications: The VLSI Ruby II Advanced Communication Processor, The VLSI ISDN Subscriber Processor, The One C™ VWS22100 GSM chip, The Ericsson-VLSI Bluetooth Baseband Controller, The ARM7500 and ARM7500FE, The ARM7100 364,The SA-1100 368,Examples and exercises.

The AMULET Asynchronous ARM Processors: Self-timed design 375,AMULET1 377,AMULET2 381,AMULET2e 384,AMULET3 387,The DRACO telecommunications controller 390, A self-timed future? 396,Example and exercises.

Question paper pattern:

- The question paper will have ten questions.
- Each full question consists of 20 marks.
- There will be 2 full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub questions covering all the topics under a module.
- The students will have to answer 5 full questions, selecting one full question from each module.

Text Book:

1. Steve Furber, ―ARM System-On-Chip Architecture‖, Addison Wesley, 2nd edition.

References Books:

1. Joseph Yiu, ―The Definitive Guide to the ARM Cortex-M3‖, 2nd edn, Newnes, (Elsevier), 2010.

2. Sudeep Pasricha and Nikil Dutt, "On-Chip Communication Architectures: System on Chip Interconnect‖, Morgan Kaufmann, Publishers © 2008.

3. Michael Keating, Pierre Bricaud, ―Reuse Methodology Manual for System on Chip designs , Kluwer Accademic Publishers, 2nd edition, 2008.

Visvesvaraya Technological University, Belagavi.

PhD Coursework Courses – 2018 (Electronics and Communication Engineering)

As per 2017 Regulation

10	16EVE423	Group-6	High Speed VLSI Design
Exam Hours:03		**Exam Marks:100**	

Module -1 Process Variability: Introduction**,** Front-end -of-line variability considerations, charge loss mechanisms, back-end-of- line variability considerations.

Module -2Non-Clocked logic styles: Introduction, static CMOS structures, DC VS logic, Non-clocked pass-gate families.

Clocked logic styles: Introduction, single-rail domino logic styles. Dual-rail domino structures, latched domino structures, clockedpass gate logic.

Module -3Circuit Design margin and design variability:

Introduction, process induced variation, design induced variations, and application induced variations‘, Noise.

Latching Strategies: Introduction, basic latch design, latching single ended logic, latching differential logic, race-free latched for pre-charge logic.

Module -4Interface Techniques:

Introduction, signaling standard, chip-chip communication networks, ESD protection, Driver design techniques, receiver design techniques.

Module -5 Clocking styles: Introduction, clock jitter and skew, clock generation and clock distribution.

Question paper pattern:

- The question paper will have ten questions.
- Each full question consists of 20 marks.
- There will be 2 full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub questions covering all the topics under a module.
- The students will have to answer 5 full questions, selecting one full question from each module.

Text Book:

Kerry Bernstein & et. Al., **—High Speed CMOS Design Styles”**, Kluwer, 1999. **Reference Books**:

1. Howard Johnson & Martin Graham, **“High Speed Digital Design”** A Handbook of Black Magic, Prentice Hall PTR, 1993.
2. William S. Dally & John W. Poulton, **“Digital Systems Engineering”**, Cambridge University Press, 1998.
3. Masakazu Shoji, **“High Speed Digital Circuits”**, Addison Wesley Publishing Company, 1996.

Visvesvaraya Technological University, Belagavi.
PhD Coursework Courses – 2018 (Electronics and Communication Engineering)
As per 2017 Regulation

11	16EVE421	Group-6	CMOS RF Circuit Design
Exam Hours:03		**Exam Marks:100**	
Module -1 Introduction to RF Design and Wireless Technology: **Basic concepts in RF design(I):** General considerations, Effects of Nonlinearity, Noise, Sensitivity and dynamic range.			
Module -2Basic concepts in RF design (II): Passive impedance transformation, scattering parameters, analysis of nonlinear dynamic systems.			
Module -3Communication Concepts: General concepts, analog modulation, digital modulation, spectral re-growth, Mobile RF communications, Multiple access techniques, Wireless standards.			
Module -4 Transceiver Architecture(I): General considerations, Receiver architecture.			
Module -5 ransceiver Architecture(II): Transmitter architectures **Low Noise Amplifiers:** LNA topologies: common-source stage with inductive load, common-source stage with resistive feedback. **Mixers:** General considerations, passive down conversion mixers.			
Question paper pattern: • The question paper will have ten questions. • Each full question consists of 20 marks. • There will be 2 full questions (with a maximum of four sub questions) from each module. • Each full question will have sub questions covering all the topics under a module. • The students will have to answer 5 full questions, selecting one full question from each module.			
Text Book: B. Razavi, **—RF Microelectronics‖**, PHI, second edition. **Reference Books**: 1. R. Jacob Baker, H.W. Li, D.E. Boyce **—CMOS Circuit Design, layout and Simulation‖**, PHI 1998. 2. Thomas H. Lee **—Design of CMOS RF Integrated Circuits‖** Cambridge University press 1998. 3. Y.P. Tsividis, **—Mixed Analog and Digital Devices and Technology‖**, TMH 1996			

Visvesvaraya Technological University, Belagavi.
PhD Coursework Courses – 2018 (Electronics and Communication Engineering)
As per 2017 Regulation

12	16EVE252	Group-6	VLSI Design for Signal Processing
Exam Hours:03		**Exam Marks:100**	

Module -1 Introduction to DSP Systems: Typical DSP Algorithms, DSP Application Demands and Scaled CMOS Technologies, Representations of DSP Algorithms.
Iteration Bounds: Data flow graph Representations, loop bound and Iteration bound.

Module -2Iteration Bounds: Algorithms for Computing Iteration Bound, Iteration Bound of multi rate data flow graphs.
Pipelining and Parallel Processing: pipelining of FIR Digital Filters, parallel processing, Pipelining and parallel processing for low power.

Module -3Retiming: Definition and Properties, Solving Systems of Inequalities, Retiming Techniques,
Unfolding: An Algorithm for Unfolding, Properties of Unfolding, Critical path, Unfolding and Retiming, Application of Unfolding.
Systolic Architecture Design: systolic array design Methodology, FIR systolic array.

Module -4 Systolic Architecture Design: Selection of Scheduling Vector, Matrix-Matrix Multiplication and 2D systolic Array Design, Systolic Design for space epresentation containing Delays.
Fast convolution: Cook-Toom Algorithm, Winograd Algorithm, Iterated convolution, cyclic convolution Design of fast convolution Algorithm by Inspection.

Module -5 Pipelined and Parallel Recursive and Adaptive Filter: Pipeline Interleaving in Digital Filter, first order IIR digital Filter, Higher order IIR digital Filter, parallel processing for IIR filter, Combined pipelining and parallel processing for IIR Filter, Low power IIR Filter Design Using Pipelining and parallel processing, pipelined adaptive digital filter.

Question paper pattern:

- The question paper will have ten questions.
- Each full question consists of 20 marks.
- There will be 2 full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub questions covering all the topics under a module.
- The students will have to answer 5 full questions, selecting one full question from each module.

Text Book:

1. Keshab K.Parthi, "VLSI Digital Signal Processing systems, Design and implementation ", Wiley 1999.

Reference Books:

1. Mohammed Isamail and Terri Fiez, "Analog VLSI Signal and Information Processing ", Mc Graw-Hill,1994.
2. S.Y. Kung, H.J. White House, T. Kailath, " VLSI and Modern Signal Processing ", Prentice Hall, 1985.
3. Jose E. France, Yannis Tsividis, " Design of Analog - Digital VLSI Circuits for Telecommunication and Signal Processing ", Prentice Hall, 1994.
4. Lars Wanhammar, ―DSP Integrated Circuits‖, Academic Press Series in Engineering, 1st Edition.

Visvesvaraya Technological University, Belagavi.
PhD Coursework Courses – 2018 (Electronics and Communication Engineering)
As per 2017 Regulation

13	16EIE423	Group-6	Medical Imaging
Exam Hours:03		**Exam Marks:100**	

Module -1 Generation and Detection of X-Rays: X-Ray generation and X-Ray generators, Filters, Beam Restrictors and Grids, Screens, X-Ray Detectors.
X-Ray Diagnostic Methods: Conventional X-Ray Radiography, Fluoroscopy, Angiography, Mammography, Xeroradiography, Image Subtraction.
X-Ray Image Characteristics: Spatial Resolution, Image Noise, Image contrast.
Biological Effects of Ionizing Radiation: Determination of biological effects, Short term and Long term effects.

Module -2X-Ray Tomography: Conventional Tomography, Computed Tomography - Projection function, Algorithms for Image Reconstruction, CT number, Image Artifacts.
Digital Radiography: Digital Subtraction Angiography (DSA), Dual Energy Subtraction, K-Edge subtraction, 3-D Reconstruction.
Recent Developments: Dynamic Spatial Reconstructor (DSR), Imatron or Fastrac Electron Beam CT.

Module -3Generation and Detection of Ultrasound: Piezoelectric effect, Ultrasonic Transducers, Transducer Beam Characteristics, Axial and Lateral resolution, Focussing and Arrays.
Ultrasonic Diagnostic Methods: Pulse Echo systems - A mode, B mode, M mode and C mode, Transmission Methods, Doppler methods, Duplex Imaging
Biological Effects of Ultrasound: Acoustic phenomena at high intensity levels, Ultrasound Bioeffects.

Module -4 Generation and Detection of Nuclear Emission: Nuclear Sources, Radionuclide Generators, Nuclear Radiation Detectors, Collimators.
Diagnostic methods using Radiation Detector Probes: Thyroid Function test, Renal function test, Blood volume measurement.
New Radio Nuclide Imaging methods: Longitudinal Section Tomography, SPECT and PET
Characteristics of Radionuclide Images: Spatial Resolution, Image contrast, Image Noise.

Module -5 Generation and Detection of NMR signal: The NMR Coil/Probe, The transmitter and the Receiver, Data acquisition.
Magnetic Resonance Imaging methods: Spin Echo Imaging, Gradient Echo Imaging, Blood flow Imaging.
Characteristics of MRI images: Spatial Resolution, Image Contrast. **Imaging Safety.**

Question paper pattern:

- The question paper will have ten questions.
- Each full question consists of 20 marks.
- There will be 2 full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub questions covering all the topics under a module.
- The students will have to answer 5 full questions, selecting one full question from each module.

Text Book:
Kirk Shung, Michael B, Smith, Benjamin M W Tsui, "Principles of Medical Imaging", Academic Press, 2012.
Reference Books:
1. Zhong Hicho and Manbir Singh **"Fundamentals of Medical Imaging"**, John Wiley, 1993.
2. Peter Josefell & Edward Sudney **"Nuclear Medicine Introductory Text"**, William Blackwell Scientific Publishers, London.

Visvesvaraya Technological University, Belagavi.

PhD Coursework Courses – 2018 (Electronics and Communication Engineering)

As per 2017 Regulation

14	16EIE421	Group-6	Advanced Power Electronic Converters and Applications

Exam Hours:03 **Exam Marks:100**

Module -1 Introduction to power electronics: Introduction to Power Processing, Several Applications of Power Electronics, Elements of Power Electronics.

Principles of Steady State Converter Analysis: Inductor Volt- Second Balance, Capacitor Charge Balance, and the Small-Ripple Approximation, Boost Converter Example, Cuk Converter Example Estimating the Output voltage ripple and inductor current ripple in converters Containing Two-Pole Low-Pass Filter. (Text 1)

Module -2Converter Dynamics and Control: AC Equivalent Circuit Modeling, The Basic AC Modeling Approach, State-Space Averaging, Circuit Averaging and Averaged Switch Modeling, The Canonical Circuit Model, Modeling the Pulse-Width Modulator, Analysis of Converter Transfer Functions, Graphical Construction of Impedances and Transfer Functions(Text 1)

Module -3 Controller Design: Introduction, Effect of Negative Feedback on the Network Transfer Functions, Construction of the Important Quantities 1/(1 + T) and T/(1 + T) and the Closed-Loop Transfer Functions, Stability, The Phase Margin Test, The Relationship Between Phase Margin and Closed-Loop Damping Factor, Transient Response vs. Damping Factor, Regulator Design, Measurement of Loop Gains. (Text 1)

Module -4 Modern Rectifiers and Power System Harmonics: Power and Harmonics in Nonsinusoidal Systems, Pulse-Width Modulated Rectifiers.

Resonant Converters: Sinusoidal Analysis of Resonant Converters with examples (Text 1)

Module -5 Power supply applications: Switching DC Power Supplies, Motor drive applications: Introduction to Motor Drives, DC-Motor Drives, Residential and Industrial Applications, Electric Utility Applications (Text 2)

Question paper pattern:

- The question paper will have ten questions.
- Each full question consists of 20 marks.
- There will be 2 full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub questions covering all the topics under a module.
- The students will have to answer 5 full questions, selecting one full question from each module.

Text Books:

1. Erickson and Maksimovic, "**Fundamentals of Power Electronics**", 2nd Edition, Kluwer Academic Publishers, 2001,
2. M.NedMohan, Tore. Undeland and William.P.Robbins, **—Power Electronics converters, Applications and Design‖**, John Wiley and Sons, 3rd Edition, 2002.

Reference Books:

1. Abraham Pressman, **—Switching Power Supply Design‖**, McGraw-Hill Publishers, 1998.
2. Muhammad H. Rashid, "**Power Electronics Handbook**", 2nd Edition, Academic Press, 2007.

Visvesvaraya Technological University, Belagavi.

PhD Coursework Courses – 2018 (Electronics and Communication Engineering)

As per 2017 Regulation

15	16ELD11	Group-6	ADVANCED ENGINEERING MATHEMATICS

Exam Hours:03 **Exam Marks:100**

Module -1 Linear Algebra-I

Introduction to vector spaces and sub-spaces, definitions, illustrative examples and simple problems. Linearly independent and dependent vectors-definition and problems. Basis vectors, dimension of a vector space. Linear transformations- definition, properties and problems. Rank-Nullity theorem(without proof). Matrix form of linear transformations-Illustrative examples.**(Text 1 & Ref. 1)**

Module -2Linear Algebra-II

Computation of Eigen values and Eigen vectors of real symmetric matrices-Given's method. Orthogonal vectors and orthogonal bases. Gram-Schmidt orthogonalization process. QR decomposition, singular value decomposition, least square approximations.**(Text 1 & Ref. 1)**

Module -3Calculus of Variations

Concept of functional-Eulers equation. functional dependent on first and higher order derivatives, functional on several dependent variables. Isoperimetric problems-variation problems with moving boundaries.**(Text 2 & Ref. 2)**

Module -4 Probability Theory

Review of basic probability theory. Definitions of random variables and probability distributions, probability mass and density functions, expectation, moments, central moments, characteristic functions, probability generating and moment generating functions-illustrations. Binomial, Poisson, Exponential, Gaussian and Rayleigh distributions-examples.**(Text 3 & Ref. 3)**

Module -5 Joint probability distributions

Definition and properties of CDF, PDF, PMF, conditional distributions. Expectation, covariance and correlation. Independent random variables. Statement of central limit theorem-Illustrative examples.

Random process- Classification, stationary and ergodic random process. Auto correlation function-properties, Gaussian random process.**(Text 3 & Ref. 3)**

Question paper pattern:

- The question paper will have ten questions.
- Each full question consists of 20 marks.
- There will be 2 full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub questions covering all the topics under a module.
- The students will have to answer 5 full questions, selecting one full question from each module.

Text Books:

1. David C.Lay, Steven R.Lay and J.J.McDonald: Linear Algebra and its Applications, 5th Edition, Pearson Education Ltd., 2015.
2. E. Kreyszig, "Advanced Engineering Mathematics", 10th edition, Wiley, 2015.
3. Scott L.Miller, Donald G.Childers: "Probability and Random Process with application to Signal Processing", Elsevier Academic Press, 2ndEdition,2013.

Reference books:

1. Richard Bronson: "Schaum's Outlines of Theory and Problems of Matrix Operations", McGraw-Hill, 1988.
2. Elsgolts L.: "Differential Equations and Calculus of Variations", MIR Publications, 3rd Edition, 1977.
3. T.Veerarajan: "Probability, Statistics and Random Process", 3rd Edition, Tata McGraw Hill Co.,2008.