Model Question Paper-1 with effect from 2019-20 (CBCS Scheme)

USN | | | | | | | | | | |

Fourth Semester B.E. Degree Examination

Signal Conditioning and Data Acquisition Circuits

TIME: 03 Hours **Max. Marks: 100**

Note: 01. Answer any **FIVE** full questions, choosing at least **ONE** question from each **MODULE**.

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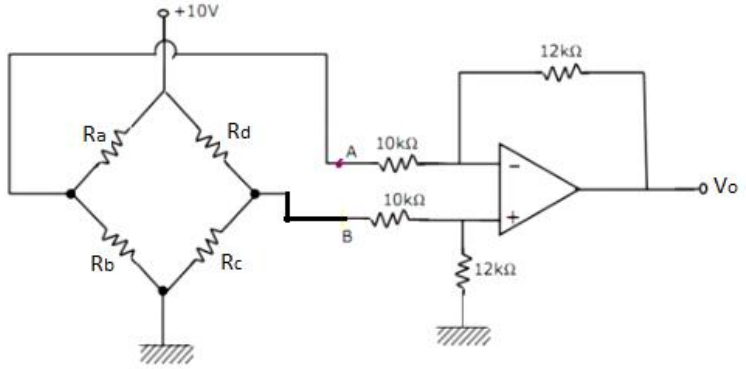
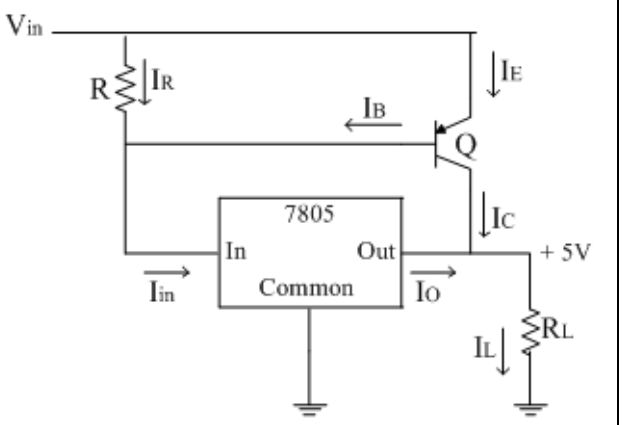
		Module -1	
Q.01	a	Draw the equivalent circuit of op-amp. Write the expression for V_o. Enumerate the characteristics of an ideal op-amp.	4
	b	 Fig 1(b) The circuit in Fig 1(b) uses an ideal op-amp. Calculate the output voltage V_o, when i) $R_a = R_b = R_c = R_d = 100\Omega$ ii) $R_a = R_b = R_c = 100\Omega$ and $R_d = 120\Omega$ Assume that the impedances at node A and B do not load the preceding bridge circuit.	8
	c	In an Inverting amplifier, $R_1 = 1\ k\Omega$, $R_f = 100\ k\Omega$, The op-amp specifications are $\Delta V_{ios}/\Delta T = 30\ \mu V/^oC$ and $\Delta I_{os}/\Delta T = 0.3\ nA/^oC$. Assume that the amplifier is nulled at 25^oC. Calculate the value of the error voltage and the output voltage V_o at 35^oC if input voltage i) $V_i = 1$ mV dc and ii) $V_i = 5$ mV dc.	8
		OR	
Q.02	a	Define Slew rate. An op-amp has a slew rate of 2V/μs. What is the maximum frequency of an output sinusoid of peak value 5V at which distortion sets in due to the slew rate limitation?	4
	b	Derive an equation for the output voltage V_o in case of an Inverting Summing amplifier circuit. Also, realize an inverting averaging circuit	8
	c	List the features of an Instrumentation Amplifier. Sketch the Instrumentation amplifier circuit and derive an equation for the overall closed loop voltage gain A_v.	8
		Module-2	
Q. 03	a	Describe the need for i) Voltage to Current conversion and ii) Current to Voltage conversion	4
	b	What is the use of a sample and hold circuit ? With a neat circuit diagram and voltage waveforms, explain the operation of the circuit. Also, define Hold time and Sampling time.	8
	c	State the limitations of a basic op-amp differentiator circuit. Draw the circuit of a practical differentiator and with a neat frequency response curve, illustrate how the practical circuit can overcome the limitations of a basic circuit.	8
		OR	
Q.04	a	Draw the transfer characteristic of an ideal comparator. The input to the non-inverting comparator is a sinusoidal input signal of $6V_{pp}$ and the reference voltage is 1V. The supply voltage is ±12V. Sketch the input and output waveforms of the comparator	4
	b	With necessary voltage waveforms, derive an expression for the frequency of the square wave output in case of an astable mutivibrator,	8
	c	State the conditions for sustained oscillations. Design a Phase shift oscillator for $f_o = 500$ Hz	8

		Module-3	
Q. 05	a	What is the function of a Voltage regulator? Distinguish between Series regulator and Switching regulator.	4
	b	 Fig5(b) In Fig.5(b), R = 7Ω, β = 15 and $V_{EB(on)}$ = 1V. For loads, 100 Ω and 5Ω, Calculate i) the output current I_o coming from IC 7805 ii) the collect current I_c of the transistor iii) the load current I_L	8
	c	Draw the circuit diagram of IC 723 low voltage regulator. With a neat functional diagram and voltage equations, explain the circuit operation.	8
		OR	
Q. 06	a	State the advantages of active filters over passive filters. Also, give the classification of Active filters	4
	b	With a neat circuit diagram and frequency response curve, deduce an expression for the magnitude of the first order low pass filter gain |H(jω)|. Verify the filter operation using |H(jω)|.	8
	c	Sketch the frequency response curve and circuit diagram of a wide band reject filter. Also, design the same filter having the cut off frequencies 400 Hz and 2 kHz and a pass band gain of 2.	8
		Module-4	
Q. 07	a	Give the pin diagram and mention the features of a 555 timer.	4
	b	With a neat circuit diagram, timing pulse waveforms and functional diagram, explain the working of a monostable multivibrator using 555 timer.	8
	c	Briefly explain the operation of the following 555 timer circuits operating in astable mode. i) FSK Generator ii) Pulse-position modulator.	8
		OR	
Q. 08	a	Show that the Phase detector is an A+nalog multiplier that multiplies the input signal by the VCO signal. Comment on the mathematical result.	4
	b	Give the block diagram of IC 566 VCO and explain its operation	8
	c	Draw the block diagram of the following circuits that use PLL: i) Frequency multiplier, and ii) Frequency translator Briefly explain the operation of each.	8
		Module-5	
Q. 09	a	List the components of Analog Data Acquisition system	4
	b	Draw the block diagram of Digital Data Acquisition system and explain the function of each block	8
	c	Describe the construction and working of recorders in digital systems	8
		OR	
Q. 10	a	Explain the following DAC/ADC specifications: i) Resolution, ii) Linearity	4
	b	Draw a 3-bit R-2R Ladder DAC circuit and perform circuit analysis to show that i) 1 MSB = $V_{FS}/2$ and ii) 1 LSB = $V_{FS}/8$	8
	c	With a neat circuit diagram and output waveform, explain the operation of a Dual slope ADC.	8