Schedule and Timing of the ONLINE WEBINARSERIES

| Sl. No. | Title of Webinar | Brief Description | Proposed Dates | Timings |
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| | **VLSI (ASIC - Concept to Chip Tapeout)** | | | |
| 1 | ASIC Design - Evolution, Current Trends, Career Opportunites & Research Avenues for Engineers | ASIC Design Methodologies - Full custom, Semicustom; Industry Demography- Product, OEM, Indian Design Houses ; Fab & Fabless companies, Product & IP Development industries; Industry evolution, Job opportunites and Skill demands | **4th Sep 2020** | **6pm – 8pm** |
| 2 | ASIC Front End Design and Verification | Architecture, Micro Architecture, Design Entry approaches, RTL Design & Simulation, Role of Functional Verification in ASIC flow, Verilog based Verification ; Design Entry, Functional Simulation and Analysis using Cadence Incisive Enterprise Simulator and Xcelium | **9th Sep 2020** | **6pm – 8pm** |
| 3 | Advanced Verification - SystemVerilog and UVM - Need and How to get started ? | Challenges and Limitations of HDL as Verification Langauge, SystemVerilog based Verification- Case study, UVM; SV & UVM based simulation of a case study usingg Cadence Incisive Enterprise Simulator & Xceilium | **11th Sep 2020** | **6pm – 8pm** |
| 4 | ASCI Logic Synthesis and Pre-Layout Timing Analysis | Synthesis and Simulation Mismatches in RTL Design - Guidelines for good design; RTL Synthesis using Cadence Genus | **15th Sep 2020** | **6pm – 8pm** |
| 5 | Role of Formal verification and Linting in ASIC Design flow | Role of Formal Verification & Linting in ASIC Design, How to perform Formal Verification and Linting Checks using Cadence Jasper | **18th Sep 2020** | **6pm – 8pm** |
| 6 | Design for Testability ( DFT) - Evolution and DFT Strategiy for designs | Importance of DFT, DFT Strategies for Designs - LBIST, MBIST, Scan & Insertion; How to run a basic DFT checks using Cadence Modus tool flow | **23rd Sep 2020** | **6pm – 8pm** |
| 7 | Physical Implementation flow in ASIC : Guidelines for SoC Designs | Synthesis and Pre-Layout Timing Signoffs, Physical Implementation flow for Industry grade SoC Designs, Guidelines & Best Practices in SoC Designs | **25th Sep 2020** | **6pm – 8pm** |
| 8 | Physical Design flow - Floor Plan, Power Plan - Industry perspective | Floor plan and Power Plan - Guidelines; Running Floor-plan and Power Plan for a given design using Cadence Innovus | **30th Sep 2020** | **6pm – 8pm** |
| 9 | Physical Design flow - Clock Tree Synthesis, P & R | Fundamentals of Clock Tree Synthesis; Automatic P & R - Algorithms in EDA Tools, Running CTS & P & R using Cadence Innovus, Tempus | **3rd Oct 2020** | **6pm – 8pm** |
| 10 | Timing & Power Signoffs in PD flow | Timing Sign offs using Cadence Tempus, Power Signoffs - Challenge in contemporary designs; Running Power Signoff using Cadence Voltus/Joules; ANSYS Redhawk flow | **7th Oct 2020** | **6pm – 8pm** |
| 11 | Physical Verification flow for SoC Designs | Physical Verification Signoffs - Common Signoff activities in Physical Verification, Running Physical Verification using Cadence PVS | **9th Oct 2020** | **6pm – 8pm** |

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| 12 | Custom IC Design - Approach and flow | Full Custom IC Design - Digital and Analog, Requirements and flow ; Cadence Virtuoso & Spectre features and capibilities , Need for Library Characterization and Cadence Liberate for Library Chracterization | **14th Oct 2020** | **6pm – 8pm** |
| 13 | Custom IC Design - Schematic and Layout Design and Analysis | Standard Cell Design - Industry practice; Schematic Design, Simulation & Analysis using Cadence Virtouso and Spectre | **16th Oct 2020** | **6pm – 8pm** |
| 14 | Building Fundamental Analog Blocks - Characterization, Schematic Design & Analysis | Building Analog Cells for SoC Designs ; Technology Nodes of Industry focus; Schematic Design, Simulation & Analysis using Cadence Virtuoso and Spectre | **21st Oct 2020** | **6pm – 8pm** |
| 15 | Analog & Mixed Signal Design & Simuluation | Analog & Mixed Signal Design - Guidelines and Design using Cadence Virtuoso Layout Editor and Layout Simulation using Spectre | **23rd Oct 2020** | **6pm – 8pm** |
| 16 | Concept to Silicon - How you can take your designs into fabrication? | Concept to Silicon- What, Why and How?; Can academia take their R & D work into Silicon/System Proof of Concept/Prototype, Support from Industry Echo System - Foundry Tie-up, Integrating PDK into the EDA Tool flow | **28th Oct 2020** | **6pm – 8pm** |
| **Electronic System Design Series** | | | | |
| 17 | Electronic System Design for Emerging Technologies - IoT, 5G and more | Electronic System Design - Evolution, Need of Modern Day Electronic System Design, Challenges and Opportunities | **3rd Sep 2020** | **6pm – 8pm** |
| 18 | Electronic Circuit Design and Analysis - Challenges and Solutions | Electronic System Design - Industrial Flow, Spec to Gerber - Detailed flow, Concept of Power/Timing Budget, BOM, Component Selection, Electronic Circuit Design and Simulation using OrCAD Pspice | **8th Sep 2020** | **6pm – 8pm** |
| 19 | Advanced Electronic System Design & Analysis | Electronic System Design beyond Hardware ; Advanced Analysis using OrCAD Pspice and PCB; Concept of Signal Integrity /Power Integrity - Pre and Post Layout Analysis using OrCAD PCB SI/Sigrity | **15th Sep 2020** | **6pm – 8pm** |
| 20 | Electronic System Design and Product Focus - How to give shape to your design ideas | Spec to an Electronic Product, Role of Mechanical Design in Electronic/IC Systems, Thermal Analysis (IC/System Level), PCB Prototyping and Product Proof of Concept; How you can support your industry echo system in your region ? | **22nd Sep 2020** | **6pm – 8pm** |