ವಿಶ್ವೇಶ್ವರಯ್ಯ ತಾಂತ್ರಿಕ ವಿಶ್ವವಿದ್ಯಾಲಯ
"ವಿಟಿಯು ಅಧಿನಿಯಮ ೧೯೯೪"ರ ಅಡಿಯಲ್ಲಿ ಕರ್ನಾಟಕ ಸರ್ಕಾರದಿಂದ ಸ್ಥಾಪಿತವಾದ ರಾಜ್ಯ ವಿಶ್ವವಿದ್ಯಾಲಯ
"ಜ್ಞಾನ ಸಂಗಮ", ಬೆಳಗಾವಿ-೫೯೦೦೧೮, ಕರ್ನಾಟಕ, ಭಾರತ

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Ref: VTU/BGM/BOS/A9/2020-21 /211

Date: 8 APR 2021

CIRCULAR

Subject: New Open Elective Subjects added to the existing list of B.E. in ECE/TCE program's Syllabus (2018 scheme) regarding.

Reference:

1. Chairperson BOS in ECE email dated 06.04.2021
2. Hon'ble Vice-Chancellor's approval dated 08.04.2021

Concerning the subject cited above, the OPEN Elective subjects are added to the existing list in the scheme and Syllabus of B.E. in Electronics & Communication Engineering and Electronics & Telecommunication Engineering programs. The complete list of subjects along with the syllabus of added subject is enclosed with this circular for kind reference to the concerned. And also uploaded on the VTU web portal **@ https://vtu.ac.in/en/category/administration-circulars/** and updated syllabus with addition open elective subjects **@ https://vtu.ac.in/en/b-e-scheme-syllabus/#menu0**

All the Principals of Engineering Colleges are hereby requested to inform the faculty of the ECE/TCE to counsel the students regarding the OPEN elective subjects.

Encl: As mentioned above

Sd/-
REGISTRAR

To,

- All the Principals of the Engineering Colleges under the ambit of VTU Belagavi.

Copy to:

1. The Registrar(Evaluation) for information and needful
2. The Registrar's Office, VTU, Belagavi, for information.
3. The Special Officer, Academic Section, VTU Belagavi, for information.
4. The Special Officer CNC section to upload the circular on the VTU web portal.

REGISTRAR

UG Programmes - 2018 Scheme & Syllabus

Purpose: **Additional Open Electives** offered by the Department of **Electronics and Communication Engineering (ECE) & Electronics and Telecommunication Engineering (TCE)**

VI Semester Open Elective A

Sl. No.	Course Code	Subject	Remarks
1	18EC651	Signal Processing	Existing
2	18EC652	Sensors & Signal Conditioning	Existing
3	**18EC653**	**Virtual Instrumentation**	Newly Added
4	**18EC654**	**Microcontrollers**	Newly Added
5	**18EC655**	**Basic VLSI Design**	Newly Added

VII Semester Open Elective B

Sl. No.	Course Code	Subject	Remarks
1	18EC751	Communication Theory	Existing
2	18EC752	Neural Networks	Existing
3	**18EC753**	**ARM Embedded Systems**	Newly Added
4	**18EC754**	**Digital Systems Design using VHDL**	Newly Added

ADDITIONAL OPEN ELECTIVES-A OFFERED BY EC/TC BOARD

B. E. EC/TE Choice Based Credit System (CBCS) and Outcome Based Education (OBE) SEMESTER – VI			
VIRTUAL INSTRUMENTATION			
Course Code	**18EC653**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**03**	**SEE Marks**	**60**
Total Number of Lecture Hours	**40(8Hours/Module)**	**Exam Hours**	**03**
CREDITS – 03			

Course objective: This course will enable students to:

- Understand the fundamental principles of virtual instrumentation
- Acquire, analyze and present data using LabVIEW

Module-1	RBT Level
Graphical System Design: Introduction, Graphical system design model, Design flow with GSD, Virtual Instrumentation, Virtual instrument and traditional instrument, Hardware and software in virtual instrumentation, Virtual instrumentation for Test, control & design, Graphical system design using LABVIEW, Graphical programming & textual programming.	**L1, L2, L3**
Module-2	
Introduction to LabVIEW: Introduction, advantages of LABVIEW software environment, palettes, front panel controls & indicators, Block diagram, Data flow program. **Repetition and Loops**: For loops, while loops, structure tunnels, terminals inside or outside loops, shift registers, feed-back nodes, control timing, case structure.	**L1, L2, L3**
Module-3	
Arrays: Introduction, arrays in LABVIEW, creating one - dimensional array controls, indicators and constants, creating two dimensional arrays, creating multidimensional arrays, initializing array, deleting, inserting, and replacing elements, rows, columns, and pages with in arrays, arrays functions.	**L1, L2, L3**
Module-4	
Plotting Data: Types of waveforms, waveform graphs, waveform charts, XY graphs, Intensity graphs & charts, Digital waveform graphs, 3D graphs, customizing graphs & charts, configuring a graph or chart, Displaying special planners on the XY graph.	**L1,L2, L3**
Module-5	
File Input/ Output: File formats, file write &read, generating filenames automatically, **String handling**: string functions, LABVIEW string formats, parsing of strings. **Instrument Control**: Introduction, GPIB communication, Hardware specification, software architecture, Instrument I/O assistant, VISA, Instrument drivers, serial port communications, using other interfaces.	**L1, L2, L3**

Course Outcomes: After studying this course, students will be able to:

1. Recognize the Graphical system design model and develop programs using the modern tools of Graphical programming & textual programming
2. Develop a virtual instrumentation model using the front panel controls & indicators and loops.
3. Analyze, design the various array and matrix operations using LabVIEW functions.
4. Evaluate the various forms of output representations using graphs & charts
5. Demonstrate Instrument Control, GPIB communication and other interfaces

Students have to conduct the following experiments as a part of CIE marks along with other Activities:

1. Build a VI code to indicate the change in temperature using LabVIEW
2. Develop a code in VI to convert 4-bit binary input to gray output using LabVIEW
3. Generate a VI code to display sinusoidal and triangular waveforms using LabVIEW
4. Build a code using LabVIEW to compute the sum of N numbers (use FOR loop)
5. Develop a VI code using LabVIEW to sort the even numbers (use while loop)
6. Using LabVIEW compute the basic operations of a simple calculator using case structure

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Books:

1. "Virtual Instrumentation using LABVIEW", Jovitha Jerome, PHI, 2010
2. "Virtual Instrumentation using LABVIEW", Sanjay Gupta, Joseph John, TMH, McGraw Hill Second Edition, 2011.

Reference:

"Learning with LabView", Robert H Bishop, Prentice Hall, 2009.

ADDITIONAL OPEN ELECTIVES-A OFFERED BY EC/TC BOARD

B. E. EC/TE
Choice Based Credit System (CBCS) and Outcome Based Education (OBE)
SEMESTER – VI

MICROCONTROLLERS

Course Code	**18EC654**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**03**	**SEE Marks**	**60**
Total Number of Lecture Hours	**40(8Hours/Module)**	**Exam Hours**	**03**

CREDITS – 03

Course objective: This course will enable students to:

- Learn architecture of 8051.
- Learn programming skills using Assembly language and C
- Design and interface microcontroller based embedded systems.
- Build projects

Module-1	**RBT Level**
Microprocessors and Microcontroller: Introduction, Microprocessors and Microcontrollers, Microcontroller Survey. (Text 1- Chapter 1) **The 8051 Architecture**: Introduction, Architecture of 8051, Pin diagram of 8051, Memory organization. (Text 1- Chapter 2)	**L1, L2**
Module-2	
Addressing Modes in 8051 Microcontroller: Introduction, Addressing Modes, External Data Moves, Code Memory Read only Data Moves, PUSH and POP opcodes, Data Exchanges, Example Programs. (Text 1- Chapter 3)	**L1, L2**
Module-3	
Instruction set: Instruction timings, 8051 instructions: Data transfer instructions, Arithmetic instructions, Logical instructions, Branch instructions, Subroutine instructions, Bit manipulation instruction. (Text 1- Chapter 4, 5 and 6)	**L1, L2, L3**
Module-4	
8051 Microcontroller Interfacing and Applications: Interfacing 8051 to LCD, Keyboard, parallel and serial ADC, DAC interfacing and programming. (Text 2 – Chapter 12 and 13)	**L1,L2, L3**
Module-5	
8051 Microcontroller Interrupts and Timers/counters: Basics of interrupts, 8051 interrupt structure, Timers and Counters, 8051 timers/counters, programming 8051 timers in assembly and C . (Text 2 – Chapter 9, Chapter 11 -11.1) **8051 Microcontroller Serial Communication**: Data communication, Basics of Serial Data Communication, 8051 Serial Communication, connections to RS-232, Serial communication Programming in assembly and C. (Text 2 – Chapter 10- 10.1,10.2, 10.3)	**L1, L2, L3**

Course Outcomes: After studying this course, students will be able to:

1. Explain the basics of Microprocessor and Microcontroller
2. Relate to the 8051 Microcontroller architecture and Pin description
3. Analyze 8051 Addressing modes and use the 8051 instruction set
4. Program the on-chip peripherals in 8051
5. Design and develop applications using 8051 Assembly language and C program

Students have to conduct the following experiments as a part of CIE marks along with other Activities:

1. Write an 8051 ALP to exchange n = 5 bytes of data at location 0027H and at location 0041H.
2. Write an 8051 ALP to sort an array of n = 6 bytes of data in ascending order stored from location 9000H.(use bubble sort algorithm)

3. Write an 8051 ALP to implement (display) an eight bit up/down binary (hex) counters on watch window.
4. Write a program to toggle all the bits of P1 and P2 continuously using CALL and RETURN instructions
5. Write an 8051 ALP to implement ASCII to hexadecimal conversion
6. Write a Program illustrating timer delay Generate a 1second delay continuously using the on-chip timer in interrupt mode.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Books:

1. "The 8051 Microcontroller Architecture, Programming and Applications", Kenneth J Ayala, Thomson learning, 2005.
2. "The 8051 Microcontroller and Embedded Systems-using Assembly and C", Muhammad Ali Mazidi and Janice Gillespie Mazidi and Rollin D McKinaly, Pearson, 2006.

Reference:

"The 8051 Microcontroller: Hardware, Software and Applications" V. Udayashankara and Mallikarjuna Swamy, TMH., 2009.

ADDITIONAL OPEN ELECTIVES-A OFFERED BY EC/TC BOARD

B. E. EC/TE Choice Based Credit System (CBCS) and Outcome Based Education (OBE) SEMESTER – VI			
BASIC VLSI DESIGN			
Course Code	**18EC655**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**03**	**SEE Marks**	**60**
Total Number of Lecture Hours	**40(8Hours/Module)**	**Exam Hours**	**03**
CREDITS – 03			

Course objective: This course will enable students to:

- Understand the fundamental aspects of circuits in silicon
- Relate to VLSI design processes and design rules

Module-1	RBT Level
Moore's law, speed power performance, nMOS fabrication, CMOS fabrication: n-well, p-well processes, BiCMOS, Comparison of bipolar and CMOS. **Basic Electrical Properties of MOS And BiCMOS Circuits**: Drain to source current versus voltage characteristics, threshold voltage, transconductance.	**L1, L2**
Module-2	
Basic Electrical Properties of MOS And BiCMOS Circuits: nMOS inverter, Determination of pull up to pull down ratio: nMOS inverter driven through one or more pass transistors, alternative forms of pull up, CMOS inverter, BiCMOS inverters, latch up. **Basic Circuit Concepts**: Sheet resistance, area capacitance calculation, Delay unit, inverter delay, estimation of CMOS inverter delay, super buffers, BiCMOS drivers.	**L1, L2**
Module-3	
MOS and BiCMOS Circuit Design Processes: MOS layers, stick diagrams, nMOS design style, CMOS design style **Design rules and layout & Scaling of MOS Circuits**: λ - based design rules, scaling factors for device parameters	**L1, L2, L3**
Module-4	
Subsystem Design and Layout-1: Switch logic pass transistor, Gate logic inverter, NAND gates, NOR gates, pseudo nMOS, Dynamic CMOS **Examples of structured design**: Parity generator, Bus arbitration, multiplexers, logic function block, code converter.	**L1,L2, L3**
Module-5	
Subsystem Design and Layout-2: Clocked sequential circuits, dynamic shift registers, bus lines, General considerations, 4-bit arithmetic processes, 4-bit shifter, Regularity-Definition & Computation **Practical aspects and testability**: Some thoughts of performance, optimization and CAD tools for design and simulation.	**L1, L2, L3**

Course Outcomes: After studying this course, students will be able to:

1. Identify the CMOS layout levels, and the design layers used in the process sequence.
2. Describe the general steps required for processing of CMOS integrated circuits.
3. Design static CMOS combinational and sequential logic at the transistor level.
4. Demonstrate different logic styles such as complementary CMOS logic, pass-transistor Logic, dynamic logic, etc.
5. Interpret the need for testability and testing methods in VLSI.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Books:

"Basic VLSI Design", Douglas A Pucknell, Kamran Eshraghian, 3rd Edition, Prentice Hall of India publication, 2005.

References:

1. "CMOS Digital Integrated Circuits, Analysis And Design", Sung – Mo (Steve) Kang, Yusuf Leblebici, Tata McGraw Hill, 3rd Edition, 2003.
2. "VLSI Technology", S.M. Sze, 2nd edition, Tata McGraw Hill, 2003.

ADDITIONAL OPEN ELECTIVES-B OFFERED BY EC/TC BOARD

B. E. EC/TE Choice Based Credit System (CBCS) and Outcome Based Education (OBE) SEMESTER – VII			
ARM EMBEDDED SYSTEMS			
Course Code	**18EC753**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**03**	**SEE Marks**	**60**
Total Number of Lecture Hours	**40(8Hours/Module)**	**Exam Hours**	**03**
CREDITS – 03			

Course objective: This course will enable students to:

- Understand the importance and applications of ARM Design
- Know the architecture of ARM processor
- Use instruction sets of ARM processor
- Analyze the adaptation of C code, firmware, OS, Interrupts, caches, etc. in ARM embedded systems

Module-1	RBT Level
ARM Embedded Systems Introduction, RISC design philosophy, ARM design philosophy, Embedded system hardware – AMBA bus protocol, ARM bus technology, Memory, Peripherals, Embedded system software – Initialization (BOOT) code, Operating System, Applications. **ARM Processor Fundamentals** ARM core dataflow model, registers, current program status register, Pipeline, Exceptions, Interrupts and Vector Table, Core extensions.	**L1, L2**
Module-2	
Introduction to the ARM Instruction set Introduction, Data processing instructions, Load - Store instruction, Software interrupt instructions, Program status register instructions, Loading constants, Conditional Execution. ALP programming.	**L1, L2, L3**
Module-3	
Introduction to the THUMB instruction set Introduction, THUMB register usage, ARM – THUMB interworking, Other branch instructions, Data processing instructions, Stack instructions, Software interrupt instructions. ALP programming	**L1, L2, L3**
Module-4	
Efficient C Programming: Overview of C Compilers and optimization, Basic C data types, Local Variable Types, Portability issues **Exception and Interrupt Handling:** Exception Handling-ARM Processor Exceptions and Modes, Vector Table, Exception Priorities, Link Register Offset, Interrupts- Interrupt Latency, Basic Interrupt Stack design and implementation, Interrupt Handling Schemes (**general description only** of the schemes)	**L1, L2, L3, L4**
Module-5	
Firmware: Firmware and Bootloader **Embedded Operating Systems:** Fundamental Components **Caches:** The memory Hierarchy and caches memory-caches and memory management units, Cache architecture basic architecture of caches memory, basic operation of cache controller, the relationship between cache and main memory.	**L1, L2**

Course Outcomes: After studying this course, students will be able to:

1. Depict the organization, architecture, bus technology, memory and operation of the ARM processors
2. Employ the knowledge of Instruction set of ARM processors to develop basic Assembly Language Programs
3. Recognize the importance of the Thumb mode of operation of ARM processors
4. Describe the techniques involved in writing C code for ARM processors and Exception & Interrupt handling in ARM Processors
5. Describe the importance and use of Firmware, OS and cache in ARM Embedded systems

Students have to conduct the following experiments as a part of CIE marks along with other Activities:

Conduct the following experiments by writing Assembly Language Program (ALP) using ARM Cortex M3 Registers using an evaluation simulator and the required software tool.

1. Write an ALP to find the sum of 10 integer numbers.
2. Write an ALP to multiply two 16-bit binary numbers.
3. Write an ALP to find factorial of a number.
4. Write an ALP to add an array of 16-bit numbers and store the 32-bit result in internal RAM
5. Write an ALP to find the square of a number (1 to 10) using look-up table.
6. Write an ALP to find the largest/smallest number in an array of 32 numbers.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Book:

"ARM System Developers Guide", Andrew N Sloss, Dominic System and Chris Wright, Elsevier, Morgan Kaufmann publisher, 1st Edition, 2008, ISBN:1758608745.

References:

1. "ARM System on chip Architecture", Furber S, Addison Wiley, 2nd Edition, 2008, ISBN:9780201675191
2. "Embedded System", Rajkamal, Tata McGraw-Hill Publishers, 2nd Edition, 2008, ISBN: 0070494703.

ADDITIONAL OPEN ELECTIVES-B OFFERED BY EC/TC BOARD

B. E. EC/TE Choice Based Credit System (CBCS) and Outcome Based Education (OBE) SEMESTER – VII			
DIGITAL SYSTEMS DESIGN USING VHDL			
Course Code	**18EC754**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**03**	**SEE Marks**	**60**
Total Number of Lecture Hours	**40(8Hours/Module)**	**Exam Hours**	**03**
CREDITS – 03			

Course objective: This course will enable students to:

- Use the industry-standard hardware description language VHDL into the digital design process.
- Design VHDL models ranging in complexity from a simple adder to more complex circuits.
- Understand the synthesis and testing of the models.

Module-1	**RBT Level**
Review of Logic Design Fundamentals: Combinational logic, Boolean Algebra and Algebraic Simplification, Karnaugh maps, Designing with NAND and NOR gates, Hazards in combinational Networks, Flipflop and Latches, Mealy Sequential Network Design, Design of Moore Sequential Network, Equivalent states and reduction of state Tables, Synchronous Design, Tristate Logic and Buses (Text 1, Chapter 1- 1.1 to 1.9, 1.12, 1.13)	**L1, L2, L3**
Module-2	
Introduction to VHDL: VHDL Description of Combinational Networks, Modeling Flip-flops using VHDL Processes, VHDL Models for a Multiplexer, Modeling a sequential Machine, Variables, signals, and constants, Arrays, VHDL operators, VHDL Functions, VHDL Procedures, Packages and Libraries. (Text 1, Chapter 2- 2.1, 2.2, 2.3, 2.5, 2.6, 2.7, 2.8, 2.9, 2.10, 2.11)	**L1, L2, L3**
Module-3	
Styles of Descriptions: VHDL Data types, VHDL Styles of Description (Text 2, Chapter 1- 1.5, 1.6) **Data flow Description**: Highlights of Data flow Description, Structure of Data flow Description, Data type-vectors, Common VHDL programming Errors (Text 2, Chapter 2- 2.1- to- 2.4)	**L1, L2, L3**
Module-4	
Designing with programmable Logic Devices: Read only memories, Programmable Logic Arrays, Programmable Array Logic, Other sequential programmable Logic Devices (PLDs), Generics, Generate statements. (Text 1, Chapter 3- 3.1, 3.2, 3.3, 3.4) **Design of Networks for Arithmetic Operations:** Design of serial Adder with Accumulator, Design of Binary Multiplier, Multiplication of signed Binary Numbers, Design of Binary Divider (Text 1, Chapter 4- 4.1, 4.3, 4.4, 4.5)	**L1, L2, L3**
Module-5	
Synthesis: Highlights of synthesis, synthesis information from entity and module, Mapping process in the hardware domain- Mapping of signal assignment, variable	**L1, L2, L3**

assignment, if statements, else-if statements, loop statement. (Text 2, Chapter5- 10.1, 10.2, 10.3) **Hardware Testing and Design for Testability**: Testing Combinational Logic, Testing Sequential Logic. (Text 1, Chapter 10- 10.1, 10.2))	

Course Outcomes: After studying this course, students will be able to:

1. Understand the basic concepts of Digital Design
2. Implement various Combinational and sequential circuits using VHDL descriptions. Write simple VHDL programs in different styles.
3. Design and verify the functionality of digital circuits (PLA, PAL, PLD) and Arithmetic Operations.
4. Identify the suitable Abstraction level for a particular digital design.
5. Write the programs more effectively using Verilog tasks and directives. Perform timing and delay Simulation.

Students have to conduct the following experiments as a part of CIE marks along with other Activities:

Conduct the following experiments using an suitable simulator and the required software tool.

1. Write a VHDL code to implement half and full adder using Data flow style.
2. Write a VHDL code to realize various logic gates.
3. Write a VHDL code to implement four-bit full adder using structural style.
4. Write a VHDL code to implement 2*2 unsigned combinational Array Multiplier.
5. Write a VHDL code to implement D Latch.
6. Implement JK flip flop modeling using VHDL process

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Books:

1. "Digital Systems Design using VHDL", Charles H. Roth, Jr., The University of Texas at Austin. 2006 reprint, Thomson Asia Pte Ltd, Singapore
2. "HDL Programming VHDL and Verilog", Nazeih M. Botros, 2009 reprint, Dreamtech press

Reference:

"VHDL for Programmable Logic", Kevin Skahill, Pearson education, 2006