ವಿಶ್ವೇಶ್ವರಯ್ಯ ತಾಂತ್ರಿಕ ವಿಶ್ವವಿದ್ಯಾಲಯ

("ವಿ ಟಿ ಯು ಅಧಿನಿಯಮ ೧೯೯೪" ರ ಅಡಿಯಲ್ಲಿ ಕರ್ನಾಟಕ ಸರ್ಕಾರದಿಂದ ಸ್ಥಾಪಿತವಾದ ರಾಜ್ಯ ವಿಶ್ವವಿದ್ಯಾಲಯ)

VISVESVARAYA TECHNOLOGICAL UNIVERSITY

(State University of Government of Karnataka Established as per the VTU Act, 1994)
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REF: VTU/BGM/ACA/2022-23/ 4052

DATE: 14 NOV 2022

CIRCULAR

Subject: Changes in the textbook prescribed for Analog electronic circuits 21EC34 of 2021 scheme of Teaching and Examinations regarding...

Reference: Email from Prof. M.K.Venkatesha, Ex-Chairperson BoS in ECE and Principal, RNSIT Bengaluru, and email from Prof. Nagashetty Biradar, Chairperson BoS in ECE VTU Belagavi, dated 19.10.2022

This is concerning to the subject cited above, module 5 of the course **Analog electronic circuits** with subject code **21EC34** is from the 'Power Electronics' textbook by M D Singh and K B Khanchandani, whereas in the syllabus published on the old textbook from 'Malvino' dealing with opamps is specified. Hence Textbook no. 3 of 21EC34 has been changed to **M D Singh and K B Khanchandani, Power Electronics, 2nd Edition, Tata Mc-Graw Hill, 2009, ISBN: 0070583897'**

The updated syllabus, of course, 21EC34 - Analog electronic circuits with changed author name of textbook no. 03 is attached to this circular for information and reference.

All the Principals of Engineering Colleges under the ambit of the University are hereby informed to bring the content of the circular to the notice of all concerned.

Sd/-
REGISTRAR

To,

1. The Principals of all affiliated/ constituent /Autonomous Engineering Colleges under the ambit of VTU Belagavi.
2. The chairperson, of the Department of Mechanical Engineering /Civil Engineering /Computer Science and Engineering & Communication Electronics Engineering of the University.

Copy to.

1. To the Hon'ble Vice-Chancellor through the secretary to VC, VTU Belagavi for information
2. The Registrar (Evaluation), VTU Belagavi for information.
3. The Regional Directors (I/c) of all the regional offices of VTU for circulation.
4. The Director I/c. ITI SMU, VTU Belagavi for information and to make arrangements to upload the Circular on the VTU web portal.

14/11/22

REGISTRAR

VISVESVARAYA TECHNOLOGICAL UNIVERSITY, BELAGAVI
B.E: Electronics & Communication Engineering / B.E: Electronics & Telecommunication Engineering
NEP, Outcome Based Education (OBE) and Choice Based Credit System (CBCS)
(Effective from the academic year 2021 – 22)

III Semester

Analog Electronic Circuits			
Course Code	**21EC34**	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:0:1	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	3	Exam Hours	3

Course objectives: This course will enable students to

- Explain various BJT parameters, connections and configurations.
- Design and demonstrate the diode circuits and transistor amplifiers.
- Explain various types of FET biasing and demonstrate the use of FET amplifiers.
- Analyze Power amplifier circuits in different modes of operation.
- Construct Feedback and Oscillator circuits using FET.

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teacher can use to accelerate the attainment of the various course outcomes.

1.Lecture method (L) does not mean only traditional lecture method, but different type of teaching methods may be adopted to develop the outcomes.
2.Show Video/animation films to explain evolution of communication technologies.
3. Encourage collaborative (Group) Learning in the class
4.Ask at least three HOTS (Higher order Thinking) questions in the class, which promotes critical thinking
5.Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.
6.Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
7.Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.

Module-1

BJT Biasing: Biasing in BJT amplifier circuits: The Classical Discrete circuit bias (Voltage-divider bias), Biasing using a collector to base feedback resistor.

Small signal operation and Models: Collector current and transconductance, Base current and input resistance, Emitter current and input resistance, voltage gain, Separating the signal and the DC quantities, The hybrid Π model, The T model.

MOSFETs: Biasing in MOS amplifier circuits: Fixing VGS, Fixing VG, Drain to Gate feedback resistor.

Small signal operation and modeling: The DC bias point, signal current in drain, voltage gain, small signal equivalent circuit models, transconductance, The T equivalent circuit model.

[Text 1: 3.5(3.5.1, 3.5.3), 3.6(3.6.1 to 3.6.7), 4.5(4.5.1, 4.5.2, 4.5.3), 4.6(4.6.1 to 4.6.7)]

Teaching-Learning Process	Chalk and talk method, Power Point Presentation. **Self-study topics:**Basic BJT Amplifier Configurations- Design of Common Emitter and Common collector amplifier circuits. **RBT Level:** L1, L2, L3

Module-2

MOSFET Amplifier configuration: Basic configurations, characterizing amplifiers, CS amplifier with and without source resistance RS, Source follower.

MOSFET internal capacitances and High frequency model: The gate capacitive effect, Junction capacitances, High frequency model.

Frequency response of the CS amplifier: The three frequency bands, high frequency response, Low frequency response.

Oscillators: FET based Phase shift oscillator, LC and Crystal Oscillators (no derivation) [Text 1: 4.7(4.7.1 to 4.7.4, 4.7.6) 4.8(4.8.1, 4.8.2, 4.8.3), 4.9, 12.2.2, 12.3.1, 12,3,2]	
Teaching-Learning Process	Chalk and talk method, Power Point Presentation. **Self-study topics:**Discrete Circuit MOS Amplifier – The common source amplifier and the source follower. **RBT Level:** L1, L2, L3
Module-3	
Feedback Amplifier: General feedback structure, Properties of negative feedback, The Four Basic Feedback Topologies, The series-shunt, series-series, shunt-shunt and shunt-series amplifiers (Qualitative Analysis). **Output Stages and Power Amplifiers:** Introduction, Classification of output stages, Class A output stage, Class B output stage: Transfer Characteristics, Power Dissipation, Power Conversion efficiency, Class AB output stage, Class C tuned Amplifier. [Text 1: 7.1, 7.2, 7.3, 7.4.1, 7.5.1, 7.6 (7.6.1 to 7.6.3), 13.1, 13.2, 13.3(13.3.1, 13.3.2, 13.3.3, 13.4, 13.7)]	
Teaching-Learning Process	Chalk and talk method, Power Point Presentation. **Self-study topics:**Class D power amplifier. **RBT Level:** L1, L2, L3
Module-4	
Op-Amp Circuits: Op-amp DC and AC Amplifiers, DAC - Weighted resistor and R-2R ladder, ADC-Successive approximation type, Small Signal half wave rectifier, Absolute value output circuit, Active Filters, First and second order low-pass and high-pass Butterworth filters, Band-pass filters, Band reject filters. **555 Timer and its applications:** Monostable and Astable Multivibrators. [Text 2: 6.2, 8.11(8.11.1a, 8.11.1b), 8.11.2a, 8.12.2,8.13 7.2, 7.3, 7.4, 7.5, 7.6, 7.8, 7.9, 9.4.1, 9.4.1(a), 9.4.3, 9.4.3(a)]	
Teaching-Learning Process	Chalk and talk method, Power Point Presentation. **Self-study topics:**Clippers and Clampers, Peak detector, Sample and hold circuit. **RBT Level:** L1, L2, L3
Module-5	
Overview of Power Electronic Systems: Power Electronic Systems, Power Electronic Converters and Applications. **Thyristors:** Static Anode-Cathode characteristics and Gate characteristics of SCR, Turn-ON methods, Turn-off Mechanism, Turn-OFF Methods: Natural and Forced Commutation – Class A without design consideration. **Gate Trigger Circuit:** Resistance Firing Circuit, Resistance capacitance firing circuit, Unijunction Transistor: Basic operation and UJT Firing Circuit. [Text 3: 1.3, 1.5,1.6, 2.2,2.3,2.4,2.6, 2.7,2.9, 2.10,3.2,3.5.1, 3.5.2, 3.6.1, 3.6.3,3.6.4]	
Teaching-Learning Process	Chalk and talk method, Power Point Presentation. **Self-study topics:** Basic Construction, working and applications of DIAC, TRIAC, IGBT, GTO. **RBT Level:** L1, L2, L3
Course Outcomes (Course Skill Set) At the end of the course the student will be able to : 1. Understand the characteristics of BJTs and FETs for switching and amplifier circuits. 2. Design and analyze FET amplifiers and oscillatorswith different circuit configurations and biasing conditions. 3. Understand the feedback topologies and approximations in the design of amplifiers and oscillators. 4. Design of circuits using linear ICs for wide range applications such as ADC, DAC, filters and timers. 5. Understand the power electronic device components and its functions for basic power electronic circuits.	
Assessment Details (both CIE and SEE) The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%.	

The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

Three Unit Tests each of **20 Marks (duration 01 hour**)

1. First test at the end of 5th week of the semester
2. Second test at the end of the 10th week of the semester
3. Third test at the end of the 15th week of the semester

Two assignments each of **10 Marks**

4. First assignment at the end of 4th week of the semester
5. Second assignment at the end of 9th week of the semester

Group discussion/Seminar/quiz any one of three suitably planned to attain the COs and POs for **20 Marks (duration 01 hours**)

6. At the end of the 13th week of the semester

The sum of three tests, two assignments, and quiz/seminar/group discussion will be out of 100 marks and will be **scaled down to 50 marks**

(to have less stressed CIE, the portion of the syllabus should not be common /repeated for any of the methods of the CIE. Each method of CIE should have a different syllabus portion of the course).

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the subject (**duration 03 hours)**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored out of 100 shall be proportionally reduced to 50 marks.

Suggested Learning Resources:

Books

1. Microelectronic Circuits, Theory and Applications, Adel S Sedra, Kenneth C Smith, 6thEdition, Oxford, 2015.ISBN:978-0-19-808913-1
2. Op-Amps and Linear Integrated Circuits, Ramakant A Gayakwad, 4thEdition, Pearson Education, 2018. ISBN: 978-93-325-4991-3
3. **MD Singh and K B Khanchandani, Power Electronics, 2nd Edition, Tata Mc-Graw Hill, 2009, ISBN: 0070583897'**

Web links and Video Lectures (e-Resources):

- Integrated Electronics: Analog and Digital Circuits and Systems, Jacob Millman, Christos C. Halkias, McGraw-Hill, 2015.
- Electronic Devices and Circuit, Boylestad & Nashelsky, Eleventh Edition, Pearson, January 2015.