Model Question Paper-I with effect from 2023-24 (CBCS Scheme)

USN | | | | | | | | | | |

Third Semester B.E. Degree Examination

Digital System Design using Verilog

TIME: 03 Hours **Max. Marks: 100**

Note: 01. Answer any **FIVE** full questions, choosing at least **ONE** question from each **MODULE**.

		Module -1	*Bloom's Taxonomy Level	Marks
Q.01	a	Design a logic circuit that has 4 inputs, the output will only be high, when the majority of the inputs are high. Use k-map to simplify	L3	10
	b	Simplify the given Boolean function using Quine MC Cluskey find the prime and essential prime implicants and also verify with K-map $f(A,B,C,D)=\sum m(0,1,4,5,7,8,13,15) +d(2)$	L3	10
		OR		
Q.02	a	Simplify the following expression using K-map. Implement the simplified expression using basic gates only $f(a,b,c,d)=\Pi M(0,2,3,4,5,12,13)+dc(8,10)$	L3	10
	b	Define the following terms with example. Minterm, Maxterm	L1	04
	c	Place the following equation into proper canonical form P = f(a,b,c) = ab'+bc T = f(a,b,c) = (a+b) (b'+c)	L3	06
		Module-2		
Q. 03	a	Design two bit magnitude comparator and write truth table, relevant expression and logic diagram.	L3	08
	b	Implement the following functions using 3:8 decoder $f1(a,b,c) =\sum m(1,3,5)$ $f2(a,b,c)=\sum m(0,1,6)$	L3	6
	c	Implement Y=ad+bc'+bd using 4:1 mux considering A and B as a select line.	L3	6
		OR		
Q.04	a	Explain 4-bit carry look ahead adder with neat diagram and relevant expressions.	L2	10
	b	Implement the following Boolean function using 8:1 multiplexer and 4:1 multiplexer $f(a,b,c,d) = \Sigma m(0,1,5,6,10,12,14,15)$.	L3	10
		Module-3		
Q. 05	a	Explain the working of Master-Slave JK flip-flop with functional table and timing diagram.	L2	10
	b	Explain Universal Shift Register with the help of logic diagram, mode control table.	L2	10
		OR		
Q. 06	a	Derive Characteristic equation for SR,T,D and JK flip-flop with the help of function table	L2	10
	b	Design a Synchronous Mod-6 counter using SR flip-flop for the sequence 0-2-3-6-5-1.	L3	10

		Module-4		
Q. 07	a	Realize the 2x1 Multiplexer with active low enable and also write the Verilog program by considering delay time to the signal assignment statements with simulation waveform.	L3	10
	b	Realize the Full Subtractor circuit using Verilog data flow description.	L3	10
		OR		
Q. 08	a	List all the data types available in Verilog HDL and explain any four data types with examples.	L2	10
	b	Explain arithmetic and logical operator with example.	L2	10
		Module-5		
Q. 09	a	Realize the D-Latch Behavioral description code with circuit diagram, waveform.	L3	10
	b	Write a Verilog structural code for four bit ripple carry adder.	L3	10
		OR		
Q. 10	a	Explain with syntax of the following sequential statements in Verilog. i) For-loop ii) While-loop iii) Repeat iv)Forever	L2	8
	b	Write a Verilog program for 8:1 MUX using case statement.	L3	6
	c	Realize the JK flip-flop using Verilog Behavioral description.	L3	6

Model Question Paper-II with effect from 2023-24 (CBCS Scheme)

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Third Semester B.E. Degree Examination

Digital System Design using Verilog

TIME: 03 Hours **Max. Marks: 100**

Note: 01. Answer any **FIVE** full questions, choosing at least **ONE** question from each **MODULE**.

		Module -1	*Bloom's Taxonomy Level	Marks
Q.01	a	What is combinational circuit? Design a combinational logic circuit with three input variables that will produce logic 1 output when more than one input variables are logic 1.	L2	06
	b	Convert the following Boolean function into canonical minterm and maxterm form in decimal format $R = f(a,b,c) = a + b(a+c) + bc$	L2	06
	c	Find all the prime implicants and essential prime implicants for the following function using k-map method. (i) $M = f(a,b,c,d) = \Sigma(1,5,7,8,9,10,11,13,15)$ (ii) $Y = f(a,b,c,d) = \pi(0,2,3,8,9,10,12,14)$	L3	08
		OR		
Q.02	a	. Simplify the following Boolean functions using K-map (i) $Y = f(a,b,c,d) = \pi(0,1,4,5,8,9,11) + d(2,10)$ (ii) $M = f(w,x,y,z) = \Sigma(0.1,2,4,5,6,8,9,12,13,14)$	L3	10
	b	Solve the following Boolean function by using QM minimization technique $P = f(w,x,y,z) = \Sigma(2,3,4,5,13,15) + \mathrm{d}(8,9,10,11)$ Verify using K-map method	L3	10
		Module-2		
Q. 03	a	Implement the following functions using 3:8 decoder along with OR and/or NOR gates. In each case the gates should be selected so as to minimize their total number of inputs. (a) f_1 (X_2, X_1, X_0) = Σ m(0,2,4,6,7) and f_2 (X_2, X_1, X_0) = Σ m(1,3,5,6,7) (b) f_1 (X_2, X_1, X_0) = ΠM (0,2,4,6,7) and f_1 (X_2, X_1, X_0) = ΠM (1,3,7)	L3	07
	b	Construct single decade decimal adder with necessary correction circuit design.	L2	08
	c	Design a one-bit comparator circuit.	L2	05
		OR		
Q.04	a	Construct the following function S = f(a,b,c,d) = Σ(1,4,5,7,8,9,14,15) using (a)8:1 Mux and (b)16:1 Mux	L2	07
	b	Construct the functional table for 4 to 2 line priority encoder with a valid output, assigning highest priority to highest bit position or input with highest index and obtain the minimal sum expressions for the outputs.	L2	07
	c	Implement a Full adder using PAL	L2	06
		Module-3		
Q. 05	a	Explain the working of Master-Slave JK flip-flop with functional table and timing diagram	L2	08
	b	Derive the characteristic equations of SR and D Flipflops	L2	04
	c	Make use of negative edge triggered T -Flip Flops to describe the working	L2	08

		of 4-bit binary ripple counter. Also draw the timing diagram.		
		OR		
Q. 06	a	Make use of 4-bit shift register circuit to explain the following modes of operations: SISO, SIPO, PISO and PIPO.	L2	08
	b	Develop a mod-5 synchronous counter with the sequence 0,2,6,3,1 using T -Flip Flops.	L3	07
	c	Explain the working of Ring counter with necessary diagram and equations.	L2	05
		Module-4		
Q. 07	a	List all the data types available in Verilog HDL. Explain any three data types with examples.	L2	08
	b	Explain three modeling styles available in Verilog with half adder example	L2	07
	c	(ii)Evaluate the following: i)A * B ii) A + B iii) A << 2 iv) {A [3], B} Given: A=0011 B= 0100	L2	05
		OR		
Q. 08	a	Explain the Signal declaration and Assignment Statements in Verilog data-flow description.	L1	06
	b	Realize D latch with active high enable and also write the Verilog program by considering delay time to the signal assignment statements with simulation waveforms.	L2	08
	c	Write a verilog dataflow model for full adder	L2	06
		Module-5		
Q. 09	a	Write a verilog behavioural description for 8:1 mux along with the design and timing diagrams.	L2	08
	b	Explain different case statements available in verilog with syntax and necessary examples	L2	06
	c	Realize the Binary up-down counter using verilog behavioral description.	L2	06
		OR		
Q. 10	a	Explain with syntax of the following sequential statements in Verilog. i) For-loop ii) While-loop iii) Repeat	L2	06
	b	Write a structural description of 3-bit ripple carry adder	L2	08
	c	Write a verilog code for 2x1 mux using If Else statement	L2	06