Model Question Paper with effect from 2023-24 (CBCS 2022 Scheme)

USN | | | | | | | | | | |

Third Semester B.E. Degree Examination

Subject Title: COMPUTER ORGANISATION & ARCHITECTURE

Time :03 Hours **Max Marks:100**

Note: Answer any **FIVE** full questions, choosing at least **ONE** question from each **MODULE**.

		Module -1	RBL	COs	Marks	PO
Q.01	a	With a neat diagram, describe the functional units of a computer	L2	1	8	1
	b	Explain little endian and big endian byte address assignment with a neat diagram. Show how the number 34761395 is stored using these methods.	L2	1	6	1,2
	c	With a neat diagram, discuss the operation concepts in a computer highlighting the role of PC, MAR, MDR & IR	L2	1	6	1,2
		OR				
Q.02	a	Explain the IEEE standard used for single & double precision floating point number representation with examples	L2	1	8	1,2
	b	Perform the subtraction on the following pairs of numbers using 5-bit signed 2's complement format. Determine about overflow in each case i) +12 and +9 ii) -15 and -9 iii) +10 and -8	L3	1	6	1,2
	c	Discuss the following with an example i) Three-address instruction ii) Two-address instruction iii) One-address instruction	L2	1	6	1,2
		Module-2				
Q. 03	a	Describe the following addressing modes with an example i) Register ii) Direct iii) Indirect iv) Index	L2	2	8	1,2
	b	Define Stack, Explain push & pop operations on stack with neat diagram and examples	L1	2	6	1
	c	Consider a register R1 to size 16-bits with initial data 5876d. With neat diagram, depict the output in each case after performing the following operations i) LshiftL #2,R1 ii)AshiftR #1,R1 iii) RotateR #1,R1	L2	2	6	1,2
		OR				
Q.04	a	Consider a database of marks scored by students in 3 tests stored in memory starting at address LIST. Each student record consists of student ID followed by marks in 3 tests. Assume each of there to be 4 bytes in size. There are 50 students in the class & this value is stored at location NUM i) Sketch the memory map showing all details	L3	2	10	2,3

		ii) Develop an ALP using indexed addressing mode to compute the sum of scores by all the students in Test 2 and store the results in location SUM. Write appropriate comments				
	b	Define subroutine. With a program segment illustrate parameter passing using registers	L2	2	6	1,2
	c	Explain memory operations with examples	L2	2	4	1,2
Module-3						
Q. 05	a	Define interrupt. Point out & explain the various ways of enabling & disabling interrupts	L2	3	10	1,2
	b	Explain operation of DMA with neat diagram	L2	3	6	1,2
	c	Write a explanary note on interrupt hardware	L1	3	4	1,2
OR						
Q. 06	a	Illustrate interrupt priority scheme with neat diagram	L2	3	8	1,2
	b	Distinguish between memory mapped I/O and standard I/O write a program segment to read a line of text from keyboard & display it.	L2	3	6	1,2
	c	Explain the concept of Vectored Interrupt	L2	3	6	1,2
Module-4						
Q. 07	a	With a neat diagram, explain the principal of working of magnetic disk	L2	4	10	1,2
	b	Explain the internal organization of 2M x 8 DRAM chip with neat diagram	L2	4	10	1,2
OR						
Q. 08	a	Illustrate Internal structure of static memory	L3	4	10	1,2
	b	With a neat diagram, explain virtual memory organization	L2	4	10	1,2
Module - 5						
Q. 09	a	Explain Single bus organization of the datapath inside a processor with neat diagram	L2	5	10	1,2
	b	Develop the complete control sequence for the execution of instruction Add (R3), R1	L3	5	10	2,3
OR						
Q. 10	a	Describe Three-bus organization of the datapath with a neat diagram.	L2	5	10	1,2
	b	Discuss Hardwired control unit organization with relevant diagram	L2	5	10	1,2

Model Question Paper-I with effect from 2023-24 (CBCS Scheme)

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COMPUTER ORGANIZATION AND ARCHITECTURE

TIME: 03 Hours **Max. Marks: 100**

Note: 01. Answer any **FIVE** full questions, choosing at least **ONE** question from each **MODULE**.

		Module -1	*Bloom's Taxonomy Level	Marks
Q.01	a	Explain the operation of computer with neat block diagram	L2	6M
	b	Write a program to evaluate the arithmetic statement Y= (A+B)*(C+D) using three address, two address, one address, zero address instruction.	L3	8M
	c	Write a short note on i) Basic performance equation ii) Clock rate	L2	6M
		OR		
Q.02	a	Explain Bus structure architecture with neat diagram.	L2	6M
	b	Illustrate Instruction and sequencing with an example.	L3	8M
	c	Explain the memory operation.	L2	6M
		Module-2		
Q. 03	a	Define Addressing Modes? Explain various types of addressing modes with example.	L2	10M
	b	Define Subroutine and parameter passing, Explain how to pass the parameter by value & by reference.	L2	10M
		OR		
Q.04	a	What are assembler directives? Explain any five assembler directives.	L2	10M
	b	Explain shift & rotate operation with example.	L2	10M
		Module-3		
Q. 05	a	What is Bus Arbitration? Explain centralized and distributed arbitration method with neat diagram.	L2	10M
	b	With relevant diagram, discuss the implementation of interrupt priority using individual interrupt request.	L2	10M
		OR		
Q. 06	a	Explain DMA techniques and its importance.	L2	10M
	b	Define Interrupt?Point out and explain the various ways of enabling and disabling interrupts.	L2	10M
		Module-4		
Q. 07	a	Explain the connection of the main memory to the processor.	L2	10M
	b	Explain the internal organization of 1Mx1 dynamic memory chip with neat diagram.	L2	10M
		OR		
Q. 08	a	Explain the Memory hierarchy in computer system.	L2	10M
	b	Explain the magnetic disk principle with neat diagram	L2	10M
		Module-5		
Q. 09	a	Explain single Bus Organization with neat diagram	L2	10M
	b	Write a steps involved in execution of an instruction. And explain the control sequence for execution of the instruction Add(R3),R1	L3	10M
		OR		
Q. 10	a	Explain complete processor with neat diagram	L2	10M
	b	Explain the organization of micro programmed control unit with neat diagram. And show how to organize control unit for handling conditional branching.	L3	10M