Model Question Paper-I with effect from 2023-24

CBCS SCHEME

Third Semester B.E Degree Examination, _____

Analog Electronics Circuits BVL302

TIME: 03Hours Max.Marks:100

NOTES: *Answer any FIVE full questions, choosing at least ONE question from each MODULE*

Q. No.		Module 1	Marks
Q1	a)	Explain the classical discrete circuit Bias arrangement with neat diagram and Equation.	08
	b)	Explain the biasing using collector-to- base feedback resistance with neat diagram & equation of BJT?	06
	c)	A BJT CE amplifier β=120 is biased at a DC collector current of 1mA and R_L =1kΩ. Determine the value of g_m, r_e, A_V and r_π at bias point	06
OR			
Q2	a)	State the disadvantage of fixed V_{GS} biasing technique & explain how stability of operating point is achieved in drain-to-gate feedback resistor basing technique in MOSFET amplifier	08
	b)	Explain the biasing of a FET using a Drain-to-gate feedback resistance with diagram	06
	c)	With meat diagram Explain the BJT Hybrid π model	06
Module 2			
Q3	a)	Explain the high frequency response of a cs amplifier using MOSFET & derive its upper cut-off frequency	10
	b)	Write a note on 3 basic configuration of a MOSFET.	04
	c)	For an n channel MOSFET with tox= 10nm, L=1um, W = 10 um, Lov = 0.05 um, C_{Sbo} = C_{dbo} = 10fF , Vo=0.6V. V_{SB}= 1V, V_{DS}-2V, calculate Cox, C_{ov}, C_{gs}, C_{gd}, C_{sb}, C_{db} when transistor is operating in saturation?	06
OR			
Q4	a)	Derive the expression for Wp1,Wp2,Wp3, from how frequency response of a common source amplifier	10
	b)	A phase shift oscillator is to be designed with FET having gm = 5000us, rd = 40Kohm, while the resistance in the feedback circuit is 9.7Kohm, select the proper value of C and Rd to have the frequency of oscillators as 5KHZ	04
	c)	Explain the working of a colpitts oscillator with neat diagram	06
Module 3			
Q5	a)	Draw the block diagram, general structure of feedback amplifier and how the overall gain is effected in this amplifier.	06
	b)	Show how gain can be desensitized with the application of negative feedback.	04
	c)	Draw the block diagram of series-shunt feedback amplifier and derive an expression f or voltage gain, input resistance and output resistance.	10

OR			
Q6	a)	Explain the transformer coupled class-A power amplifier with neat diagram and prove the efficiency is 50%.	08
	b)	A class-B push pull amplifier is supplied with Vcc=50V.The signal brings the collector voltage down to Vmin=5V.The total dissipation from both transistors is 40W.Find the total power and conversion efficiency.	06
	c)	Define power amplifiers and list the types of power amplifiers based on the location of Q-point and efficiency.	06
Module 4			
Q7	a)	How does negative feedback effect the performances of non-inverting amplifier with feedback [voltage-series feedback amplifier] using OP-AMP?. Derive the relevant expression for gain , input resistance , output resistance and band width	10
	b)	Design the non-inverting comparator using OP-AMP and derive the output voltage?	06
	c)	Design the basic differential amplifier used as a subtractor using OP-AMP?	04
OR			
Q8	a)	Explain the working of instrumentation amplifier using transducer bridge and derive the expression of output voltage.	10
	b)	Design the non-inverting configuration using OP-AMP with 3input as average amplifier and summing amplifier. If supply voltage = ±15V Va=2V, Vb=3V, Vc=4V, R= R1=1K Ω, Rf= 2K Ω. Determine voltage V1 at non-inverting terminal and output voltage V0. Assume that OP-AMP is initially nulled.	10
Module 5			
Q9	a)	With a neat diagram, explain the working of 4- bit R-2R DAC . Draw the staircase waveform when Vr=50v	08
	b)	With neat diagram and output waveforms, Explain the working of positive small signal half wave rectifier circuit.	06
	c)	Design a wide Band pass filter with fL=200 and fH=1khz and passband gain=4, choose c=0.01µf for LPF, c==0.05uf for LPF. Calculate the value of d choose fc=447.2 hz	06
OR			
Q10	a)	Explain the working of a Monostable operation with functional diagram using 555 timer with relevant circuit and waveforms	10
	b)	Draw the circuit and frequency response of a first order low pass Butterworth filter. Design a first order low pass filter to have a cut off frequency of 1khz with passband gain of 2	10