MODEL QUESTION PAPER

DEPARTMENT OF ELECTRONICS ENGINEERING (VLSI DESIGN AND TECHNOLOGY).

DIGITAL LOGIC CIRCUIT (BVL303)

Module -1			RBL	CO's	Marks	PO's
Q.01	a	Define the following: i) Sum of product, ii) Canonical product of sum, iii) Essential Prime Implicants, iv) Prime implicants, v) Maxterm, vi) literal.	L1	1	6	1,2
	b	Express the following equation in their proper Canonical form: i) P = f (a,b,c,d) = ab+c'+acd . ii) T = f(a,b,c) = b . (a+c').(c'+b).	L2	1,2	6	1,2
	c	Simplify the following function using K-map and Realize simplified expression using logic gates: V = f (a,b,c,d,e) = π M (0, 2, 4, 6, 8, 9,0,11,12, 14,16,17,18,19,24,25,26,27)	L2	1,2	8	1,2, 3
Or						
Q.02	a	Simplify the following function, using K-map. Realize simplified expression using logic gates: V=f(a,b,c,d)=∑m(3,7,10,11,12,13,15).	L2	1,2	4	1,2, 3
	b	Construct a function table for a Binary to Gray code converter, using K map simplify the output equation and design a logical circuit.	L3	1,2	10	1,2, 3
	c	Simplify the following function using Quine McCluskey method. S= f(w,x,y,z) =∑m(1,3,5,13,15,)+∑d(7,8,9,10,11) .	L2	1,2	6	1,2
Module-2						
Q.03	a	Starting from the function table, design and illustrate a 1-bit full adder circuit using basic gates.	L2	1,2	6	1,2
	b	With a neat Truth table, and block diagram explain IC 74138, 3:8 Decoder.	L1	1,2	6	1,2
	c	With a neat architecture explain the working of a CPLD	L1	1,2	8	1,2
Or						
Q.04	a	Design A 4-bit Carry look Ahead Logic network.	L3	1,2	8	1,2, 3
	b	Realize 1-bit subtractor using IC 74153 Dual 4:1 multiplexer.	L3	1,2	6	1,2
	c	Realize the following Boolean functions using PLA. i)f_0 =A'B'+AC', ii) f_1 = AC'+B, iii) f_2 =A'B'+BC', iv) f_3 =B+AC.	L2	1,2	6	1,2, 3
Module -3						
Q.05	a	With a neat logic circuit and truth table, and all relevant cases explain the working of a pulse triggered S R flip-flop.	L2	1,2, 3	8	1,2
	b	Design a twisted ring counter to count odd sequence.	L2	1,3	6	1,2
	c	Define the following terms with a neat timing diagram illustration: i) Propagation delay, ii) Setup time iii) Hold time.	L1	1,3	6	1
Or						
Q.06	a	With a neat block diagram explain the implementation of a SR Latch as a switch debounce circuit.	L2	1,3	6	1,2
	b	With a neat Block diagram, counting sequence and timing diagram illustrate the working of 4-bit Asynchronous Counter.	L2	1,3	6	1,2
	c	Starting with the function table, design a universal Shift register.	L2	1,3	8	1,2
Module-4						
Q.07	a	Design a MOD-6 synchronous counter to count the sequence:0-2-4-5-3-1, using T flip flop.	L3	1,3, 4	12	1,2, 3

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	b	With a neat transistor circuit diagram explain the working of SRAM memory cell.	L1	1,3	8	1,2
Or						
Q.08	a	Design an MOD -6 Up counter using JK Flip-flop.	L3	1,3	12	1,2, 3
	b	List and explain different types of read only memory.	L1	1,3	8	1
Module-5						
Q.09	a	With a neat block diagram discuss the Mealy and Moore state machine.	L1	1,3	4	1,2
	b	A sequential circuit has one input X and two outputs Z. The circuits examine groups of 4 consecutive inputs and produce output if the input sequence is either “0101” or “1001”. The circuit should reset after every 4 inputs. Design a mealy state diagram.	L3	1,4, 5,6	10	1,2, 3
	c	With a neat block diagram explain the working of serial adder with Accumulator.	L1	1,4, 5,6	6	1,2
or						
Q.10	a	List the guidelines for construction of state graph.	L1	1,4, 5,6	8	1,2
	b	Design an iterative Comparator	L3	1,4, 5,6	12	1,2, 3