MODEL QUESTION PAPER

DEPARTMENT OF ELECTRONICS ENGINEERING (VLSI DESIGN AND TECHNOLOGY).

Verilog HDL (BVL304)

Module -1			RBL	CO's	Marks	PO's
1	a	**Discuss** the importance of HDLs in digital design. Mention the two important HDLs	L1	1	5	1,2
	b	With the neat flow diagram **Explain** the designing of VLSI Integrated circuits.	L2	1	8	1,2
	c	With the Example **Explain** the different Design methodologies in VLSI chip Design.	L2	1	7	2,3
OR						
2	a	**What** is Design hierarchy in Chip design? **Discuss** the designing of Four bit Ripple counter by adopting design hierarchy.	L3	1	8	1,2, 3
	b	**Design** a Verilog model, A 4-bit ripple carry adder (Ripple_Add) contains four 1-bit full adders. i) Define the module FA. Do not define the internals or the inal list. ii) Define the module Ripple_Add. Do not define the internals or the terminal list. Instantiate four full adders of the type FA in the module le_Add and call them fa0, fa1, fa2 and fa3.	L3	1	7	1,2, 3
	c	**What** is module in Verilog? **Write** a module definition for the following in Verilog . i) 4:1 Multiplexer ii) Half adder	L1, L2	1	5	1,2
Module-2						
3	a	If A ,B and C are the three unsigned variables with A=11110000, B= 01011101 and C=00000000 find the value of i) ~|B ii) B<<2 iii) { A,B }	L2	2	3	1,2
	b	**Write** the following numbers: a) Decimal number 123 as a sized 8-bit number in binary. Use_for readability. b) A 16-bit hexadecimal unknown number with all x's. c) A 4-bit negative 4 in decimal. Write the 2's complement form for this number. d) An unsized hex number ABCD.	L1	2	4	1,2
	c	**What** is Simulation? With the block diagram **explain** how to instantiate design block in to the stimulus block.	L1, L2	2	6	1,2
	d	**Write** and **explain** the design hierarchy for SR Latch Simulation.	L1, L2	2	7	1,2, 10
		OR				
4	a	**Discuss** the following date types with example in Verilog HDL. i)Nets ii)Registers iii) arrays iv) Real v) Integers vi) Memory	L2	2	8	1,2,
	b	**Describe** the following variables in Verilog: a) A 32-bit storage register called address. Bit 31 must be the most significant bit. Set the value of the register to a 32-bit decimal number equal to 3. b) An array called delays. Array contains 20 elements of the type integer. c) A memory MEM containing 256 words of 64 bits each	L2	2	6	1,2
	c	**Declare** a top-level module stimulus. **Define** REG_IN(4-bit)and CLK(1-bit) as **reg** register variables and REG_OUT(4-bit)as **wire**.	L2	1,2	6	1,2, 3

		Instantiate the module shift_reg and call it sr1.i) Connect the ports by ordered list. ii) Connect the ports by name list.				
Module -3						
5	a	**Design** 4:1 Multiplexer using basic Gates. **Write** the gate level modeling to implement the same.	L1, L1	3	8	1,2
	b	**With** the logic symbol and truth table **discuss** how to instantiate bufif0 and notifo using **Verilog HDL.**	L2	3	6	1,2
	c	**Discuss** the following delays with example **i)** Rise delay ii) Fall delay iii) Turn off delay	L1	3	6	1,2, 10
Or						
6	a	**Design** a logic diagram to implement the expression Y= (A+B).C assume that delay of each gates is 4 time units . **write** the Verilog model and stimulus to implement the same.	L2	3	6	1,2
	b	**Discuss** the following with Example . i) Regular Assignment Delay ii) Implicit Continuous Assignment Delay iii) Net Declaration Delay	L2		6	1,2
	c	**Design** and write the Logic diagram to implement full adder. **Write** the gate level modeling to implement the same.	L1, L2	3	8	1,2, 10
Module-4						
7	a	**Discuss** the following Verilog Statement with Example i) if-else statement ii) case statement iii)For loop iv)forever loop v) Initial statement vi) always statement	L2	3	9	1,2, 3
	b	**Discuss** the Blocking and Non Blocking statements with example.	L2	3	4	1,2
	c	**Write** a Verilog description to implement four bit Binary counter with asynchronous reset	L2	3	7	1,2, 10
Or						
8	a	**Write** a Verilog Description to implement D-Flip-Flop and JK Flip-Flop.	L2	3	6	1,2, 3
	b	**Explain** the difference between task and Functions in Verilog	L2	4	6	1,2
	c	**Define** a task to **compute** factorial of a four bit number. The output is a 32 bit value **.**The result is assigned to the output after a delay of 10 time units.	L3	4	8	1,2, 3,10
Module-5						
9	a	**What** is Logic Synthesis **?** With the flow diagram **discuss** the Computer aided Logic Synthesis process.	L3	1,3	8	1,2
	b	**Derive** a synthesis output for the Verilog HDL code assign out = (a & b) | c	L3	1,3	5	1,2, 3
	c	With the flow diagram **explain** the Logic Synthesis from RTL to gate level netlist**.**	L1	1,4, 5,6	7	1,2
or						
10	a	**What** is Value change dump file (VCD **) ? Explain** the Designing and analysis of simulation with VCD file.	L3	4	8	1,2
	b	**Write** a synthesis output for the Verilog code assign out = (s) ? i1: i0 ;	L3	4	6	1,2, 3

	c	**Write** the Gate level net list for the RTL code assign { sum, cout } = a + b + cin	L3	5	6	1,2, 10