Model Question Paper with effect from2023-24(CBCS 2022 Scheme)

USN | | | | | | | | | | |

Third Semester B.E. Degree Examination

Subject Title: COMPUTER ORGANISATION & ARCHITECTURE

Time:03 Hours **Max Marks:100**

Note: Answer any **FIVE** full questions, choosing at least **ONE** question from each **MODULE**.

		Module-1	RBL	COs	Marks	PO
Q.01	a	Explain basic operational concepts between the processor and memory with neat block diagram.	L1	1	8	1
	b	Explain the various parameters affecting the performance of a computer and also provide the basic performance equation	L2	1	8	1,2
	c	Illustrate Single bus structure of a computer	L2	1	4	1,2
		OR				
Q.02	a	Define Addressing mode. Discuss the following modes with example :i)Register ii)Direct iii)Indirect iv)Index	L2	1	8	1,2
	b	Explain Little-endian and Big-endian byte address assignment.	L2	1	6	1,2
	c	Discuss the following with an example i)Three-address instruction. ii)Two-address instruction. iii)One-address instruction.	L2	1	6	1,2
		Module-2				
Q.03	a	What is interrupt? With an example illustrate the concept of interrupt.	L2	2	8	1,2
	b	Discuss in brief about interrupt hardware with a neat diagram .	L2	2	6	1,2
	c	Explain the concept of vectored interrupt.	L2	2	6	1,2
		OR				
Q.04	a	Distinguish between memory mapped I/O and standard I/O. Develop a program segment to read a line of text from keyboard and display it	L3	2	8	2,3
	b	Write a neat diagram ,demonstrate how to interface printer to the processor.	L2	2	6	1,2
	c	Explain DMA controllers in a computer system, with a neat diagram.	L2	2	6	1,2
		Module-3				
Q.05	a	Explain the internal organization of memory chips with example	L2	3	8	1,2
	b	Discuss a single transistor dynamic memory cell.	L2	3	6	1,2
	c	What is cache memory? Explain direct mapping technique with a neat diagram.	L2	3	6	1,2
		OR				

Q.06	a	Explain internal organization of 2M x 8 DRAM chip with neat diagram.	L2	3	8	1,2
	b	Discuss about four types of read only memory.	L2	3	6	1,3
	c	Briefly discuss the concept of virtual memory with a diagram.	L2	3	6	1,2
Module-4						
Q.07	a	Explain Single bus organization of the data path inside a processor with neat diagram.	L2	4	8	1,2
	b	Write the decimal values 6, -3,16, -11, 25, -17, 50, -42 and -8 as signed 8 bit numbers in the following binary formats. i) Sign and magnitude ii)1'scomplement iii)2's complement.	L1	4	6	1
	c	Discuss micro programmed control unit design with relevant diagrams.	L2	4	6	1,2
OR						
Q.08	a	Discuss Hardwired control unit organization with relevant diagram.	L2	4	8	1,2
	b	Convert the following pairs of decimal numbers to 5-bit, signed 2's complement binary number and add them. State whether or not overflow occurs in each case i)6and10 ii)-14and12 iii)-6and7 iv)-4and-7 v)-11 and-12 vi)8and11	L2	4	6	1,2
	c	Compare and contrast the following: i)Hardwired control v/s ii) Microprogrammed control.	L2	4	6	1,3
Module-5						
Q.09	a	Discuss Pipelining and illustrate an example of pipeline Processing.	L2	5	10	1,2
	b	Explain parallel processing with a diagram of processor with multiple functional units.	L2	5	10	1,2
OR						
Q.10	a	With a diagram of SIMD array processor organization, explain SIMD array processor.	L2	5	10	1,2
	b	Describe four segment CPU pipeline with a neat diagram.	L2	5	10	1,2