Mathematics-III for EC Engineering		Semester	**III**
PCC Course Code	BMATEC301/BEC301	CIE Marks	50
Teaching Hours/Week(L:T:P:S)	3:0:0:0	SEE Marks	50
Total Hours of Pedagogy	40 hours	Total Marks	100
Credits	03	Exam Hours	03
Examination nature(SEE)	**Theory**		

The Syllabus is same as ECE syllabus

Analog Electronics Circuits			
Course Code	**BVL302**	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:2:0	SEE Marks	50
Total Hours of Pedagogy	40hours heory+13Labslots	Total Marks	100
Credits	4	Exam Hours	3

Course objectives: This course will enable students to

- Explain various BJT parameters and configurations.
- Understand types of MOSFET biasing and demonstrate the use of MOSFET amplifiers.
- Analyze Power amplifier circuits in different modes of operation.
- Construct Feedback and Oscillator circuits using FET.
- Analyze the different types of active filters and different modes of 555 Timer.

Teaching-Learning Process (General Instructions)

These are sample Strategies teachers can use to accelerate the attainment of the various course outcomes.

1. Lecture method (L) does not mean only traditional lecture method, but different type of teaching methods may be adopted to develop the outcomes.
2. Show Video/animation films to explain evolution of communication technologies.
3. Encourage collaborative (Group) Learning in the class
4. Ask at least three HOTS (Higher order Thinking) questions in the class, which promotes critical thinking
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skillssuch as the ability to evaluate, generalize, and analyze information rather than simply recall it.
6. Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
7. Discuss how every concept can be applied to the real world - and when that's possible, it helps improvethe students understanding.

Module-1:

BJT Biasing: Biasing in BJT amplifier circuits: The Classical Discrete circuit bias (Voltage-divider bias), Biasing using a collector to base feedback resistor.

Small signal operation and Models: Collector current and transconductance, Base current and input resistance, Emitter current and input resistance, voltage gain, Separating the signal and the DC quantities, The hybrid π model.

MOSFETs: Biasing in MOS amplifier circuits: Fixing VGS, Fixing VG, Drain to Gate feedback resistor.

Small signal operation and modeling: The DC bias point, signal current in drain, voltage gain, small signal equivalent circuit models, transconductance. [Text 1: 3.5(3.5.1, 3.5.3), 3.6(3.6.1 to 3.6.6), 4.5(4.5.1, 4.5.2, 4.5.3), 4.6(4.6.1 to 4.6.6)]

Teaching-Learning Process	Chalk and talk method, Power Point Presentation. Self-study topics: Basic BJT Amplifier Configurations- Design of Common Emitter and Common collector amplifier circuits. RBT Level: L1, L2, L3

Module-2:

MOSFET Amplifier configuration: Basic configurations, characterizing amplifiers, CS amplifier with and without source resistance RS, Source follower.

MOSFET internal capacitances and High frequency model: The gate capacitive effect, Junction capacitances, High frequency model.

Frequency response of the CS amplifier: The three frequency bands, high frequency response,

Oscillators: FET based Phase shift oscillator, LC and Crystal Oscillators (no derivation) [Text 1: 4.7(4.7.1 to 4.7.4, 4.7.6) 4.8(4.8.1, 4.8.2, 4.8.3), 4.9, 12.2.2, 12.3.1, 12,3,2]	
Teaching-Learning Process	Chalk and talk method, Power Point Presentation. Self-study topics: Discrete Circuit MOS Amplifier – The common gate amplifierand Wein bridge oscillator. RBT Level: L1, L2, L3
Module-3:	
Feedback Amplifier: General feedback structure, Properties of negative feedback, The Four Basic Feedback Topologies, The series-shunt, series-series, shunt-shunt and shunt-series amplifiers (Qualitative Analysis). **Output Stages and Power Amplifiers:** Introduction, Classification of output stages, Class A output stage, Class B output stage: Transfer Characteristics, Power Dissipation, Power Conversion efficiency, Class AB output stage, Class C tuned Amplifier. [Text 1: 7.1, 7.2, 7.3, 7.4.1, 7.5.1, 7.6 (7.6.1 to 7.6.3), 13.1, 13.2, 13.3(13.3.1, 13.3.2, 13.3.3, 13.4, 13.7)]	
Teaching-Learning Process	Chalk and talk method, Power Point Presentation. Self-study topics: Class D power amplifier, Class S output stage. RBT Level: L1, L2, L3
Module-4:	
Op-Amp with Negative Feedback and general applications: Inverting and Non inverting Amplifiers – Closed Loop voltage gain, Input impedance, Output impedance, Bandwidth with feedback. DC and AC Amplifiers, Summing, Scaling and Averaging Amplifiers, Instrumentation amplifier, Comparators, Zero Crossing Detector, Schmitt trigger. [Text 2: 3.3(3.3.1 to 3.3.6), 3.4(3.4.1 to 3.4.5) 6.2, 6.5, 6.6 (6.6.1), 8.2, 8.3, 8.4] L1,L2, L3	
Teaching-Learning Process	Teaching- Learning Process Chalk and talk method, Power Point Presentation. Self-study topics: Clippers and Clampers, Peak detector, Sample and hold circuit. RBT Level: L1, L2, L3
Module-5:	
Op-Amp Circuits: DAC - Weighted resistor and R-2R ladder, ADC-Successive approximation type, Small Signal half wave rectifier, Active Filters, First and second order low-pass and high-pass Butterworth filters, Band-pass filters, Band reject filters. **555 Timer and its applications:** Monostable and Astable Multivibrators. [Text 2: 8.11(8.11.1a, 8.11.1b), 8.11.2a, 8.12.2, 7.2, 7.3, 7.4, 7.5, 7.6, 7.8, 7.9, 9.4.1, 9.4.1(a), 9.4.3, 9.4.3(a)]	
Teaching-Learning Process	Teaching- Learning Process Chalk and talk method, Power Point Presentation. Self-study topics: All pass filters,Monostable and Astable Multivibrator applications RBT Level: L1, L2, L3
Course Outcomes (Course Skill Set) At the end of the course the student will be able to : 1. Understand the biasing and small signal analysis of BJT and MOSFET amplifier circuits. 2. Design and analyze MOSFET amplifiers and Oscillatorcircuits. 3. Understand the feedback topologies,Output Stages and Power Amplifiers. 4. Design of Op-Amp circuits with Negative Feedback and general applications. 5. Design and analysis of Op-Amp Circuits such as DAC, ADC, Filters and 555 timer applications. 06. Utilize the characteristics of transistor for different applications. 07. Design and analyze biasing circuits for transistor. 08. Design, analyze and test transistor circuitry as amplifiers and oscillators	

PART A: Hardware Experiments
01. Design and set up the BJT common emitter voltage amplifier with and without feedback and determine the gain- bandwidth product, input and output impedances.
02. Design and set-up BJT/FET i) Colpitts Oscillator, ii) Crystal Oscillator and iii) RC Phase shift oscillator
03. Design and set up the circuits using op-amp: i) Adder, ii) Integrator, iii) Differentiator iv) Inverting Schmitt trigger
04. Design active second order Butterworth low pass and high pass filters.
05. Design 4-bit R – 2R Op-Amp Digital to Analog Converter (i) using 4-bit binary input from toggle switches and (ii) by generating digital inputs using mod-16 counter.
06. Design Monostable and a stable Multivibrator using 555 Timer.
07. Experiments on series, shunt and double ended clippers and clampers
08. Design and Testing of Full wave – centre tapped transformer type and Bridge type rectifier circuits with and without Capacitor filter. Determination of ripple factor, regulation and efficiency.
PART B: Simulation using EDA software. (Edwin, PSpice, MultiSim, Proteus, Circuit Lab or any other equivalent tool can be used)
09. RC Phase shift oscillator and Hartley oscillator.
10. Narrow Band-pass Filter and Narrow band-reject filter.
11. Precision Half and full wave rectifier.
12. Monostable and Astable Multivibrator using 555 Timer.
13. Demonstrate crossover distortion and transfer characteristics of class B output stage using complementary transistors.
Assessment Details (both CIE and SEE) The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%.The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together. **CIE for the theory component of the IPCC (maximum marks 50)** • IPCC means practical portion integrated with the theory of the course. • CIE marks for the theory component are **25 marks** and that for the practical component is **25marks**. • 25 marks for the theory component are split into **15 marks** for two Internal Assessment Tests (Two Tests, each of 15 Marks with 01-hour duration, are to be conducted) and **10 marks** for other assessment methods mentioned in 22OB4.2. The first test at the end of 40-50% coverage of the syllabus and these condtest after covering 85-90% of the syllabus. • Scaled-down marks of the sum of two tests and other assessment methods will be CIE marks for the theory component of IPCC (that is for **25 marks)**. • The student has to secure 40% of 25marks to qualify in the CIE of the theory component of IPCC. **CIE for the practical component of the IPCC** • **15 marks** for the conduction of the experiment and preparation of laboratory record,

For the test to be conducted after the completion of all the laboratory sessions.

- On completion of every experiment/ program in the laboratory, the students shall be evaluated including viva-voce and marks shall be awarded on the same day.
- The CIE marks awarded in the case of the Practical component shall be based on the continuous evaluation of the laboratory report. Each experiment report can be evaluated for 10 marks. Marks of all experiments' write-ups are added and scaled down to **15marks**.
- The laboratory test **(duration 02 / 03 hours)** after completion of all the experiments shall be conducted for 50 marks and scaled down to**10 marks.**
- Scaled-down marks of write-up evaluations and tests added will be CIE marks for the laboratory component of IPCC for **25 marks**.
- The student has to secure 40% of 25 marks to qualify in the CIE of the practical component of the IPCC.

SEE for IPCC

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours**)

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored by the student shall be proportionally scaled down to 50 Marks

The theory portion of the IPCC shall be for both CIE and SEE, whereas the practical portion will have a CIE component only. Questions mentioned in the SEE paper may include questions from the practical component.

Suggested Learning Resources:

Books

1. Microelectronic Circuits, Theory and Applications, Adel S Sedra, Kenneth C Smith, 6th Edition, Oxford,2015. ISBN:978-0-19-808913-1
2. Op-Amps and Linear Integrated Circuits, Ramakant A Gayakwad, 4th Edition, Pearson Education,2018. ISBN: 978-93-325-4991-3
3. Integrated Electronics: Analog and Digital Circuits and Systems, Jacob Millman, Christos C.Halkias, McGraw-Hill, 2015.
4. Electronic Devices and Circuit, Boylestad & Nashelsky, Eleventh Edition, Pearson, January 2015.
5.

Web links and Video Lectures (e-Resources):

- **www.nptel.ac.in**
- **https://www.ti.com/design-resources/design-tools-simulation/analog_circuits/overview.html**

https://www.analog.com/en/education/education-library/tutorials/analog-electronics.html

DIGITAL LOGIC CIRCUITS		Semester	III
Course Code	**BVL303**	CIE Marks	50
Teaching Hours/Week(L:T:P:S)	3:0:2:0	SEE Marks	50
Total Hours of Pedagogy	40 hours Theory+8-10Labslots	Total Marks	100
Credits	04	Exam Hours	03
Examination nature (SEE)	**Theory**		

Course objectives:

- To illustrate simplification of algebraice quations using Karnaugh Mapsand Quine-Mc Clusky methods
- To designed coders, encoders, digital multiplexer, adders, sub tractors and binary comparators
- To explain latche sand flip-flops, registers and counters
- To analyze Melayad Moore Models
- To develop state diagrams synchronous sequential circuits
- To understand the applications of sequential circuits

Teaching-Learning Process (General Instructions)

These are sample Strategies; that teachers can use to accelerate the attainment of the various course outcomes.

1. Lecturer method (L) needs not to be only traditional lecture method, but alternative effective teaching methods could be adopted to attain the outcomes.
2. Use of Video/Animation to explain functioning of various concepts.
3. Encourage collaborative (Group Learning) Learning in the class.
4. Ask at least three HOT (Higher order Thinking) questions in the class, which promotes critical thinking.
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop design thinking skills such as the ability to design, evaluate, generalize, and analyze information rather than simply re call it.
6. Introduce Topics in mani fold representations.
7. Show the different ways to solve the same problem with different circuits/logic and encourage the students to come up with their own creative ways to solve them.
8. Discuss how every concept can be applied to the real world-and when that's possible, it helps improve the students' understanding.

MODULE-1

Principles of Combinational Logic: Definition of combinational logic, canonical forms, Generation of switching equations from truth tables, Karnaugh maps-3,4,5 variables, Incompletely specified functions (Don't care terms) Simplifying Max term equations, Quine – McClus key minimization technique, Quine- Mc Cluskey using don't care terms. (Section 3.1 to 3.5 of Text 1).

MODULE-2

Analysis and design of combinational logic: Decoders, Encoders, Digital multiplexers, Adders and subtractors, Look ahead carry, Binary comparators.(Text 1 - Chapter 4).

Programmable Logic Devices, Complex PLD, FPGA.(Text 3 - Chapter 9, 9.6 to 9.8)

MODULE-3

Flip-Flops and its Application: Basic Bis table elements, Latches, Timing considerations, The Master-Slave Flip-flops (Pulse-Triggered flip-flops): SR flip-flops, JK flip flops, Characteristic equations, Registers, Binary Ripple Counters, Synchronous Binary Counters, Counters based on Shift Registers. (Section6.1,6.2, 6.4, 6.6 to 6.7 of Text 2)

MODULE-4

Sequential Circuit Design: Design of a synchronous counter, Design of a synchronous mod-n counter using clocked JK, D, T and SR flip-flops. ((Section 6.8 to 6.9 of Text 2 excluding 6.9.3). Memories: Read only and Read / Write Memories, Programmable ROM, EPROM, Flash memory. (Text 1 - Chapter 6)

MODULE-5

Applications of Digital Circuits: Design of a Sequence Detector, Guidelines for construction of state graphs, Design Example – Code Converter, Design of Iterative Circuits (Comparator), Design of Sequential Circuits using ROMs and PLAs, CPLDs and FPGAs, Serial Adder with Accumulator, Design of Binary Multiplier, Design of Binary Divider. (Text 3 – 14.1, 14.3, 16.2, 16.3, 16.4, 18.1, 18.2, 18.3)

PRACTICAL COMPONENT OF IPCC

Sl.NO	Experiments
1	Simplification and realization of Boole an expressions using logic gates / Universal gates.
2	Realization of half / full adder and half/ full sub tractors using logic gates.
3	Realization of parallel adder/ sub tractors using 7483 chip-BCD to Excess-3 code conversion and Vice-Versa.
4	Design and implementation of 1-bit and 2-bit comparators using basic gates
5	Design and implementation of half / full adder and half/ full sub tractors using IC 74153
6	To realize the following flip-flops using NAND gates S-R flip-flop, D & T flip-flop
7	To realize the following flip-flops using IC 7476 master-slave JK flip-flop
8	Realize the following shift registers using IC 7495 a)Ring counter b) Johnson Counter
9	Realize the following shift registers using IC 7495 a) SISO b) SIPO c) PISO d) PIPO
10	To design and implement: a) mod-N synchronous UP counter and down counter using 7476J K Flip- Flop b) mod-N counter using IC 7490/7476c)synchronouscounterusingIC74192

Course out comes(Course Skill Set):

At the end of the course, the student will be able to:

- Explain the concept of combinational and sequential logic circuits
- Analyse and design combinational circuits
- Describe and characterize flip flop sand its applications
- Design the sequential circuits using SR, JK,D and T flip-flop sand Melay and Moore applications
- Design applications of combinational and sequential circuits
- Employ the digital circuits for different applications

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

CIE for the theory component of the IPCC (maximum marks 50)

- IPCC means practical portion integrated with the theory of the course.
- CIE marks for the theory component are **25 marks** and that for the practical component is **25marks**.
- 25 marks for the theory component are split into **15 marks** for two Internal Assessment Tests (Two Tests, each of 15 Marks with 01-hour duration, are to be conducted) and **10 marks** for other assessment methods mentioned in 22OB4.2.The first test at the end of 40-50% coverage of the syllabus and the second test after covering 85-90% of the syllabus.
- Scaled-down marks of the sum of two tests and 7 other assessment methods will be CIE marks for the theory component of IPCC (that is for **25 marks)**.
- The student has to secure 40% of 25 marks to qualify in the CIE of the theory component of IPCC.

CIE for the practical component of the IPCC

- **15 marks** for the conduction of the experiment and preparation of laboratory record, and **10 marks**
  For the test to be conducted after the completion of all the laboratory sessions.
- On completion of every experiment/ program in the laboratory, the students shall be evaluated including viva-voce and marks shall be awarded on the same day.
- The CIE marks awarded in the case of the Practical component shall be based on the continuous evaluation of the laboratory report. Each experiment report can be evaluated for 10 marks. Marks of all experiments' write-ups are added and scaled down to **15marks**.
- The laboratory test **(duration 02 / 03 hours)** after completion of all the experiments shall be conducted for 50 marks and scaled down to**10marks.**
- Scaled-down marks of write-up evaluations and tests added will be CIE marks for the laboratory component of IPCC for **25marks**.
- The student has to secure 40% of 25 marks to qualify in the CIE of the practical component of the IPCC.

SEE for IPCC

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours**)

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored by the student shall be proportionally scaled down to 50 Marks

The theory portion of the IPCC shall be for both CIE and SEE, where as the practical portion will

Have a CIE component only. Questions mentioned in the SEE paper may include questions from the practical component.

Suggested Learning Resources:

Books

1) John M Yarbrough , Digital logic applications and design, Thomson Learning, 2001.2)Donald D Givone, Digital Principles and design, MC GrawHill2002

3)Charles HR oth Jr, Larry L Kinney, Fundamentals of logic design, Cengage Learning, 7th Edition

Reference books:

1)D. P. Kothari and J S Dhillon, -Digital circuits and design, Pearson, 20162)Morris Mano, Digital Design, PHI,3rd edition

3) K. A. Navas, Electronics Lab Manual, Vol.1, PHI 5th edition, 2015.

Web links and Video Lectures (e-Resources):

- https://onlinecourses.nptel.ac.in/noc20_ee32/preview
- You Tube videos on digital electronics
- National Instruments : https://education.ni.com/teach/resources/1104/digital-electronics

Activity Based Learning (Suggested Activities in Class) / Practical Based learning

- To develop mini projects on digital electronics
- Simple applications like Smart Digital School Bell With Timetable Display, Stop and Go Queue Entry Manager System, Digital Car Turning and Braking Indicator, Digital Name plate with Visitor Sensing, electronic watchdog etc
- Applications based on PLAs ,FPGA, CPLD etc

Verilog HDL		Semester	III
Course Code	BVL304	CIE Marks	50
Teaching Hours/Week(L:T:P:S)	3:0:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	03
Examination nature(SEE)	**Theory**		

Course objectives:

- Learn different Verilog HDL Constructs
- Familiarize the different levels of abstraction in Verilog
- Understand Verilog tasks , functions and directives
- Understand timing and delay simulation
- Understand the concept of logic synthesis and its impact in verification

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

1. Lecturer method (L) needs not to be only traditional lecture method, but alternative effective teaching methods could be adopted to attain the outcomes.
2. Use of Video/Animation to explain functioning of various concepts.
3. Encourage collaborative (Group Learning) Learning in the class.
4. Ask at least three HOT (Higher order Thinking) questions in the class, which promotes critical thinking.
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop design thinking skills such as the ability to design, evaluate, generalize, and analyze information rather than simply recall it.
6. Introduce Topics in manifold representations.
7. Show the different ways to solve the same problem with different circuits/logic and encourage the students to come up with their own creative ways to solve them.
8. Discuss how every concept can be applied to the real world-and when that's possible, it helps improve the students' understanding.

Module-1

Overview of digital design with Verilog HDL:

Evolution of CAD, emergence of HDLs, typical HDL flow, why Verilog HDL? Trends in HDL

Hierarchical Modelling Concepts:

Top down and bottom-up design methodology, difference between modules and module instances, parts of a simulation, design block, stimulus block.

Module-2

Basic Concepts:

Lexical conventions, data types, system tasks, compiler directives.

Modules and ports:

Module definition, port declaration, connecting ports, Hierarchical name referencing.

Module-3

Gate level modeling :

Modelling using basic Verilog gate primitives, description of and /or and buf/not type gates, rise, fall and turn off delays, min, max and typical delays

Data flow modeling :

Continuous assignments, delay specification, expressions, operators, operand sand operate types.

Module-4
Behavioral modeling : Structured procedures, initial and always, blocking and non-blocking statements, delay control, generate statement, event control, conditional statements, multi way branching, loops, sequential and parallel blocks. **Tasks and functions:** Differences between tasks and functions, declaration, invocation, automatic tasks and functions.
Module-5
Useful Modeling techniques : Procedural continuous assignments, over riding parameters, conditional compilation, and execution, useful system tasks **Logic Synthesis with Verilog:** Logic synthesis, impact of logic synthesis, Verilog HDL synthesis, synthesis design flow, verification of gate level net list, (Chapter 14, till14.5 of Text1)
Course outcome(Course Skill Set) At the end of the course, the student will be able to: 1. Write Verilog program singate, dataflow(RTL), behavioral and switch modeling levels of abstraction 2. Design and verify the functionality of digital circuit and system, using test benches 3. Identify the suitable abstraction level for a particular digital system 4. Write the programs more effectively using Verilog tasks, function sand directives 5. Program timing and delay simulation and interpret the various constructs in logic synthesis.

Assessment Details(both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50)and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination)taken together.

Continuous Internal Evaluation:

- For the Assignment component of the CIE, there are 25 marks and for the Internal Assessment Test component, there are 25marks.
- The first test will be administered after 40-50% of the syllabus has been covered, and these condtest will be administered after 85-90% of the syllabus has been covered
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The teacher should not conduct two assignments at the end of the semester if two assignments are planned.
- For the course, CIE marks will be based on a scaled-down sum of two tests and other methods of assessment.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics under** that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks

Suggested Learning Resources:

Books

1) Samir Palnitkar, "Verilog HDL: Aguide to digital design and synthesis", Pearson Education, II Edition.

Reference Books:

1) Donald ET homas, Philip RMoorby, "The Verilog hardware description Language", Springer Science Business Media, LLC, 5th Edition

2) Michael D.Ciletti, "Advanced digital design with the Verilog HDL", Pearson (PHI), II Edition

3) Padmanabhan, Tripura Sunadri, "Design through Verilog HDL",Wiley,2016.

Web links and Video Lectures (e-Resources):

- NPTEL course on VHDL : https://nptel.ac.in/courses/117108040
- Youtube videos on VHDL

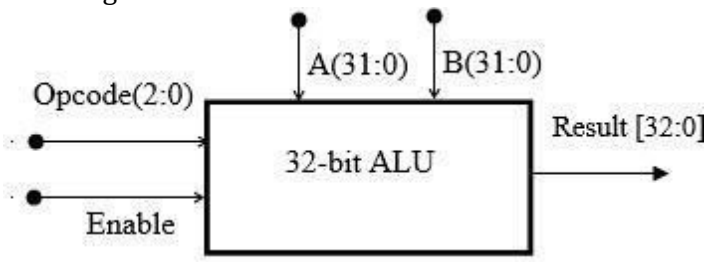
ActivityBasedLearning(SuggestedActivitiesinClass)/PracticalBasedlearning

- VHDL based projects for different applications
- Seminars
- Quizzes
- Assignments

Verilog HDL LAB		Semester	III
Course Code	**BVLL305**	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	0:0:2:0	SEE Marks	50
Credits	01	Total Marks	100
		Exam Hours	3
Examination type (SEE)	**practical**		

Course objectives:

- Familiarize with the CAD tool to write HDL programs.
- Choose Verilog for a given Abstraction level. Along with prescribed hours of teaching – learning process, provide opportunity to perform the experiments / program mesat their own time, at their own pace, at any place as per their convenience and repeat any number of times to understand the concept.

Sl.NO	Experiments
	PART-A
1	Write Verilog code to realize all the logic gates
2	Write Verilog program for the following combinational design along with test bench to verify the design: a) 2 to 4 decoder realization using NAND gates only(structural model) b) 8 to 3 encoder with priority encoder and without priority encoder (behavioral model)
3	Write Verilog program for the following combinational design along with test bench to verify the design: a) 8 to1 Multiplexer using case statement and if statement b) 4 bit binary to gray code converter using 1 bit gray to binary converter1 bit adder and sub tractor.
4	Model in Verilog for a full adder and add functionality to perform logical operations of XOR, XNOR, AND and OR gates. Write test bench with appropriate input patterns to verify the model led behavior.
5	Verilog 32 bit ALU shown in figure below and verify the functionality of ALU by selecting appropriate test patterns. The functionality of the ALU is shown in Table-1. a) Write test bench to verify the functionality of the ALU considering all possible in put patterns b) The enable signal will set the output to required functions if enabled, if disabled all the outputs are settotri-state. c) The acknowledge signalis sethigh after every operation is complete. ALUT op Level Diagram  Table-1ALUfunctions:

	<table><tr><th>Opcode (2:0)</th><th>ALU Operation</th><th colspan="2">Remarks</th></tr><tr><td>000</td><td>A + B</td><td>Addition of two numbers</td><td rowspan="2">Both A and B are in two's complement format</td></tr><tr><td>001</td><td>A – B</td><td>Subtraction of two numbers</td></tr><tr><td>010</td><td>A + 1</td><td>Increment Accumulator by 1</td><td rowspan="2">A is in two's complement format</td></tr><tr><td>011</td><td>A - 1</td><td>Decrement accumulator by 1</td></tr><tr><td>100</td><td>A</td><td>True</td><td rowspan="4">Inputs can be in any format</td></tr><tr><td>101</td><td>A Complement</td><td>Complement</td></tr><tr><td>110</td><td>A OR B</td><td>Logical OR</td></tr><tr><td>111</td><td>A AND B</td><td>Logical AND</td></tr></table>
6	Write Verilog code for SR, JK , D and T verify the flip flop
7	WriteVerilogcodefor4bit binary/BCD synchronous counter and Asynchronous counter
8	Write Verilog code for counter with given input clock and check whether it works as clock divider performing division of clock by2,4,8 and 16.Verify the functionality of the code.
9	Write Verilog code for Carry Look Ahead Adder. Verify the functionality of the code
10	Write Verilog code for 4- Bit Multiplier. Verify the functionality of the code
11	Write Verilog code for 4- Bit Divider. Verify the functionality of the code
12	Design of Sequence Detector (Finite State Machine Mealy and Moore Machines).

Note:
Programming can be done using any compiler, verify the simulation results with tools such as Altera / Models im or equivalent. Downloaded Program code in to any FPGA / CPLD boards are not Required.

Course outcomes (Course Skill Set):

At the end of the course the student will be able to:

- Write the VHDL/ Verilog programs to simulate combinational circuits in data flow, behavioral, gate level abstractions.
- Describe sequential circuits like flip-flops, counters, in behavioral descriptions and obtain simulated wave forms.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation (CIE):

CIE marks for the practical course are 50 **Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment is to be evaluated for conduction with an observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments are designed by the faculty who is handling the laboratory session and are made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled down to **30 marks** (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct a test of 100 marks after the completion of all the experiments listed in the syllabus.
- In a test, test write-up, conduction of experiment, acceptable result, and procedural

Semester End Evaluation (SEE):

- SEE marks for the practical course are 50 Marks.
- **SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the Head of the Institute**.
- The examination schedule and names of examiners are informed to the university before the conduction of the examination. These practical examinations are to be conducted between the schedule mentioned in the academic calendar of the University.
- All laboratory experiments are to be included for practical examination.
- (Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.
- Students can pick one question (experiment) from the questions lot prepared by the examiners jointly.
- Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.

General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)

Change of experiment is allowed only once and 15% of Marks allotted to the procedure part are to be made zero.

The minimum duration of SEE is 02 hours

Suggested Learning Resources:

- HDLProgrammingfundamentals,VHDLandVerilog,N.Botros,CengageLearning,

UNIX Programming			
Course Code	**BVLL358A**	CIE Marks	50
Teaching Hours/Week(L:T:P: S)	0:0:2:0	SEE Marks	50
Credits	01	Total Marks	100
		Exam Hours	02

Course objectives:

1. Use a variety of standard Unix commands
2. Pipe simple commands together to create powerful compound commands

Sl. NO	Experiments
1	Shell script implementing ten UNIX commands.
2	Shell script to create multiple files and copy it to another directory.
3	Shell script to design a calculator demonstrating while loop.
4	Write a menu-driven program according to choices: a. Check if a given number is even or odd. b. Check if the number is prime or not, demonstrating break statement
5	Shell script to convert the given decimal number to binary and vice-versa demonstrating basic calculator.
6	Write a program to check whether the user is logged in or not and send a mail demonstrating pipelining.
7	Write a program to replace or delete a pattern from the given file demonstrating filter command tr.
8	Write a program accept a string from user reverse it and check if it is palindrome or not also count the vowels demonstrating string library functions.
9	Write a program to find factorial of a number using recursion
10	Shell script to create a data file and perform copy, rename, append, display and delete file also demonstrating file manipulation commands.
11	UNIX program demonstrating AWK and SED with options.
12	Write a program which uses fork ()& wait () system call to create a child process and display an appropriate message.

Course outcomes (Course Skill Set):

At the end of the course the student will be able to:

tandard Unix editor 'vi'

learn to write shell script and debug

nd implement shell scripts

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%.TheminimumpassingmarkfortheCIEis40%of the maximum marks (20marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course. The student has to secure not less than 35% (18 Marks out of 50) in the semester-end examination (SEE).

Continuous Internal Evaluation(CIE):

CIE marks for the practical course is **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment to be evaluated for conduction with observation sheet and record write-

designed by the faculty who is handling the laboratory session and is made known to students at the beginning of the practical session.

- Record should contain all the specified experiments in the syllabus and each experiment write-up will beevaluatedfor10 marks.
- Total marks scored by the students are scaled downed to 30 marks (60% of maximum marks).
- Weightage to be given for neatness and submission of record / write-upon time.
- Department shall conduct 02 tests for 100 marks, the first test shall be conducted after the 8th week of the semester and the second test shall be conducted after the 14thweekof the semester.
- In each test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubric scan be designed to evaluat each student's performance and learning ability. Rubrics suggested in Annexure-II of Regulation book
- The average of 02 tests is scaled down to20 marks (40 % of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and average marks of two tests is the total CIE marks scored by the student.

Semester End Evaluation(SEE):

- SEE marks for the practical course is 50Marks.
- SEE shall be conducted jointly by the two examiner soft he same institute, examiners are appointed by the University
- All laboratory experiments are to be included for practical examination.
- (Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. OR based on the course requirement evaluation rubrics shall be decided jointly by examiners.
- Students can pick one question (experiment) from the questions lot prepared by the internal /external examiners jointly.
- Evaluation of test write-up/conduction procedure and result/viva will be conducted jointly by

  Examiners. General rubrics suggested for SEE are mentioned here, write up-20% , Conduction procedure and result in-60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)
- Change of experiment is allowed only once and 15% Marks allotted to the procedure part to be made zero. The duration of SEE is 03 hours.
- Rubrics suggested in Annexure-II of Regulation book.

Suggested Learning Resources:

- W. Richard Stevens: Advanced Programming in the UNIX Environment, 2nd Edition, Pearson Education, 2005
- M.G. Venkatesh Murthy: UNIX & Shell Programming, Pearson Education.

Circuit Laboratory using P-spice			
Course Code	**BVLL358B**	CIE Marks	50
Teaching Hours/Week(L:T:P: S)	0:0:2:0	SEE Marks	50
Credits	01	Total Marks	100
		Exam Hours	02

Course objectives:

1. Along with prescribed hours of teaching –learning process, provide opportunity to perform the experiments/ programmes at their own time, at their own pace, at any place as per their convenience and repeat any number of times to understand the concept.
2. Provide unhindered access to perform whenever the students wish.
3. Vary different parameters to study the behaviour of the circuit without the risk of damaging equipment/ device or injuring themselves.

Sl. NO	Experiments
1	Simulate Series RL & RC circuit and observe phase difference between waveforms of voltage and current.
2	Simulation and verification of Kirchhoff's Current Law & Kirchhoff's Voltage Law.
3	Simulation of Mesh analysis for a given circuit.
4	Simulation of Nodal analysis for a given circuit.
5	Determination of Z & Y parameters of a given two-port network
6	Simulate and verify Super Positions theorem.
7	Simulation and verification Reciprocity theorem.
8	Simulation and verification Thevenin's and Norton's theorem.
9	Simulation and verification Maximum Power Transfer theorem.
10	Simulation and verification Millman's theorem.
11	Simulation of Series and Parallel Resonance circuit.

Course outcomes (Course Skill Set):

At the end of the course the student will be able to:

- Analyse In an intelligent manner, thinks better, and perform better.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%.The minimum passing mark for the CIE is 40% of the maximum marks (20marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course. The student has to secure not less than 35% (18 Marks out of 50) in the semester-end examination (SEE).

Continuous Internal Evaluation(CIE):

CIE marks for the practical course is 50 **Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment to be evaluated for conduction with observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments designed by the faculty who is handling the laboratory session and is made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will beevaluatedfor10 marks.
- Total marks scored by the students are scaled downed to 30 marks (60%of maximum marks).
- Weightage to be given for neatness and submission of record/write-upontime

8th week of the semester and the second test shall be conducted after the 14thweekof the semester.

- In each test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability. Rubrics suggested in Annexure-II of Regulation book
- The average of 02 tests is scaled down to **20 marks** (40% of the maximum marks).
- The Sum of scaled-down marks scored in the report write-up/journal and average marks of two tests is the total CIE marks scored by the student.

Semester End Evaluation (SEE):

- SEE marks for the practical course is 50 Marks.
- SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the University
- All laboratory experiments are to be included for practical examination.
- (Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.
- Students can pick one question (experiment) from the questions lot prepared by the internal /external examiners jointly.
- Evaluation of test write-up/ conduction procedure and result /viva will be conducted jointly by examiners. General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)
- Change of experiment is allowed only once and 15% Marks allotted to the procedure part to be made zero. The duration of SEE is 03 hours

Rubrics suggested in Annexure-II of Regulation book.

Suggested Learning Resources:

- Networks and Systems, D Roy Choudhury, New age international Publishers, second edition.
- Network Analysis, M E Van Valkenburg, Pearson, 3e.

Digital Engineering Course (NASSCOM)			
Course Code	**BVL358C**	CIE Marks	50
Teaching Hours/Week(L:T:P: S)	0:0:2:0	SEE Marks	50
Credits	01	Total Marks	100
		Exam Hours	02

Course objectives:

(1)

Sl. NO	Experiments
1	
2	
3	
4	
5	
6	
7	
8	

Course out comes (Course Skill Set):

At the end of the course the student will be able to:

an intelligent manner, think better, and perform better.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%.The minimum passing mark for the CIE is 40% of the maximum marks (20marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course. The student has to secure not less than35% (18Marks out of 50) in the semester-end examination (SEE).

Continuous Internal Evaluation (CIE):

CIE marks for the practical course is **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment to be evaluated for conduction with observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments designed by the faculty who is handling the laboratory session and is made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled downed to 30 marks (60% of maximum marks).

8th week of the semester and the second test shall be conducted after the 14thweekof the semester.

- In each test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability. Rubrics suggested in Annexure-II of Regulation book
- The average of 02 tests is scaled down to 20 marks (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up / journal and average marks of two tests is the total CIE marks scored by the student.

Semester End Evaluation(SEE):

- SEE marks for the practical course is 50 Marks.
- SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the University
- All laboratory experiments are to be included for practical examination.
- (Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. OR based on the course requirement evaluation rubrics shall be decided jointly by examiners.
- Students can pick one question (experiment) from the questions lot prepared by the internal /external examiners jointly.
- Evaluation of test write-up/conduction procedure and result / viva will be conducted jointly by Examiners. General rubrics suggested for SEE are mentioned here, write up-20%, Conduction procedure and result in-60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)
- Change of experiment is allowed only once and 15% Marks allotted to the procedure part to be made zero. The duration of SEE is 03 hours.
- Rubrics suggested in Annexure-II of Regulation book.

Suggested Learning Resources:

IoT (Internet of Things) Lab			
Course Code	**BVLL358D**	CIE Marks	50
Teaching Hours/Week(L:T:P: S)	0:0:2:0	SEE Marks	50
Credits	01	Total Marks	100
		Exam Hours	02

Course objectives:

- To impart necessary and practical knowledge of components of Internet of Things
- To develop skills required to build real-life IoT based projects.

Sl. NO	Experiments
1	i) To interface LED/Buzzer with Arduino/Raspberry Pi and write a program to 'turn ON' LED for 1 sec after every 2 seconds. ii) To interface Push button/Digital sensor (IR/LDR) with Arduino/Raspberry Pi and write a program to 'turn ON' LED when push button is pressed or at sensor detection.
2	i) To interface DHT11 sensor with Arduino/Raspberry Pi and write a program to print temperature and humidity readings. ii) To interface OLED with Arduino/Raspberry Pi and write a program to print temperature and humidity readings on it.
3	To interface motor using relay with Arduino / Raspberry Pi and write a program to 'turn ON' motor when push button is pressed
4	To interface Bluetooth with Arduino / Raspberry Pi and write a program to send sensor data to smart phone using Bluetooth.
5	To interface Bluetooth with Arduino / Raspberry Pi and write a program to turn LED ON/OFF when '1'/'0' is received from smart phone using Bluetooth.
6	Write a program on Arduino / Raspberry Pi to upload temperature and humidity data to thing speak cloud.
7	Write a program on Arduino/Raspberry Pi to retrieve temperature and humidity data from thing speak cloud.
8	To install My SQL database on Raspberry Pi and perform basic SQL queries

Course outcomes (Course Skill Set) :

At the end of the course the student will be able to:

- Understand internet of Things and its hardware and software components
- Interface I/O devices, sensors & communication modules
- Remotely monitor data and control devices
- Develop real life IoT based projects

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%.The minimum passing mark for the CIE is 40% of the maximum marks (20marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course. The student has to secure not less than 35% (18 Marks out of 50) in the semester-end examination (SEE).

Continuous Internal Evaluation(CIE):

CIE marks for the practical course is **50 Marks**.

The split-up of CIE marks for record/journal and test are in the ratio 60:40.

- Each experiment to be evaluated for conduction with observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments designed by the faculty who is handling the laboratory session and is made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment

- Weightage to be given for neatness and submission of record / write- upon time.
- Department shall conduct 02 tests for 100 marks, the first test shall be conducted after the 8th week of the semester and the second test shall be conducted after the 14thweek of the semester.
- In each test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability. Rubrics suggested in Annexure-II of Regulation book
- The average of 02 tests is scaled down to 20 marks (40% of the maximum marks).

The Sum of scaled-down marks scored in there port write-up / journal and average marks of two tests is the total CIE marks scored by the student.

Semester End Evaluation(SEE):

- SEE marks for the practical course is 50 Marks.
- SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the University
- All laboratory experiments are to be included for practical examination.
- (Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. OR based on the course requirement evaluation rubrics shall be decided jointly by examiners.
- Students can pick one question (experiment) from the questions lot prepared by the internal /external examiners jointly.
- Evaluation of test write-up/conduction procedure and result/viva will be conducted jointly by Examiners. General rubrics suggested for SEE are mentioned here, write up-20%, Conduction procedure and result in-60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)
- Change of experiment is allowed only once and 15% Marks allotted to the procedure part to be made zero. The duration of SEE is 03 hours.
- Rubrics suggested in Annexure-II of Regulation book.

Suggested Learning Resources:

1. Vijay Madisetti, ArshdeepBahga, Internet of Things. "A Hands on Approach", University Press
2. Dr. SRN Reddy, RachitThukral and Manasi Mishra, "Introduction to Internet of Things: A practical Approach", ETI Labs
3. Pethuru Raj and Anupama C Raman, "The Internet of Things: Enabling Technologies, Platforms, and Use Cases", CRC Press
4. Jeeva Jose, "Internet of Things", Khanna Publishing House, Delhi
5. Adrian McEwen, "Designing the Internet of Things", Wiley
6. Raj Kamal,"Internet of Things: Architecture and Design", McGraw Hill

Circuits & Controls		Semester	III
Course Code	BVL306A	CIE Marks	50
Teaching Hours / Week(L: T:P:S)	3:0:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	03
Examination nature (SEE)	**Theory**		

Course objectives:

- Apply mesh and nodal techniques to solve an electrical network.
- Solve different problems related to Electrical circuits using Network Theorems and Two port network.
- Familiarize with the use of Laplace transforms to solve network problems.
- Understand basics of control systems and design mathematical models using block diagram reduction, SFG, etc.
- Understand Time domain and Frequency domain analysis.

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

1. Lecturer method (L) needs not to be only traditional lecture method, but alternative effective teaching methods could be adopted to attain the outcomes.
2. Use of Video/ Animation to explain functioning of various concepts.
3. Encourage collaborative (Group Learning) Learning in the class.
4. Ask at least three HOT (Higher order Thinking) questions in the class, which promotes critical thinking.
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop design thinking skills such as the ability to design, evaluate, generalize, and analyze information rather than simply recall it.
6. Introduce Topics in manifold representations.
7. Show the different ways to solve the same problem with different circuits/logic and encourage the students to come up with their own creative ways to solve them.
8. Discuss how every concept can be applied to the real world-and when that's possible, it helps improve the students' understanding.

Module-1

Basic concepts and network theorems

Types of Sources, Loop analysis, Nodal analysis with in dependent DC and AC Excitations. (Text book 1:2.3,4.1,4.2,4.3,4.4,10.6)

Super position theorem, The venin's theorem, Norton's Theorem, Maximum Power transfer Theorem. (Text book 2: 9.2,9.4,9.5,9.7)

Module-2

Twoportnetworks:Short-circuitAdmittanceparameters,Open-circuitImpedanceparameters,Transmissionparameters,Hybrid parameters(Textbook3:11.1,11.2, 11.3, 11.4,11.5)

LaplacetransformanditsApplications:StepRamp,Impulse,SolutionofnetworksusingLaplacetransform,Initial value and final value theorem (Textbook 3:7.1,7.2,7.4,7.7, 8.4)

Module-3

Resonance: Series Resonance: Variation of Current and Voltage with Frequency, Selectivity and Bandwidth, Q-Factor, Circuit Magnification Factor, Selectivity with Variable Capacitance, Selectivity with Variable Inductance.

Parallel Resonance: Selectivity and Bandwidth, Maximum Impedance Conditions with C, L and f Variable, current in Anti-Resonant Circuit, The General Case-Resistance Present in both Branches.

Module-4

Basic Concepts and representation: Types of control systems, effect of feedback systems, differential equation of physical systems (only electrical systems), Introduction to block diagrams, transfer functions, Signal Flow Graphs (Textbook 4: Chapter 1.1, 2.2, 2.4, 2.5, 2.6).

Module-5

Time Response analysis: Time response of first order systems. Time response of second order systems, time response specifications of second order systems (Textbook 4: Chapter 5.3, 5.4) Stability Analysis: Concepts of stability necessary condition for stability, Routh stability criterion, relative stability Analysis (Textbook 4: Chapter 5.3, 5.4, 6.1, 6.2, 6.4, 6.5)

Course outcome (Course Skill Set)

At the end of the course, the student will be able to :

1. Analyse and solve Electric circuit, by applying, loop analysis, Nodal analysis and by applying network Theorems.
2. Evaluate two port parameters of a network and Apply Laplace transforms to solve electric networks.
3. Understand the concept of resonance and determine the parameters that characterize series/parallel resonant circuits.
4. Deduce transfer function of a given physical system, from differential equation representation or Block Diagram representation and SFG representation.
5. Calculate time response specifications and analyse the stability of the system

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50)and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE(Semester End Examination) taken together.

Continuous Internal Evaluation:

- For the Assignment component of the CIE, there are 25 mark sand for the Internal Assessment Test component, there are 25marks.
- The first test will be administered after 40-50% of the syllabus has been covered, and these condtest will be administered after 85-90% of the syllabus has been covered
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The teacher should not conduct two assignments at the end of the semester if two assignments are planned.
- For the course, CIE marks will be based on a scaled-down sum of two tests and other methods of assessment.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks

Suggested Learning Resources:

Text Books

1. Engineering circuit analysis, William HHayt, Jr, Jack EKemmerly, Steven MD urbin, McGraw Hill Education, Indian Edition 8e.
2. Networks and Systems, D Roy Choudhury, New age international Publishers, second edition.
3. Network Analysis, MEV an Valkenburg, Pearson, 3e.
4. Control Systems Engineering, IJ Nagrath, M.Gopal, New age international Publishers, Fifth edition.

Web links and Video Lectures (e-Resources):

- https://nptel.ac.in/courses/108106098
- https://nptel.ac.in/courses/108102042

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

- *Programming Assignments / Mini Projects can be given to improve programming skills*

Sensors and Instrumentation Actuators		Semester	III
Course Code	BVL306B	CIE Marks	50
Teaching Hours/Week(L: T:P: S)	3:0:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	03
Examination type (SEE)	Theory		

Course objectives:

- Explain the characteristics of electrical and electronic measuring instruments.
- Illustrate the working principles of transducers, sensors and actuators.
- Develop and exemplify basic programming skills in Virtual Instrumentation.
- Design and implement a system using sensor and instrumentation configuration.
- Demonstrate the skill set using modern tool for simulation of virtual instrumentation.

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

1. Lecture method (L) does not mean only the traditional lecture method, but a different type of teaching method may be adopted to develop the outcomes.
2. Show Video/animation films to explain the functioning of various techniques.
3. Encourage collaborative (Group) Learning in the class
4. Ask at least three HOTS (Higher-order Thinking) questions in the class, which promotes critical thinking
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.
6. Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
7. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.
8. Incorporate programming examples given under Activity based learning

Module-1

Instrumentation System: Introduction, Input output configuration, Generalized functional elements, Advantages of electronic measurement, Errors in measurement, Gross errors and systematic errors, Absolute and relative errors, static characteristics, dynamic characteristics, calibration and standards-process of calibration.

Module-2

Transducers: Introduction, Electrical transducers, Selecting a transducer, Resistive transducer, Resistive position transducer, Strain gauges, Resistance thermometer, Thermistor, Inductive transducer, Capacitive transducers, Differential output transducers and LVDT. Piezoelectric transducer, photoelectric transducer, Photovoltaic transducer. Temperature transducers. Basics of pressure measurement- Thin plate Diaphragms, Corrugated Diaphragms and Capsules, Bourdon tube elements.

Module-3

Virtual Instrumentation: Introduction, advantages, data types, graphical system design, modular programming, vis and sub-vis loops, arrays, clusters, plotting data, customizing graphs and charts, case structures, formula nodes, timed structures, data acquisition

Module-4

Sensors: Introduction, principles, classification, characterization, Smart sensors: Introduction Primary sensors Information coding/ processing, Data communication, automation. Introduction to MEMS and Microsystems, Microsystems and Microelectronics Multidisciplinary nature of micro system design and manufacture applications of micro systems, Micro sensors, Humidity and Moisture Sensors.

Actuators: Functional components of an actuator, Performance Characteristics of Actuators, Thermo mechanical Actuators, Optical Actuators, Capacitive Actuators, Actuator as a system component, Intelligent & Self sensing actuators, micro actuators, MEMS with micro actuators, Application examples.

Course outcome (Course Skill Set)

At the end of the course, the student will be able to :

1. Demonstrate understanding of MOS transistor theory, CMOS fabrication flow and technology scaling.
2. Draw the basic gates using the stick and layout diagrams with the knowledge of physical design aspects.
3. Interpret Memory elements along with timing considerations
4. Demonstrate knowledge of FPGA based system design
5. Interpret testing and testability issues in VLSI Design
6. Analyze CMOS subsystems and architectural issues with the design constraints.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks

Suggested Learning Resources:

Text Books

1. D.V.S. Murthy: "Transducers and Instrumentation", 2nd Edition, PHI Ltd., 2014.
2. Tai-Ran Hsu: "MEMS & Microsystems Design Manufacture and nanoscale Engineering", 2nd Edition, Tata McGraw Hill, 2008.

4. Hartmut Janocha:"Actuators Basics and Applications", Springer publication 2013.
Web links and Video Lectures (e-Resources):
• https://nptel.ac.in/courses/108105064/34 • https://nptel.ac.in/courses/112103174/3
Activity Based Learning (Suggested Activities in Class)/ Practical Based learning Wireless sensor and actuators, Robotic sensors and actuators, automation using sensors and virtual instrumentation, polymeric sensors.

Computer Organization and Architecture		Semester	III
Course Code	BVL306C	CIE Marks	50
Teaching Hours/Week(L: T:P:S)	3:0:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	03
Examination nature(SEE)	Theory		

Course objectives:

- Understand the organization and architecture of computer systems, their structure and operation
- Illustrate the concept of machine instructions and programs
- Demonstrate different ways of communicating with I/O devices
- Describe different types memory devices and their functions
- Explain arithmetic and logical operations with different data types
- Demonstrate processing unit with parallel processing and pipeline architecture

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teachers can use to accelerate the attainment of the various course out comes.

1. Lecturer method (L) needs not to be only traditional lecture method, but alternative effective teaching methods could be adopted to attain the outcomes.
2. Use of Video/Animation to explain functioning of various concepts.
3. Encourage collaborative (Group Learning) Learning in the class.
4. Ask at least three HOT (Higher order Thinking) questions in the class, which promotes critical thinking.
5. AdoptProblemBasedLearning(PBL),whichfostersstudents'Analyticalskills,developdesignthinking skills such as the ability to design, evaluate, generalize, and analyze information rather than simply recall it.
6. Introduce Topics in mani fold representations.
7. Show the different ways to solve the same problem with different circuits/logic and encourage the students to come up with their own creative ways to solve them.
8. Discuss how every concept can be applied to the real world-and when that's possible, it helps improve the students' understanding.

Module-1

Basic Structure of Computers: Basic Operational Concepts, Bus Structures, Performance – Processor Clock, Basic Performance Equation, Clock Rate, Performance Measurement. Machine Instructions and Programs: Memory Location and Addresses, Memory Operations, Instructions and Instruction Sequencing, Addressing Modes

Textbook 1: Chapter1 – 1.3, 1.4, 1.6 (1.6.1-1.6.4, 1.6.7), Chapter2 – 2.2 to 2.5

Module-2

Input / Output Organization: Accessing I/O Devices, Interrupts – Interrupt Hardware, Direct Memory Access, Buses, Interface Circuits

Textbook 1: Chapter4 – 4.1, 4.2, 4.4, 4.5, 4.6

Module-3

Memory System: Basic Concepts, Semiconductor RAM Memories, Read Only Memories, Speed, Size, and Cost, Cache Memories – Mapping Functions, Virtual memories

Textbook 1: Chapter 5 – 5.1 to 5.4, 5.5 (5.5.1, 5.5.2)

Module-4

Arithmetic: Numbers, Arithmetic Operations and Characters, Addition and Subtraction of Signed Numbers, Design of Fast Adders, Multiplication of Positive Numbers Basic Processing Unit: Fundamental Concepts, Execution of a Complete Instruction, Hardwired control, Micro programmed control

Textbook 1: Chapter2-2.1, Chapter6 – 6.1 to 6.3 Textbook 1: Chapter7 – 7.1, 7.2,7.4, 7.5

Module-5

Pipeline and Vector Processing: Parallel Processing, Pipelining, Arithmetic Pipeline, Instruction Pipeline, Vector Processing, Array Processors

Textbook 2: Chapter 9 – 9.1, 9.2, 9.3, 9.4, 9.6, 9.7

Course outcome (Course Skill Set)

At the end of the course, the student will be able to :

1. Explain the organization and architecture of computer systems with machine instructions and programs
2. Analyze the input/output devices communicating with computer system
3. Demonstrate the functions of different types of memory devices
4. Apply different data types on simple arithmetic and logical unit
5. Analyze the functions of basic processing unit, Parallel processing and pipelining

Assessment Details(both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50)and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE(Semester End Examination) taken together.

Continuous Internal Evaluation:

- For the Assignment component of the CIE, there are 25 marks and for the Internal Assessment Test component, there are 25 marks.
- The first test will be administered after 40 - 50% of the syllabus hasbeencovered,andthesecondtestwillbeadministeredafter85-90% of the syllabus has been covered
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The teacher should not conduct two assignments at the end of the semester if two assignments are planned.
- For the course, CIE marks will be based on a scaled-down sum of two tests and other methods of assessment.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course(**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks

Suggested Learning Resources:

Text Books

1. Carl Hamacher, ZvonkoVranesic, SafwatZaky, Computer Organization, 5th Edition, Tata McGraw Hill
2. M. Morris Mano, Computer System Architecture, PHI, 3rd Edition

Reference:

1. 1. William Stallings: Computer Organization & Architecture, 9th Edition, Pearson

Web links and Video Lectures(e-Resources):

1. https://nptel.ac.in/courses/106/103/106103068/
2. https://nptel.ac.in/content/storage2/courses/106103068/pdf/coa.pdf
3. https://nptel.ac.in/courses/106/105/106105163/
4. https://nptel.ac.in/courses/106/106/106106092/
5. https://nptel.ac.in/courses/106/106/106106166/
6. http://www.nptelvideos.in/2012/11/computer-organization.html

ActivityBasedLearning(SuggestedActivitiesinClass)/PracticalBasedlearning

- Discussion and literature survey on real world use cases • Quizzes

Physics of semiconductor devices		Semester	III
Course Code	BVL306D	CIE Marks	50
Teaching Hours/Week(L: T:P:S)	3:0:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	03
Examination nature(SEE)	Theory		

Course objectives:

- Expound the fundamentals of intrinsic, extrinsic semiconductors with carrier concentration, modeling and physics of various carrier current transport mechanisms
- Introduce detailed physics and modeling of PN Junction, MOS capacitors, and MOSFETs

Teaching-Learning Process(General Instructions)

These are sample Strategies, which teachers can use to accelerate the attainment of the various course out comes.

1. Lecturer method (L) needs not to be only traditional lecture method, but alternative effective teaching methods could be adopted to attain the outcomes.
2. Use of Video/ Animation to explain functioning of various concepts.
3. Encourage collaborative (Group Learning) Learning in the class.
4. Ask at least three HOT (Higher order Thinking) questions in the class, which promotes critical thinking.
5. Adopt Problem Based Learning(PBL) ,which fosters students' Analytical skills, developed sign thinking skills such as the ability to design, evaluate, generalize, and analyze information rather than simply recall it.
6. Introduce Topics in manifold representations.
7. Show the different ways to solve the same problem with different circuits/logic and encourage the students to come up with their own creative ways to solve them.
8. Discuss how every concept can be applied to the real world-and when that's possible, it helps improve the students' understanding.

Module-1

Semiconductor Physics: Energy bands in solids - Intrinsic and Extrinsic semiconductors - Direct and Indirect bandgap - Density of states - Fermi distribution -Free carrier densities - Boltzmann statistics - Thermal equilibrium.

Carrier Transport in Semi conductors : Current flow mechanisms: Drift current, Diffusion current - Mobility of carriers - Current density equations - Continuity equation.

Module-2

P-N Junctions: Thermal equilibrium physics - Energy band diagrams - Space charge layers - Poisson equation - Electric fields and Potentials - p-n junction under applied bias - Static current-voltage characteristics of p-n junctions - Breakdown mechanisms.

Module-3

MOS Capacitor : Accumulation - Depletion - Strong inversion - Threshold voltage - Contact potential - Gate work function - Oxide and Interface charges - Body effect - C-V characteristics of MOS

Module-4

MOSFETs and Compact Models: Drain current - Saturation voltage - Sub-threshold conduction - Effect of gate and drain voltage on carrier mobility - Compact models for MOSFET and their implementation in SPICE: Level 1, 2 and 3 - MOS model parameters in SPICE

Module-5

Scaling and Short Channel Effects: Effect of scaling - Channel length modulation - Punch-through - Hot carrier degradation - MOSFET breakdown - Drain-induced barrier lowering.
Effect of tox - Effect of high-k and low-k dielectrics on the gate leakage and Source and drain leakage

Course outcome (Course Skill Set)

At the end of the course, the student will be able to :

1. Design extrinsic semiconductors with specific carrier concentrations and, understand the band structure and diagrams of semiconductors.
2. Calculate and model the carrier transport mechanism in semiconductors.
3. Model PN- junctions of given specifications
4. Model MOS capacitors
5. Classify and Analyze the various circuit configurations of Transistor and MOSFETs.

Assessment Details(both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50)and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- For the Assignment component of the CIE, there are 25 marks and for the Internal Assessment Test component, there are 25marks.
- The first test will be administered after 40-50% of the syllabus has been covered, and these condtest will be administered after 85-90% of the syllabus has been covered
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The teacher should not conduct two assignments at the end of the semester if two assignments are planned.
- For the course, CIE marks will be based on a scaled-down sum of two tests and other methods of assessment.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course(**duration03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks

Suggested Learning Resources:

Text Books

1. Ben G. Streetman and S. Banerjee, Solid State Electronic Devices, Pearson Education, U.S, Seventh Edition, 2014.

Publishers, US, 2017.

Reference:

1. Y.P. Tsividis and Colin McAndrew, Operation and Modelling of the MOS Transistor, Oxford University Press, US, Third Edition, 2011.
2. M K Achutan and K N Bhatt, Fundamental of Semiconductor Devices, McGraw Hill Education, US, 2017.

Weblinks and Video Lectures(e-Resources):

- Semiconductor Devices and Circuits - Course (nptel.ac.in)
- NPTEL :: Electrical Engineering - NOC:Semiconductor Devices and Circuits
- NPTEL :: Electronics & Communication Engineering - Solid State Devices

ActivityBasedLearning(SuggestedActivitiesinClass)/PracticalBasedlearning

- Quizzes, Seminars

FPGA Based System design Using Verilog		Semester	IV
Course Code	**BVL401**	CIE Marks	50
Teaching Hours/Week (L: T:P: S)	3:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	03
Examination type (SEE)	THEORY		

Course objectives:

This course will enable students to:

- Understand the types programmable logic devices and building blocks of FPGA and thus implement the design using Xilinx FPGAs.
- Understand the concepts of Advanced Logic design and implementation using Verilog HDL
- Designing different Digital applications using SM chart .

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

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1. Lecture method (L) does not mean only traditional lecture method, but different types of teaching methods may be adopted to develop the outcomes.
2. Encourage collaborative (Group) Learning in the class.
3. Ask at least three HOTS (Higher Order Thinking) questions in the class, which promotes criticalthinking.
4. Adopt Problem-Based Learning (PBL), which fosters students' Analytical skills, and develops thinking skillssuch as the ability to evaluate, generalize, and analyze information rather than simply recall it.
5. Topics will be introduced in a multiple representation.
6. Show the different ways to solve the same problem and encourage the students to come up withcreative ways to solve them.
7. Discuss how every concept can be applied to the real world and when that's possible, it helps improve the student's understanding.
8. Adopt the Flipped class technique by sharing the materials/Sample Videos before the class and having discussions on the topic in the succeeding classes.

Module-1

Introduction to Programmable Logic Devices:

Hazards in Combinational Circuits, Brief overview of Programmable Logic Devices, Simple Programmable Logic Devices (SPLDs)
Complex Programmable Logic devices (CPLDs), Field-Programmable Gate Arrays (FPGAs)

(**Text 1: 1.5,3.1,3.2 , 3.3, 3.4) RBT Level:** L1, L2, L3

Module-2

Advanced Digital Design Examples:

BCD to 7-Segment Display Decoder, BCD Adder, Traffic Light controller, Synchronization and debouncing, Shift-and-Add Multiplier
Array Multiplier, A Signed Integer/Fraction Multiplier, (Excluding Test Bench) , Keypad Scanner

Module-3
SM Charts and Microprogramming : State Machine Charts, Derivation of SM Charts, SM chart for binary multiplier , Dice Game (Excluding Test Bench) , Realization of SM Charts , Implementation of the Dice Game . Microprogramming , Linked State Machines. **(Text 1: 5.1, 5.2, 5.3 , 5.4 , 5.5 , 5.6) RBT Level:** L1, L2, L3
Module-4
Floating-Point Arithmetic: Representation of Floating-Point Numbers, Floating-Point Multiplication, Floating-Point Addition, Other Floating-Point Operations. Multivalued Logic and Signal Resolution, Built-in Primitives, User-Defined Primitives, SRAM Model, Rise and Fall Delays of Gates, Rise and Fall Delays of Gates **(Text 1:7.1,7.2, 7.3,7.4, 8.3, 8.4, 8.5,8.6,8.8) RBT Level:** L1, L2, L3
Module-5
Designing with Field Programmable Gate Arrays : Implementing Functions in FPGAs, Implementing Functions Using Shannon's Decomposition Carry Chains in FPGAs , Cascade Chains in FPGAs , Examples of Logic Blocks in Commercial FPGAs , Examples of Logic Blocks in Commercial FPGAs, Dedicated Multipliers in FPGAs, FPGAs Capacity: Maximum gates versus Usable gates , Design Translation. **(Text 1: 6.1,6.2,6.3, 6.4 ,6.5 , 6.6, 6.7, 6.8,6.10, 6.11) RBT Level:** L1, L2, L3
Course outcome (Course Skill Set) At the end of the course the student will be able to: 1. Apply the concept of Programmable logic devices to implement digital design. 2. Design and implementation of Advanced logic design using Verilog HDL 3. Understand the concept of SM Chart and how design complex digital circuits using SM Chart. 4. Performing the Floating-point arithmetic operations and designing of Memories 5. Designing and performance evaluation of advanced digital design using FPGAs

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
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- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.

Suggested Learning Resources:

Text Book:

1 Digital Systems Design Using Verilog First Edition, Charles H. Roth, Jr. The University of Texas at Austin, Lizy Kurian John The University of Texas at Austin, Byeong Kil Lee The University of Texas at San Antonio

Reference Books:

1. Advanced FPGA Design Architecture, Implementation, and Optimization Steve Kilts Spectrum
2. ASIC and FPGA Verification: A guide to component Modelling.
Richard Munden, Morgan Kaufmann Publishers is an imprint of Elsevier
3. Processor Design . System-on-Chip Computing for ASICs and FPGAs, Jari Nurmi Finland

Tampere University of Technology Sringer Publications.

4. The design Warrior's guide to FPGA Clive 'Max' Maxfield Elsevier Publications

Activity Based Learning (Suggested Activities in Class)/Practical-Based Learning

- Group Discussion/Quiz
- Demonstration of Verilog and FPGA concepts.
- Case Study on small design and implementation on FPGA's

PRINCIPLES OF COMMUNICATION SYSTEMS		Semester	4
Course Code	**BVL402**	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:2:0	SEE Marks	50
Total Hours of Pedagogy	40 hours Theory + 8-10 Lab slots	Total Marks	100
Credits	04	Exam Hours	03
Examination nature (SEE)	Theory/practical/Viva-Voce /Term-work/Others		

Course objectives:

This course will enable students to

- Understand and analyse concepts of Analog Modulation schemes viz; AM, FM
- Design and analyse the electronic circuits for AM and FM modulation and demodulation.
- Understand the concepts of random variable and random process to model communication systems.
- Understand and analyse the concepts of digitization of signals.
- Evolve the concept of SNR in the presence of channel induced noise

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teacher can use to accelerate the attainment of the various course outcomes.

1. Lecture method (L) does not mean only traditional lecture method, but different type of teaching methods may be adopted to develop the outcomes.
2. Show Video/animation films to explain evolution of communication technologies.
3. Encourage collaborative (Group) Learning in the class.
4. Ask at least three HOTS (Higher order Thinking) questions in the class, which promotes critical thinking.
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.
6. Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
7. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.

MODULE-1

Random Variables and Processes: Introduction, Probability, Conditional Probability, Random variables. Statistical Averages: Function of a random variable, Moments, Random Processes, Mean, Correlation and Covariance function: Properties of autocorrelation function, Cross–correlation functions, Gaussian Process: Gaussian Distribution Function.

[Text 2: 5.1, 5.2,5.3,5.4,5.5,5.6,5.9]

RBT: L1,L2

MODULE-2

Amplitude Modulation Fundamentals:AM Concepts, Modulation index and Percentage of Modulation, Sidebands and the frequency domain, AM Power, Single Sideband Modulation.

AM Circuits: Amplitude Modulators: Diode Modulator, Transistor Modulator, collector Modulator. Amplitude Demodulators: Diode Detector, Balanced Modulators: Lattice Modulators.

Frequency Division Multiplexing: Transmitter-Multiplexer, Receiver-Demultiplexer.

[Text1: 3.1, 3.2,3.3,3.4,3.5,4.2,4.3,4.4,10.2]

RBT: L1, L2, L3

MODULE-3

Fundamentals of Frequency Modulation: Basic Principles of Frequency Modulation, Principles of Phase Modulation, Modulation index and sidebands, Noise Suppression Effects of FM, Frequency Modulation versus Amplitude Modulation.

FM Circuits: Frequency Modulators: Voltage Controlled Oscillators. , Frequency Demodulators:Slope Detectors, Phase Locked Loops.

Communication Receiver: Super heterodyne receiver, Frequency Conversion: Mixing Principles, JFET Mixer.

[Text1: 5.1,5.2,5.3,5.4,5.5,6.1,6.3,9.2,9.3]

RBT: L1, L2, L3

MODULE-4
Digital Representation of Analog Signals: Introduction, Why Digitize Analog Sources?, The Sampling process, Pulse Amplitude Modulation, Time-Division Multiplexing, Pulse Position Modulation: Generation and Detection of PPM wave.The Quantization Process. Pulse Code Modulation: Sampling, Quantization, Encoding, line Codes, Differential encoding, Regeneration, Decoding, filtering, multiplexing. **[Text2: 7.1,7.2,7.3,7.4,7.5,7.6,7.8,7.9]** **RBT: L1,L2,L3**
MODULE-5
Baseband Transmission of Digital signals: Introduction, Intersymbol Interference, Eye Pattern, Nyquist criterion for distortionless Transmission, Baseband M-ary PAM Transmission. **[Text2:8.1,8.4,8.5,8.6,8.7]** **Noise:** Signal to Noise Ratio, External Noise, Internal Noise, Semiconductor Noise, Expressing Noise Levels, Noise in Cascade Stages. **[Text1:9.5]** **RBT:L1,L2,L3**

PRACTICAL COMPONENT OF IPCC*(Experiments can be conducted using MATLAB/SCILAB/OCTAVE)*

Sl.NO	Experiments
1	Basic Signals and Signal Graphing: a) unit Step, b) Rectangular, c) standard triangle d) sinusoidal and e) Exponential signal.
2	Illustration of signal representation in time and frequency domains for a rectangular pulse.
3	Amplitude Modulation and demodulation: Generation and display the relevant signals and its spectrums.
4	Frequency Modulation and demodulation: Generation and display the relevant signals and its spectrums.
5	Sampling and reconstruction of low pass signals. Display the signals and its spectrum.
6	Time Division Multiplexing and demultiplexing.
7	PCM Illustration: Sampling, Quantization and Encoding
8	Generate a)NRZ, RZ and Raised cosine pulse, b) Generate and plot eye diagram
9	Generate the Probability density function of Gaussian distribution function.
10	Display the signal and its spectrum of an audio signal.

Course outcomes (Course Skill Set):

At the end of the course, the student will be able to:

1. Understand the principles of analog communication systems and noise modelling.
2. Identify the schemes for analog modulation and demodulation and compare their performance.
3. Design of PCM systems through the processes sampling, quantization and encoding.
4. Describe the ideal condition, practical considerations of the signal representation for baseband transmission of digital signals.
5. Identify and associate the random variables and random process in Communication system design.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

The IPCC means the practical portion integrated with the theory of the course. CIE marks for the theory component are **25 marks** and that for the practical component is **25 marks**.

CIE for the theory component of the IPCC

- 25 marks for the theory component are split into **15 marks** for two Internal Assessment Tests (Two Tests, each of 15 Marks with 01-hour duration, are to be conducted) and **10 marks** for other assessment methods mentioned in 22OB4.2. The first test at the end of 40-50% coverage of the syllabus and the second test after covering 85-90% of the syllabus.
- Scaled-down marks of the sum of two tests and other assessment methods will be CIE marks for the theory component of IPCC (that is for **25 marks)**.
- The student has to secure 40% of 25 marks to qualify in the CIE of the theory component of IPCC.

CIE for the practical component of the IPCC

- **15 marks** for the conduction of the experiment and preparation of laboratory record, and **10 marks** for the test to be conducted after the completion of all the laboratory sessions.
- On completion of every experiment/program in the laboratory, the students shall be evaluated including viva-voce and marks shall be awarded on the same day.
- The CIE marks awarded in the case of the Practical component shall be based on the continuous evaluation of the laboratory report. Each experiment report can be evaluated for 10 marks. Marks of all experiments' write-ups are added and scaled down to **15 marks**.
- The laboratory test **(duration 02/03 hours)** after completion of all the experiments shall be conducted for 50 marks and scaled down to **10 marks.**
- Scaled-down marks of write-up evaluations and tests added will be CIE marks for the laboratory component of IPCC for **25 marks**.
- The student has to secure 40% of 25 marks to qualify in the CIE of the practical component of the IPCC.

SEE for IPCC

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours**)

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored by the student shall be proportionally scaled down to 50 Marks

The theory portion of the IPCC shall be for both CIE and SEE, whereas the practical portion will have a CIE component only. Questions mentioned in the SEE paper may include questions from the practical component.

- The minimum marks to be secured in CIE to appear for SEE shall be 10 (40% of maximum marks-25) in the theory component and 10 (40% of maximum marks -25) in the practical component. The laboratory component of the IPCC shall be for CIE only. However, in SEE, the questions from the laboratory component shall be included**.** The maximum of 04/05 sub-questions are to be set from the practical component of IPCC, the total marks of all questions should not be more than 20 marks.
- SEE will be conducted for 100 marks and students shall secure 35% of the maximum marks to qualify for the SEE. Marks secured will be scaled down to 50.
- The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Suggested Learning Resources:

Books

1. Louis E Frenzel, Principles of Electronic Communication Systems, 3rd Edition, Mc Graw Hill Education (India) Private Limited, 2016. ISBN: 978-0-07-066755-6.
2. Simon Haykin &Michael Moher, Communication Systems, 5th Edition, John Wiley, India Pvt. Ltd, 2010, ISBN: 978-81-265-2151-7.

Reference Books

1. B.P.Lathi, Zhi Ding, "Modern Digital and Analog Communication Systems", Oxford University Press, 4th

edition, 2010, ISBN: 97801980738002.
2. Herbert Taub, Donald L Schilling, Goutam Saha, "Principles of Communication systems", 4th Edition, Mc Graw Hill Education (India) Private Limited, 2016. ISBN: 978-1-25-902985-1

Web links and Video Lectures (e-Resources):

1. Principles of Communication Systems**https://nptel.ac.in/courses/108104091**
2. Communication Engineering **https://nptel.ac.in/courses/117102059**

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

1. Assignments and test – Knowledge level, Understand Level and Apply level
2. Experiential Learning by using free and open source software's SCILAB or OCTAVE
3. Open ended questions by faculty, Open ended questions from students

VISVESVARAYA TECHNOLOGICAL UNIVERSITY, BELAGAVI
B.E: Electronics & Communication Engineering / B.E: Electronics & Telecommunication EngineeringNEP, Outcome Based Education (OBE) and Choice Based Credit System (CBCS)
(Effective from the academic year 2023 – 24)

IV Semester

Control Systems			
Course Code	**BVL403**	CIE Marks	50
Teaching Hours/Week (L: T: P)	(3:0:2)	SEE Marks	50
Total Hours of Pedagogy	40 hours Theory + 12 Lab slots	Total Marks	100
Credits	04	Exam Hours	03

Course objectives: This course will enable students to:

1. Understand basics of control systems and design mathematical models using block diagram reduction, SFG, etc.
2. Understand Time domain and Frequency domain analysis.
3. Analyze the stability of a system from the transfer function
4. Familiarize with the State Space Model of the system.

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teacher can use to accelerate the attainment of the various course outcomes.

- Lecture method (L) does not mean only traditional lecture method, but different type of teaching methods may be adopted to develop the outcomes.
- Show Video/animation films to explain the different concepts of Linear Algebra & Signal Processing.
- Encourage collaborative (Group) Learning in the class.
- Ask at least three HOTS (Higher order Thinking) questions in the class, which promotes critical thinking.
- Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.
- Topics will be introduced in a multiple representation.
- Show the different ways to solve the same problem and encourage the students to come up withtheir own creative ways to solve them.
- Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.
- Adopt Flipped class technique by sharing the materials / Sample Videos prior to the class and havediscussions on the that topic in the succeeding classes.
- Give Programming Assignments.

Module-1

Introduction to Control Systems: Types of Control Systems, Effect of Feedback Systems, Differential equation of Physical Systems -Mechanical Systems, Electrical Systems, Analogous Systems. (Textbook 1: Chapter 1.1, 2.2)

Teaching-LearningProcess	Chalk and Talk, YouTube videos **RBT Level:** L1, L2, L3

Module-2	
Block diagrams and signal flow graphs: Transfer functions, Block diagram algebra and Signal Flow graphs. (Textbook 1: Chapter 2.4, 2.5, 2.6)	
Teaching-LearningProcess	Chalk and Talk, YouTube videos, Any software tool to implement block diagram reduction techniques and Signal Flow graphs **RBT Level:** L1, L2, L3
Module-3	
Time Response of feedback control systems: Standard test signals, Unit step response of First and Second order Systems. Time response specifications, Time response specifications of second order systems, steady state errors and error constants. Introduction to PI, PD and PID Controllers (excluding design). (Textbook 1: Chapter 5.3, 5.4, 5.5)	
Teaching-LearningProcess	Chalk and Talk, YouTube videos, Any software tool to show time response for various transfer functions and PI, PD and PID controllers. **RBT Level:** L1, L2, L3
Module-4	
Stability analysis: Concepts of stability, Necessary conditions for Stability, Routh stability criterion, Relative stability analysis: more on the Routh stability criterion. **Introduction to Root-Locus Techniques**, The root locus concepts, Construction of root loci. (Textbook 1: Chapter 6.1, 6.2, 6.4, 6.5, 7.1, 7.2, 7.3)	
Teaching-LearningProcess	Chalk and Talk, YouTube videos, Any software tool to plot Root locus for various transfer functions **RBT Level:** L1, L2, L3
Module-5	
Frequency domain analysis and stability: Correlation between time and frequency response, Bode Plots, Experimental determination of transfer function. (Textbook 1: Chapter 4: 8.1, 8.2, 8.4) Mathematical preliminaries, Nyquist Stability criterion, (Stability criteria related to polar plots are excluded) (Textbook 1: 9.2, 9.3) **State Variable Analysis:** Introduction to state variable analysis: Concepts of state, state variable and state models. State model for Linear continuous –Time systems, solution of state equations. (Textbook 1: 12.2, 12.3, 12.6)	
Teaching-LearningProcess	Chalk and Talk, YouTube videos, Any software tool to draw Bode plot for various transfer functions **RBT Level:** L1, L2, L3

PRACTICAL COMPONENT OF IPCC Using suitable simulation software (P-Spice/ MATLAB / Python / Scilab / OCTAVE / LabVIEW) demonstrate the operation of the following circuits:	
Sl.No	**Experiments**
1	Implement Block diagram reduction technique to obtain transfer function a control system.
2	Implement Signal Flow graph to obtain transfer function a control system.
3	Simulation of poles and zeros of a transfer function.
4	Implement time response specification of a second order Under damped System, for different damping factors.
5	Implement frequency response of a second order System.
6	Implement frequency response of a lead lag compensator.
7	Analyze the stability of the given system using Routh stability criterion.
8	Analyze the stability of the given system using Root locus.
9	Analyze the stability of the given system using Bode plots.
10	Analyze the stability of the given system using Nyquist plot.
11	Obtain the time response from state model of a system.
12	Implement PI and PD Controllers.

Course Outcomes

At the end of the course the student will be able to:

1. Deduce transfer function of a given physical system, from differential equation representation or Block Diagram representation and SFG representation.
2. Calculate time response specifications and analyse the stability of the system.
3. Draw and analyse the effect of gain on system behaviour using root loci.
4. Perform frequency response Analysis and find the stability of the system.
5. Represent State model of the system and find the time response of the system.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together

CIE for the theory component of IPCC

Two Tests each of **20 Marks (duration 01 hour**)

- First test at the end of 5^{th} week of the semester
- Second test at the end of the 10^{th} week of the semester

Two assignments each of **10 Marks**

- First assignment at the end of 4^{th} week of the semester
- Second assignment at the end of 9^{th} week of the semester

Scaled-down marks of two tests and two assignments added will be CIE marks for the theory component of IPCC for **30 marks**.

CIE for the practical component of IPCC

- On completion of every experiment/program in the laboratory, the students shall be evaluated and marks shall be awarded on the same day. The **15 marks** are for conducting the experiment and preparation of the laboratory record, the other **05 marks shall be for the test** conducted at the end of the semester.
- The CIE marks awarded in the case of the Practical component shall be based on the continuous evaluation of the laboratory report. Each experiment report can be evaluated for 10 marks. Marks of all experiments' write-ups are added and scaled down to 15 marks.
- The laboratory test **(duration 03 hours)** at the end of the 15^{th} week of the semester /after completion of all the experiments (whichever is early) shall be conducted for 50 marks and scaled down to 05 marks**.**
- Scaled-down marks of write-up evaluations and tests added will be CIE marks for the laboratory component of IPCC for **20 marks**.

SEE for IPCC

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (duration 03 hours)

- The question paper will have ten questions. Each question is set for 20 marks.
- There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
- The students have to answer 5 full questions, selecting one full question from each module.

The theory portion of the IPCC shall be for both CIE and SEE, whereas the practical portion will have a CIE component only. Questions mentioned in the SEE paper shall include questions from the practical component.

- The minimum marks to be secured in CIE to appear for SEE shall be the 12 (40% of maximum marks-30) in the theory component and 08 (40% of maximum marks -20) in the practical component. The laboratory component of the IPCC shall be for CIE only. However, in SEE, the questions from the laboratory component shall be included**.** The maximum of 04/05 questions to be set from the practical component of IPCC, the total marks of all questions should not be more than the 20 marks.

SEE will be conducted for 100 marks and students shall secure 35% of the maximum marks to qualify inthe SEE. Marks secured out of 100 shall be reduced proportionally to 50.

Suggested Learning Resources:

Text Books

1. Control Systems Engineering, I J Nagrath, M. Gopal, New age international Publishers, Fifth edition.

Web links and Video Lectures (e-Resources):

- https://nptel.ac.in/courses/108106098

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

Programming Assignments / Mini Projects can be given to improve programming skills

FPGA Based System design Lab Using Verilog		Semester	4
Course Code	**BVLL404**	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	0:0:2	SEE Marks	50
Credits	01	Exam Hours	02
Examination type (SEE)	Theory/Practical/Viva-Voce /Term-work/Others		

Course objectives:

This laboratory course enables students to

- Understand FPGA Design flow for VLSI Chip Design
- Understand the concept of Design and implementation of Advanced Digital System Design
- Learning the Implementation of advanced digital circuits on FPGA boards

	Verilog Program can be compile using any compiler ,Verifying the functionality using suitable simulator. Down load the programs on FPGA boards and Verify the Functionality
1	Write Verilog program for the following combinational logic, verify the design using test bench and perform the synthesis by downloading the design on to FPGA device. a. Structural modelling of Full adder using two half adders and or Gate b. BCD to Excess-3 code converter
2	Write Verilog program for the following Sequential Circuits, verify the design using test bench and perform the synthesis by downloading the design on to FPGA device. a. Mod-N counter b. Random sequence counter
3	Write Verilog program for the following Sequential Circuits, verify the design using test bench and perform the synthesis by downloading the design on to FPGA device. a. SISO and PISO shift register b. Ring counter
4	Write Verilog program for the following Digital Circuits, verify the functionality using test bench and perform the synthesis by downloading the design on to FPGA device. a.4-Bit Ripple Carry Adder b. 4-Bit Linear Feedback shift register
5	Write Verilog program for the following Digital Circuits, verify the functionality using test bench and perform the synthesis by downloading the design on to FPGA device. a. 4-bit Array Multiplication b. 4-bit Booth Multiplication

6	Write a Verilog code to design a clock divider circuit that generates 1/2, 1/3rdand 1/4thclock from a given input clock. Port the design to FPGA and validate the functionality through oscilloscope.
7	Interface a Stepper motor to FPGA and write Verilog code to control Stepper motor rotation.
8	Interface a DAC to FPGA and write Verilog code to generate Squre wave of frequency F KHz. Modify the code to down sample the frequency to F/2 KHz. Display the original and Down sampled signals by connecting them to an oscilloscope.
9	Write Verilog code to convert an analog input of a sensor to digital form and to display the same on a suitable display like set of simple LEDs like 7-Segment display digits.

Course outcomes:

- Familiarize with the EDA tool to write HDL programs to understand simulation and synthesis of digital design.
- Design, Simulation and Synthesis of Combinational circuits using EDA tool
- Design, Simulation and Synthesis of Sequential Circuits using EDA tool
- Interfacing DAC to FPGA device to generate different waveforms using Verilog HDL.
- Interfacing Stepper motor to FPGA device to count the number of rotations of a stepper motor.

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Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation (CIE):

CIE marks for the practical course are **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment is to be evaluated for conduction with an observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments are designed by the faculty who is handling the laboratory session and are made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled down to **30 marks** (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct a test of 100 marks after the completion of all the experiments listed in the syllabus.
- In a test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability.
- The marks scored shall be scaled down to **20 marks** (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and marks of a test is the total CIE marks scored by the student.

Semester End Evaluation (SEE):

- SEE marks for the practical course are 50 Marks.
- **SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the Head of the Institute**.
- The examination schedule and names of examiners are informed to the university before the conduction of the examination. These practical examinations are to be conducted between the schedule mentioned in the academic calendar of the University.
- All laboratory experiments are to be included for practical examination.
- (Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.
- Students can pick one question (experiment) from the questions lot prepared by the examiners jointly.
- Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.

General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)

Change of experiment is allowed only once and 15% of Marks allotted to the procedure part are to be made zero.

The minimum duration of SEE is 02 hours

Suggested Learning Resources:

1) SamirPalnitkar, "Verilog HDL : A guide to digital design and synthesis", Pearson Education, II Edition.

2) Donald E Thomas, Philip R Moorby, “The Verilog hardware description Language”, Springer Science Business Media , LLC, 5th Edition

3) Michael D. Ciletti, “Advanced digital design with the Verilog HDL”, Pearson (PHI),II Edition

4) Padmanabhan, Tripura Sunadri, “Design through Verilog HDL”, Wiley, 2016.

5) Verilog HDL user manual

MICROCONTROLLERS		Semester	4
Course Code	BVL405A	CIE Marks	50
Teaching Hours/Week(L:T:P)	3:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	3
Examination type(SEE)	Theory		

Course objectives:

This course will enable students to:

- Understand the difference between Microprocessor and Microcontroller and embedded microcontrollers.
- Analyze the basic architecture of 8051microcontroller.
- Program 8051 microcontroller using Assembly Language and C.
- Understand the operation and use of inbuilt Timers/Counters and Serial port of 8051
- Understand the interrupt structure of 8051 and Interfacing I/O devices using I/O ports of 8051.

Teaching-Learning Process(General Instructions)

The samples strategies, which the teacher can use to accelerate the attainment of the various course outcomes are listed in the following:

1. Lecture method (L) does not mean only the traditional lecture method, but a different type of teaching method may be adopted to develop the outcomes.
2. Show Video/animation films to explain the functioning of various techniques.
3. Encourage collaborative(Group)Learning in the class
4. Ask at least three HOTS(Higher-order Thinking) questions in the class, which promotes critical thinking
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical kills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.
6. Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
7. Discuss how every concept can be applied to the real world and when that's possible, it helps improve the students' understanding.
   Give Programming Assignments.

	RBT Level
Module-1 (8 Hrs)	
Microcontroller: Microprocessor Vs Microcontroller, Micro controller & Embedded Processors, Processor Architectures-Harvard Vs Princeton & RISC Vs CISC , 8051 Architecture- Registers, Pin diagram, I/O ports functions, Internal Memory organization. External Memory (ROM & RAM) interfacing. (Text book 1-1.1,Text book 2-1.0,1.1,3.0,3.1,3.2,3.3 Text book 3-Pg 5-9)	L1,L2
Module-2 (8 Hrs)	
Instruction Set: 8051 Addressing Modes, Data Transfer Instructions, Arithmetic instructions, Logical Instructions, Jump & Call Instructions Stack & Subroutine Instructions of 8051 (with examples in assembly Language). (Text book 2- Chapter 5,6,7,8, **Additional reading Refer Textbook 3, Chapter 3 for complete understanding of instructions with**	L1,L2

Module-3 (8 Hrs)	
Timers/Counters & Serial port programming: Basics of Timers & Counters, Data types & Time delay in the 8051 using C, Programming 8051 Timers, Mode 1 & Mode 2 Programming, Counter Programming (Assembly Language only). (Text book 2- 3.4, Text book 1- 7.1, 9.1,9.2) Basics of Serial Communication, 8051 Connection to RS232, Programming the 8051 to transfer data serially & to receive data serially using C.(Text book 2- 3.5, Text book 1- 10.1,10.2,10.3 except assembly language programs, 10.5)	**L1,L2, L3**
Module-4 (8 Hrs)	
Interrupt Programming: Basics of Interrupts, 8051 Interrupts, Programming Timer Interrupts, Programming Serial Communication Interrupts, Interrupt Priority in 8051(Assembly Language only) (Text book 2- 3.6, Text book 1- 11.1,11.2,11.4, 11.5)	**L1,L2, L3**
Module-5 (8 Hrs)	
I/O Port Interfacing & Programming: I/O Programming in 8051 C, LCD interfacing, DAC 0808 Interfacing, ADC 0804 interfacing, Stepper motor interfacing, DC motor control & Pulse Width Modulation (PWM) using C only. (Text book 1- 7.2, 12.1, 13.1, 13.2, 17.2, 17.3)	**L1, L2, L3**

Course outcome (Course Skill Set)

At the end of the course, students will be able to:

1. Describe the difference between Microprocessor and Microcontroller, Types of Processor Architectures and Architecture of 8051Microcontroller.
2. Discuss the types of 8051 Microcontroller Addressing modes & Instructions with Assembly Language Programs.
3. Explain the programming operation of Timers/Counters and Serial port of 8051 Microcontroller.
4. Illustrate the Interrupt Structure of 8051 Microcontroller & its programming.
5. Develop C programs to interface I/O devices with 8051 Microcontroller.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE)is 50%.The minimum passing mark for the CIE is 40%of the maximum marks(20marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- There are 25marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25marks.The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the courses hall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20marks.
2. There will be 2questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to50 marks

Suggested Learning Resources:

TEXT BOOKS

1. The "8051 Microcontroller and Embedded Systems – Using Assembly and C", Muhammad Ali Mazidi and Janice Gillespie Mazidi and Rollind. Mckinlay; Phi, 2006 / Pearson, 2006.
2. "The 8051 Microcontroller", Kenneth j. Ayala, 3rd edition, Thomson/Cengage Learning.
3. "Programming And Customizing The 8051 Microcontroller".,Myke Predko Tata Mc Graw-Hill Edition 1999 (reprint 2003).

REFERENCEBOOKS:

1. "The 8051 Microcontroller Based Embedded Systems", Manish K Patel, McGraw Hill, 2014, ISBN: 978-93-329-0125-4.
2. "Microcontrollers: Architecture, Programming, Interfacing and System Design", Raj Kamal, Pearson Education, 2005.

Web links and Video Lectures(e-Resources):

https://youtu.be/pA6K5NgWTow?si=zQqqgXQq50dVL_-s

Industrial Electronics		Semester	IV
Course Code	BVL405B	CIE Marks	50
Teaching Hours/Week (L: T:P: S)	3:0:0	SEE Marks	50
Total Hours of Pedagogy	40 hours	Total Marks	100
Credits	03	Exam Hours	03
Examination type (SEE)	Theory		

Course objectives: This course will enable student to

- Explain broad types of industrial power devices, there structure, and its characteristics.
- Design and analyse the broad categories of power electronic circuits.
- Explain various types of MEMs devices, principle of operation and construction.
- Familiarize with soft core processors and computer architecture.
- Apply protective methods for devices and circuits.

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

1. Lecture method (L) does not mean only traditional lecture method, but different type of teaching methods may be adopted to develop the outcomes.
2. Show Video/animation films to explain evolution of communication technologies.
3. Encourage collaborative (Group) Learning in the class.
4. Ask at least three HOTS (Higher order Thinking) questions in the class, which promotes critical thinking.
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.
6. Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
7. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.

Module-1

Industrial Power Devices: General purpose power diodes, fast recovery power diodes, schottky power diodes, silicon carbide power diodes **(Text book 1: 2.5, 2.6)**, Power MOSFETs, Steady state characteristics, switching characteristics, silicon carbide MOSFETs, COOLMOS, Junction field effect transistors, operation and characteristics of JFETs, Silicon Carbide JFET structures, Bipolar Junction Transistors, Steady state characteristics, switching characteristics, silicon carbide BJTs, IGBT, silicon carbide IGBTs **(Text book 1: 4.3, 4.4, 4.6, 4.7**

Module-2

Power Electronics Circuits:), Thyristor, Thyristor characteristics, two transistor model **(Text book 1: 9.2, 9.3, 9.4)**.Controlled Rectifiers – Single phase full converter with R and RL load, Single phase dual converters, and Three phase full converter with RL load **(Text book 1: 10.2, 10.3, 10.4)**.

Switching mode regulators – Buck Regulator, Boost regulator, Buck – Boost regulator, comparison of regulators **(Text book 1: 5.9.1, 5.9.2, 5.9.3, 5.10)**

Module-3

Inverters – Principle of operation, Single phase bridge inverter, Three phase inverter with 180 and 120 degree conduction, Current source inverter **(Text book 1: 6.3, 6.4, 6.5, 6.9)**.

AC voltage controllers – Single phase full wave controller with resistive load, single phase full wave controller with inductive load **(Text book 1: 11.3, 11.4)**.

Module-4

MEMS Devices: Sensing and Measuring Principles, Capacitive Sensing, Resistive Sensing, Piezoelectric Sensing, Thermal Transducers, Optical Sensors, Magnetic Sensors, MEMS Actuation Principles, Electrostatic Actuation, Thermal Actuation, Piezoelectric Actuation, Magnetic Actuation, MEMS Devices Inertial Sensors, Pressure Sensors, Radio Frequency MEMS: Capacitive Switches and Phase Shifters, Microfluidic Components, Optical Devices. **(Text book 2: 13.1, 13.3, 13.4)**

MEMS Applications: Introduction, Industrial, Automotive, Biomedical (**Text book 2:15.1, 15.2, 15.3, 15.4)**

Module-5

Protections of Devices and Circuits: Cooling and Heat sinks, Thermal Modeling of Power Switching Devices, Electrical Equivalent Thermal model, Mathematical Thermal Equivalent Circuit, Coupling of Electrical and Thermal Components, Snubber circuits, Voltage protection by Selenium Diodes and Metaloxide Varistors, Current protection, Fusing, Fault current with AC source, Fault current with DC source, Electromagnetic Interference, sources of EMI, Minimizing EMI Generation, EMI shielding, EMI standards **(Text book 1: 17.2, 17.3, 17.4, 17.5, 17.6, 17.7, 17.8, 17.9)**.

Course outcome (Course Skill Set)

At the end of the course, the student will be able to :

1. Explain different types of industrial power devices such as MOSFET, BJT, IGBT etc, there structure, and its operating characteristics.
2. Design and analyse the power electronic circuits such as switch mode regulators, inverters, controlled rectifiers and ac voltage controllers.
3. Explain various types of MEMs devices used for sensing pressure, temperature, current, voltage, humidity, vibration etc..
4. Familiarize with soft core processors such as ASIC and FPGA.
5. Familiarize with computer hardware, software, architecture, instruction set, memory organization, multiprocessor architecture.
6. Apply protective methods for devices various industrial power devices based on thermal requirements and develop protective methods for the circuits against various electrical parameters.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks

Suggested Learning Resources:

Text Books

1. Power Electronics: Devices, Circuits, and Applications, Muhammad H. Rashid, Pearson, 4th International edition.
2. Fundamentals of Industrial Electronics , Bogdan M. Wilamowski, J. David Irwin, CRC Press, 2011,

Reference Books

1. Thomas E. Kissell, Industrial Electronics: Applications for Programmable Controllers, Instrumentation and Process Control, and Electrical Machines and Motor Controls, 3rd edition, 2003, Prentice Hall.
2. Ned Mohan, T.M. Undeland and W.P. Robbins, "Power Electronics: Converters, Applications and Design", Wiley India Ltd, 2008.

Web links and Video Lectures (e-Resources):

- https://archive.nptel.ac.in/courses/108/102/108102145/
- https://nptel.ac.in/courses/117105082
- https://www.youtube.com/channel/UCKg8GNii0Q-ieXE56AXosGg/featured
- https://www.ieee-ies.org/

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

- Quiz and Seminars

OPERATING SYSTEM		Semester	4
Course Code	BVL405C	CIE Marks	50
Teaching Hours/Week(L:T:P)	3:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	3
Examination type(SEE)	Theory		

Course objectives:

This course will enable students to:

- Understand the services provided by an operating system.
- Explain how processes are synchronized and scheduled.
- Understand different approaches of memory management and virtual memory management. Describe the structure and organization of the file system
- Understand interprocess communication and deadlock situations.

Teaching-Learning Process(General Instructions)

The samples strategies, which the teacher can use to accelerate the attainment of the various course outcomes are listed in the following:

1. Lecturer method (L) need not to be only traditional lecture method, but alternative effective teaching methods could be adopted to attain the outcomes.
2. Use of Video/Animation to explain functioning of various concepts.
3. Encourage collaborative (Group Learning) Learning in the class.
4. Ask at least three HOT (Higher order Thinking) questions in the class, which promotes critical thinking.
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop design thinking skills such as the ability to design, evaluate, generalize, and analyze information rather than simply recall it.
6. Introduce Topics in manifold representations.
7. Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
8. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.

	RBT Level
Module-1	
Introduction to Operating Systems: OS, Goals of an OS, Operation of an OS, Computational Structures, Resource allocation techniques, Efficiency, System Performance and User Convenience, Classes operating System, Batch processing, Multi programming, Time Sharing Systems, Real Time and distributed Operating Systems **(Topics from Sections 1.2, 1.3, 2.2 to 2.8 of Text).**	**L1,L2**
Module-2	
Process Management: OS View of Processes, PCB, Fundamental State Transitions of a process, Threads, Kernel and User level Threads, Non-preemptive scheduling- FCFS and SRN, Preemptive Scheduling- RR and LCN, Scheduling in Unix and Scheduling in Linux **(Topics from Sections 3.3, 3.3.1 to 3.3.4, 3.4, 3.4.1, 3.4.2 , Selected scheduling topics from 4.2 and 4.3 , 4.6, 4.7 of Text)**	**L1,L2, L3**

Module-3	
Memory Management: Contiguous Memory allocation, Non-Contiguous Memory Allocation, Paging, Segmentation, Segmentation with paging, Virtual Memory Management, Demand Paging, VM handler, FIFO, LRU page replacement policies, Virtual memory in Unix and Linux **(Topics from Sections 5.5 to 5.9, 6.1 to 6.3 except Optimal policy and 6.3.1, 6.7,6.8 of Text)**	**L1,L2, L3**
Module-4	
File Systems: File systems and IOCS, File Operations, File Organizations, Directory structures, File Protection, Interface between File system and IOCS, Allocation of disk space, Implementing file access **(Topics from Sections 7.1 to 7.8 of Text).**	**L1,L2**
Module5	
Message Passing and Deadlocks: Overview of Message Passing, Implementing message passing, Mailboxes, Deadlocks, Deadlocks in resource allocation, Handling deadlocks, Deadlock detection algorithm, Deadlock Prevention **(Topics from Sections 10.1 to 10.3, 11.1 to 11.5 of Text).**	**L1, L2**

Course outcome (Course Skill Set)

At the end of the course, students will be able to:

1. Explain the goals, structure, operation and types of operating systems.
2. Apply scheduling techniques to find performance factors.
3. Explain organization of file systems and IOCS.
4. Apply suitable techniques for contiguous and non-contiguous memory allocation.
5. Describe message passing, deadlock detection and prevention methods.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE)is 50%.The minimum passing mark for the CIE is 40%of the maximum marks(20marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- There are 25marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25marks.The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the courses hall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the endof the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20marks.
2. There will be 2questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to50 marks

Suggested Learning Resources:

TEXT BOOKS

Operating Systems – A concept based approach, by Dhamdhere, TMH, 2nd edition.

REFERENCEBOOKS:

1. Operating systems concepts, Silberschatz and Galvin, John Wiley India Pvt. Ltd, 5th edition,2001.
2. Operating system–internals and design system, William Stalling, Pearson Education, 4th ed, 2006.
3. Design of operating systems, Tannanbhaum, TMH, 2001.

Web links and Video Lectures(e-Resources):

- **https://archive.nptel.ac.in/courses/106/105/106105214/**
- **https://onlinecourses.nptel.ac.in/noc20_cs04/preview**
- **https://onlinecourses.nptel.ac.in/noc21_cs72/preview**

Data Structures Using C		Semester	IV
CourseCode	**BVL405D**	CIEMarks	50
TeachingHours/Week(L: T:P: S)	3:0:0:0	SEEMarks	50
TotalHoursofPedagogy	40	TotalMarks	100
Credits	03	ExamHours	03
Examinationnature(SEE)	Theory		

COURSEOVERVIEW:

COURSEOBJECTIVES:

Theobjectivesofthiscourseareto:

1. Developproficiencyin designingandimplementingfundamentaldatastructures.
2. Learnvarioussortingandsearchingalgorithmsandanalyzetheirtime complexity.
3. Understandalgorithmic problem-solvingtechniques,includingrecursion.
4. Exploreadvanceddata structuresliketrees,graphs,andhashtables.
5. Applydata structuresandalgorithmsknowledge tosolve real-worldprogrammingchallengesefficiently.

Teaching-LearningProcess(GeneralInstructions)

These are sampleStrategies,whichteachers canuse toaccelerate theattainmentofthevariouscourseoutcomes.

1. The lecturer's approach (L) does not have to be limited to traditional methods of teaching. Itis possible to incorporate alternative and effective teaching methodsto achieve the desiredoutcomes.
2. Utilizevideosandanimationstoillustratethefunctioning ofdifferenttechniquesusedinthemanufacturingofsmartmaterials.
3. Fostercollaborativelearningexerciseswithintheclassroomtoencouragegroupparticipationandengagement.
4. PoseaminimumofthreeHigherOrderThinking(HOT)questionsduringclassdiscussionstostimulatecriticalthinkingamong students.
5. ImplementProblem-BasedLearning(PBL)asanapproachthatenhancesstudents'analyticalskillsandnurturestheirabilitytodesign,evaluate,generalize,andanalyze information, ratherthansolelyrelyingonrotememorization.

Module-1

Arrays:1D,2D and multidimensional.
Pointers: Definition and Concepts, Arrayof pointers, Structures and unions. Array of structures, pointer arrays, pointer to structures. Passing pointer variable as parameter in functions
Dynamic memory allocation: malloc(), calloc(), realloc() and free function.
Introduction to data structures and algorithms
Text book 1 -Chapter-1.1-1.3 except Rational Numbers.
Text Book 2, chapter-2

Module-2
The Stack – Definition and examples, primitive operations, Example. Representing Stacks in C, Example:Infix,Postfix and Prefix,converting an Expression from Infix to Prefix and Program. Text Book -1-Chapter – 2.1-2.3 Recursion – Recursive Definition and Processes, Recursion in C, Writing Recursive Programs. Recursions - Text Book -1-Chapter – 3.1-3.3
Module-3
Queues and Lists – The Queue and its sequential representation, Linked Lists, Lists in C. Other Lists structures – Circular Lists, Stacks, Queues as circular list. The Josephus problem ,doubly linked lists. Linked lists and Queues - Text Book -1-Chapter – 4.1-4.3,4.5
Module-4
Trees – Binary Trees, binary tree representations, Huffman algorithm, Trees and their applications. Searching – Basic searching Techniques, Tree Searching. Trees - Text Book -1-Chapter – 5.1-5.3,5.5,7.1,7.2
Module-5
Hashing – Introduction, Static Hashing, Dynamic Hashing Text Book 3 -8.1 – 8.3 Graphs - Graph representation, Elementary graph operations, Minimum cost spanning Trees – Kruskal's Algorithm, Prim's algorithm Text Book 3 - 6.1,6.2,6.3.1,6.3.2
CourseOutcomes(COs)(CourseSkillSet) Atthe endofthecourse,thestudent willbe ableto: 1. Masterthe implementationandapplicationofkeydata structuresinprogramming. 2. Demonstratetheabilitytoanalyzealgorithmefficiencyandoptimizecode. 3. Solvecomplex problemsbyapplyingalgorithmicstrategiesand techniques. 4. Designandimplementalgorithmsfortasksinvolvingsearching,sorting,andgraphtraversal. 5. Utilizedatastructuresandalgorithmstoenhancesoftwareperformanceandscalability

AssessmentDetails(bothCIEandSEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) andfortheSEEminimumpassingmarkis35%ofthemaximummarks(18outof50marks).Astudentshallbe deemed to have satisfied the academic requirements and earned the credits allotted to each subject/course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE(ContinuousInternalEvaluation) and SEE(SemesterEndExamination)takentogether.

ContinuousInternalEvaluation:

- FortheAssignmentcomponentoftheCIE,thereare25marksandfortheInternalAssessmentTest component, thereare25 marks.
- Thefirsttestwillbeadministeredafter40-50%ofthesyllabushasbeencovered,andthesecondtestwillbeadministeredafter85-90%ofthesyllabushasbeencovered
- Anytwoassignmentmethodsmentionedinthe22OB2.4,ifanassignmentisproject-basedthenonly one assignment for the course shall be planned. The teacher should not conduct twoassignmentsattheendofthe semesteriftwoassignmentsare planned.
- Forthecourse,CIEmarkswill bebasedonascaled-downsumoftwotestsandothermethodsofassessment.

InternalAssessmentTestquestionpaperisdesignedtoattainthedifferentlevelsofBloom'staxonomyasper theoutcomedefinedforthe course.

Semester-EndExamination(SEE):

TheorySEEwillbeconductedbyUniversityasperthescheduledtimetable,withcommonquestionpapersfor thecourse(**duration03hours).**

1. Thequestionpaperwill havetenquestions.Eachquestionissetfor20marks.
2. There will be 2 questions from each module. Each of the two questions under a module (withamaximumof3 sub-questions),**shouldhaveamixof topics**underthatmodule.

SuggestedLearningResources:

TEXTBOOKS:

1. Data Structures using C and C++, Yedidyah, Augenstein, Tannenbaum, 2nd Edition, Pearson Education, 2007.
2. Data Structures using C, Reema Thareja, 2nd Edition, Oxford University Press, 2011
3. Fundamentals of Data structures in C, 2nd Edition, Horowitz,Sahni, Anderson freed Universities Press,2008

REFERENCEBOOKS:

1. ReemaThareja,Computer fundamentals and programming in C, second edition, Oxford University Press.
2. Gilberg and Forouzan, Data Structures: A Pseudo-code approach with C, 2ndEd,CengageLearning,2014.

WeblinksandVideoLectures(e-Resources):

- https://archive.nptel.ac.in/courses/106/102/106102064/
- https://archive.nptel.ac.in/courses/106/106/106106127/
- https://nptel.ac.in/courses/106102064
- http://elearning.vtu.ac.in/econtent/courses/video/CSE/06CS35.html
- https://nptel.ac.in/courses/106/105/106105171/
- http://www.nptelvideos.in/2012/11/data-structures-and-algorithms.html
- http://elearning.vtu.ac.in/econtent/courses/video/CSE/06CS43.html
- https://nptel.ac.in/courses/106/101/106101060/

ActivityBasedLearning(SuggestedActivitiesinClass)/PracticalBasedlearning

Realworldproblemsolvingusinggroupdiscussion.

- Back/Forwardstacksonbrowsers.
- Undo/RedostacksinExcelorWord.
- Linkedlistrepresentationofreal-worldqueues-Musicplayer,imageviewer
- Realworldproblemsolvingandpuzzlesusinggroupdiscussion.E.g.,Fakecoinidentification,Peasant,wolf,goat,cabbagepuzzle,Konigsbergbridgepuzzleetc.,
- Demonstrationofsolutiontoaproblemthroughprogramming.

AssessmentDetails(bothCIEandSEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is50%. Theminimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to havesatisfied the academic requirements and earned the credits allotted to each course. The student has to secure not lessthan35% (18Marksout of 50) inthesemester-endexamination(SEE).

ContinuousInternalEvaluation(CIE):

CIEmarksfor thepractical course is**50Marks**.

Thesplit-upofCIEmarksforrecord/journalandtestareintheratio **60:40**.

- Each experiment to be evaluated for conduction with observation sheet and record write-up. Rubrics for theevaluation of the journal/write-up for hardware/software experiments designed by the faculty who is handling thelaboratorysessionandismadeknowntostudentsat the beginningof thepractical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up willbeevaluatedfor10marks.
- Totalmarksscoredby thestudentsarescaled downed to30marks(60%of maximum marks).
- Weightagetobegivenforneatnessandsubmissionofrecord/write-upon time.
- Department shall conduct 02 tests for 100 marks, the first test shall be conducted after the 8th week of thesemester andthese testshall beconductedafterthe14thweekofthesemester.
- In each test, write-up, conduction of experiment, acceptable result, and procedural knowledge will carry aweightage of60%andtherest40% forviva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability. Rubricssuggested inAnnexure-IIof Regulationbook
- Theaverage of02testsisscaleddownto **20marks**(40%ofthe maximummarks).

The Sum of scaled-down marks scored in the report write-up/journal and average marks of two tests is the total CIE marksscoredbythestudent.

SemesterEndEvaluation(SEE):

SEEmarksforthepractical courseis50Marks.

SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the UniversityAlllaboratoryexperimentsare to be includedforpracticalexamination.

(Rubrics)Breakupofmarksandtheinstructionsprintedonthecoverpageoftheanswerscripttobestrictlyadheredtoby theexaminers.**OR**based on thecourserequirementevaluation rubricsshallbedecided jointlybyexaminers.

Studentscanpickonequestion(experiment)fromthequestionslotpreparedbytheinternal/externalexaminersjointly.Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners. Generalrubrics suggested for SEE are mentioned here, write up-20%, Conduction procedure and result -60%, Viva-voce 20%of maximum marks. SEEf or practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50marks(however, based oncoursetype, rubricsshallbedecidedbythe examiners)

Change of experiment is allowed only once and 15% Marks allotted to the procedure part to be made zero.

Thedurationof SEEis03hours

Rubricssuggestedin Annexure-IIofRegulationbook

SuggestedLearningResources:

Textbooks:

- Data Structures using C, Reema Thareja, 2nd Edition, Oxford University Press, 2011
- IntroductiontotheDesignandAnalysisofAlgorithms,AnanyLevitin:2ndEdition,2009.Pearson.

- OnlineCourses:
  - Coursera:"Algorithms"byPrincetonUniversity(taughtbyRobertSedgewickandKevinWayne).
  - edX:"AlgorithmicDesignandTechniques"(offeredbyUCSanDiegoandHigherSchoolofEconomics).
- WebsitesandOnlineResources:
  - GeeksforGeeks:Offersawiderangeoftutorials,practiceproblems,andcodingchallengesrelatedtodatastructuresandalgorithms.
  - LeetCode:Providescodingchallengesthatarefrequentlyasked intechnicalinterviewsandcovera

varietyofalgorithmicconcepts.
    - HackerRank:Offerscodingchallengesandcompetitionswithafocusonalgorithmsanddatastructures.
    - Top Coder: Provides algorithmic challenges and competitions for practicing and improving problem-solving skills.
- YouTubeChannels:
    - Mycodeschool:Offersvideotutorialsonvariousdatastructuresandalgorithmstopics.
    - TheCodingTrain:Providesinteractivecodingtutorialsonalgorithmsanddatastructures.
- CodingPlatforms:
    - Code forces: Offers competitive programming challenges to improve algorithmic problem-solving skills.Hackerearth:Providescodingcompetitionsandchallengesalongwithtutorialsandpracticeproblems.

CourseCode	Microcontroller Lab **BVL456A**	CIEMarks	50
TeachingHours/Week(L:T:P)	0:0:2	SEEMarks	50
Credits	01	TotalMarks	100
		ExamHours	2
Examinationtype(SEE)	Practical		

Courseobjectives: Thiscoursewillenablestudentsto:

- UnderstandthebasicprogrammingofMicrocontrollers.
- Developthe8051 Microcontroller-basedprogramsforvariousapplicationsusing Assembly Language & C Programming.
- Program8051Microcontrollertocontrolanexternalhardwareusingsuitable I/Oports.

Note	Execute the following experiments by using Keil Microvision Simulator (any 8051 Microcontroller can be chosen as the target) and Hardware Interfacing Programs using 8051 Trainer Kit.
Sl.No	**I. Assembly Language Programming**
Data Transfer Programs:	
1	Write an ALP to move a block of n bytes of data from source (20h) to destination (40h) using Internal-RAM.
2	Write an ALP to move a block of n bytes of data from source (2000h) to destination (2050h) using External RAM.
3	Write an ALP To exchange the source block starting with address 20h, (Internal RAM) containing N (05) bytes of data with destination block starting with address 40h (Internal RAM).
4	Write an ALP to exchange the source block starting with address 10h (Internal memory), containing n (06) bytes of data with destination block starting at location 00h (External memory).
Arithmetic & Logical Operation Programs:	
5	Write an ALP to add the byte in the RAM at 34h and 35h, store the result in the register R5 (LSB) and R6 (MSB), using Indirect Addressing Mode.
6	Write an ALP to subtract the bytes in Internal RAM 34h &35h store the result in register R5 (LSB) & R6 (MSB).
7	Write an ALP to multiply two 8-bit numbers stored at 30h and 31h and store16- bit result in 32h and 33h of Internal RAM.
8	Write an ALP to perform division operation on 8-bit number by 8-bit number.
9	Write an ALP to separate positive and negative in a given array.
10	Write an ALP to separate even or odd elements in a given array.
11	Write an ALP to arrange the numbers in Ascending & Descending order.
12	Write an ALP to find Largest & Smallest number from a given array starting from 20h & store it in Internal Memory location 40h.
Counter Operation Programs:	
13	Write an ALP for Decimal UP-Counter.
14	Write an ALP for Decimal DOWN-Counter.
15	Write an ALP for Hexadecimal UP-Counter.
16	Write an ALP for Hexadecimal DOWN-Counter.
	II. C Programming
1	Write an 8051 C program to find the sum of first 10 Integer Numbers.
2	Write an 8051 C program to find Factorial of a given number.
3	Write an 8051 C program to find the Square of a number (1 to 10) using Look-Up Table.
4	Write an 8051 C program to count the number of Ones and Zeros in two consecutive memory locations.
	III. Hardware Interfacing Programs
1	Write an 8051 C Program to rotate stepper motor in Clock & Anti-Clockwise direction.
2	Write an 8051 C program to Generate Sine & Square waveforms using DAC interface.

Language/Cprogramsin8051forsolvingsimpleproblemsthatmanipulateinputdatausingdifferentinstructions.

2. Develop Testing and experimental procedures on 8051 Microcontroller, Analyze their operation under different cases.
3. Developprogramsfor8051Microcontrollertoimplementreal worldproblems.
4. DevelopMicrocontrollerapplicationsusingexternalhardwareinterface.

AssessmentDetails(bothCIEandSEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%.Theminimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimumpassing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied theacademic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester EndExamination)takentogether.

ContinuousInternalEvaluation(CIE):

CIEmarksforthepracticalcourseare**50Marks**.

Thesplit-upofCIEmarksforrecord/journalandtestareintheratio**60:40**.

- Each experiment is to be evaluated for conduction with an observation sheet and record write-up. Rubrics fortheevaluationofthejournal/write-upforhardware/softwareexperimentsaredesignedbythefacultywhoishandlingthelaboratorysessionandaremadeknowntostudentsatthebeginningofthepracticalsession.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will beevaluatedfor 10marks.
- Totalmarksscoredbythestudentsarescaleddownto **30marks**(60%ofmaximummarks).
- Weightagetobegivenforneatnessandsubmissionofrecord/write-upontime.
- Departmentshallconductatestof100marksafterthecompletionofalltheexperimentslistedinthesyllabus.
- Inatest,testwrite-up,conductionofexperiment,acceptableresult,andproceduralknowledgewillcarryaweightageof60%andthe rest40%forviva-voce.
- Thesuitablerubricscanbedesignedtoevaluateeachstudent'sperformanceandlearningability.
- Themarksscoredshallbescaleddownto**20marks**(40%ofthemaximummarks).

TheSumofscaled-downmarksscoredinthereportwrite-up/journalandmarksofatestisthetotalCIEmarksscored bythe student.

SemesterEndEvaluation(SEE):

- SEEmarksforthepractical courseare50Marks.
- **SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointedbytheHeadof theInstitute**.
- The examination schedule and names of examiners are informed to the university before the conduction ofthe examination. These practical examinations are to be conducted between the schedule mentioned in theacademiccalendar of the University.
- Alllaboratoryexperimentsaretobeincludedforpracticalexamination.
- (Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to bestrictly adhered to by the examiners.**OR** based on the course requirement evaluation rubrics shall bedecidedjointlybyexaminers.
- Studentscanpickonequestion(experiment)fromthequestionslotpreparedbytheexaminersjointly.
- Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%,Viva-voce20%ofmaximummarks.SEEforpracticalshallbeevaluatedfor100marksandscoredmarksshallbescaleddownto 50marks(however,basedoncoursetype,rubricsshallbedecidedby theexaminers)

Changeofexperimentisallowedonlyonceand15%ofMarksallottedtotheprocedurepartaretobemadezero.Theminimum durationofSEEis02hours

SuggestedLearningResources:

PROGRAMMABLE LOGIC CONTROLLER		Semester	IV
Course Code	**BVL456B**	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	1:0:0:0	SEE Marks	50
Total Hours of Pedagogy	14 to 16 hours	Total Marks	100
Credits	01	Exam Hours	01
Examination type (SEE)	Theory		

Course objectives: This course will enable student to

- To understand the need for automation in the industry with basic controller mechanisms involved.
- To study programming concepts to achieve the desired goal or to define the various steps involved in the automation.
- To understand programming involved with basic subroutine functions.
- To make use of the internal hardware circuits of automation circuit to control the devices during various states by monitoring the timers and counters.
- To handle the data of the I/O devices to interface the data with the controller andauxiliary devices.

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

1. Lecture method (L) does not mean only traditional lecture method, but different type of teaching methods may be adopted to develop the outcomes.
2. Show Video/animation films to explain evolution of communication technologies.
3. Encourage collaborative (Group) Learning in the class.
4. Ask at least three HOTS (Higher order Thinking) questions in the class, which promotes critical thinking.
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.
6. Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
7. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.

Module-1

Introduction: Programmable logic controller (PLC), role in automation (SCADA), advantages and disadvantages, hardware, internal architecture, sourcing and sinking**(Textbook 1:1.1 to 1.4)**

I/O devices and Processing: list of input and output devices, examples of applications. I/O processing, input/output units, signal conditioning, remote connections, networks, processing inputs I/O addresses. **(TextBook1: 2.1 to 2.3 and 4.1 to 4.7).**

Module-2

Programming: Ladder programming- ladder diagrams, logic functions, latching, multiple outputs, entering programs, functional blocks, program examples like location of stop and emergency switches. (**TextBook1: 5.1 to 5.7).**

Module-3

Programming Methods: Instruction Lists- Ladder programs and Instruction lists, Branch codes, Programming Examples- Signal lamp-valve operation task. Sequential Function Charts- Branching and convergence. **(TextBook1: 6.1 to 6.3).**

Module-4

Internal Relays: ladder programs, battery-backed relays, one-shot operation, set and reset, master control relay (**TextBook1: 7.1 to 7.6).**

Timers and counters: Types of timers, ON and OFF- delay timers, pulse timers, forms of counter, programming, up and down counters. **(TexBook1: 9.1 to 9.6).**

Module-5

Shift register and data handling: shift registers, ladder programs, registers and bits, data handling, arithmetic functions. **(TextBook1: 11.1 to 11.2 and 12.1 to 12.3)**

Course outcome (Course Skill Set)

At the end of the course, the student will be able to :

1. Describe the PLC and how to construct PLC ladder diagrams.
2. Illustrate an application with programming.
3. Describe characteristics of registers and conversion examples.
4. Apply PLC functions to timing and counting applications.
5. Analyse the analog operation of PLC and demonstrate the robot applications with PLC.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned.
- The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 01 hours).**

1. SEE paper shall be set for 50 questions, each of the 01 marks. The pattern of the question paper is MCQ (multiple choice questions).
2. The time allotted for SEE is 01 hour. The student has to secure a minimum of 35% of the maximum marks meant for SEE.

Suggested Learning Resources:

Textbooks:

1. Programmable Logic controllers-W Bolton, 5th edition/6th edition, Elsevier- newness, 2009/2015.
2. Programmable logic controllers - principles and applications"-John W. Webb, Ronald A Reiss, Pearson education, 5th edition, 2007.

Reference Books:

1. Programmable Logic Controllers"- E. A Paar, 3rd Edition, An Engineers Guide. Newness, 2003.
2. "Introduction to Programmable Logic Controller"- Garry Dunning, 3rd Edition, Thomson Asia Pte Ltd. Publication, 2006
3. "PLCs & SCADA - Theory and Practice"- Rajesh Mehra, Vikrant Vij, 2nd Edition, Laxmi publication, 2017
4. "PLC Programming for Industrial Automation"- Kevin Collins, 1st Edition, Kindle, 2016

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning.

- Quiz and Seminars

Octave Programming			
CourseCode	BVL456C	CIEMarks	50
TeachingHours/Week(L:T:P:S)	0:0:2	SEEMarks	50
TotalHoursofPedagogy	12Sessions	Total	100
Credits	01	ExamHours	03

**AdditionalOnehourmaybeconsideredforinstructionsif required*

Courseobjectives:

- ApplytheoreticalknowledgeofOctave programming topracticalprogrammingtasks.
- Gain hands-on experience in implementing and debugging octave Programming through coding exercisesand projects.

CourseSyllabus :

BasicdatastructuresinOctave – Vectors,Matrices,CellArrays.Specialvecors.Linearsamplingandlogarithmicsampling.Accessingelementsofvectors,matrices,andmatrices.Mathematicaloperationsonvectorsandmatrices.Addition,Multiplication,Subtraction,Division,Power,Square-Root,trigonometricoperations.DotProductsandCrossProductsofVectors.Matrixmultiplication,matrixinverseandmatrixtransposeoperations.Findingeigenvaluesandvectorsofasquarematrix.Findingthesolutionofasystemoflinearequations.Linearprogrammingandintegerlinearprogrammingusingglpk.PlottinginOctave.Subplots,StemPlots,SemilogandLog-logplots.PackagesinMatlab – symbolic,signalprocessing,control.ApplicationsofOctavetosolveproblemsinElectricalengineering,Electronicsengineering,ControlSystems,SignalsandSystems/SignalProcessing.

Sl..NO	Experiments

1	(a) Definethefollowingmatrices usingOctave
	i. A4x4identitymatrix
	ii. A 4x4matrixofzeros
	iii. A 4x4matrixofones
	iv. ThematrixU4definedbelow.
	`1 2 3 4`
	`2 3 1 4`
	`1 3 2 4`
	`4 3 1 2`
	v. MatrixD4definedbelow. Itisalso calledthe Hadamardmatrixof dimension4.
	`1 1 1 1`
	`1 -1 1 -1`
	`1 1 -1 -1`
	`1 -1 -1 1`
	vi. MatrixH4 definedbelow
	$\mathbf{H}_4 = \frac{1}{\sqrt{4}}\begin{bmatrix} 1 & 1 & 1 & 1 \\ 1 & 1 & -1 & -1 \\ \sqrt{2} & -\sqrt{2} & 0 & 0 \\ 0 & 0 & \sqrt{2} & -\sqrt{2} \end{bmatrix}$
	vii. A4x4magic squareG4
	viii. A4x4matrixofrandom numbersselectedfromthe range {-1,0,1}.
	ix. A4x4matrixofrandomnumbersinthe range0to 1.
	(b)

(ii) Findthe transposeofU4.

(iii) Multiply D4 by its transpose and obtain the resulting matrix. How is related tothe identifymatrix?

(iv) Findtheinverseof H4 andverify thatit istheinverse.

(v) What isthe determinantofD4?

(vi) Extractthediagonalelements ofH4.

(vii) HowcanyoureshapetheelementsofD4 intoa 2x8matrix?

(viii) What is the magic sum of a 4x4 matrix? How can you verify that G4 is indeed amagicsquare?

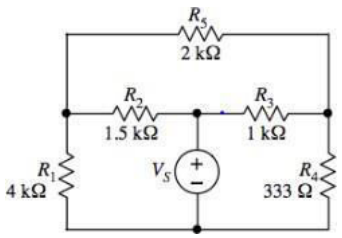
(ix) The matrix D4 mentioned above is a 4x4 matrix. We wish to extract the sub-matrix consisting of rows 1 and 4 and columns 1 and 4. [In other words, thefourcornersofD4.)ShowOctave codeforgeneratingthesubmatrixSM.

(x) Checkifthe H4andD4 areorthogonalmatrices.

2

YouwillhavelearntKirchhoff'scurrentandvoltagelawsto solvethevoltagesandcurrentsin aDCcircuit.Given a circuit with n loops, we can write down n equations in n unknowns (loop currents). Alternately,givenacircuitwithnnodes,wecanwritedownnequationsinn unknowns(nodevoltages).Theselinearequationscan besolved usingOctave.

(a) WritedowntheKCLandKVLforthefollowingcircuitandsolvethenodevoltagesandcurrents.Assumethat Vsis100V.

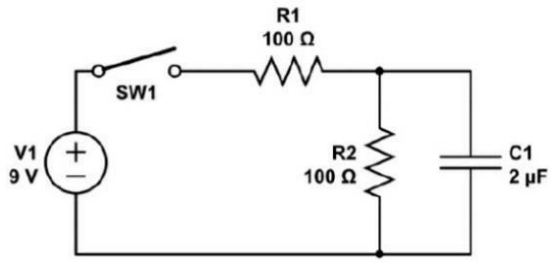
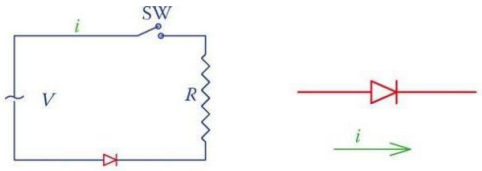


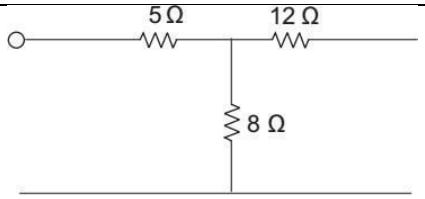
(b) Findthetotalpowerdissipatedinthecircuit.

(c) Findthetotalpowersuppliedbythevoltagesource.

(d) Challenge – Instead of hardcoding the values of the resistors and the voltage source, can you allowthe user to input R1, R2, R3, R4, R5, and Vs? Develop a complete Octave script which reads in thevaluesofcircuitparametersandprintsthenodevoltages,nodecurrents,andpowerdissipation.

(e) Variations of the above exercises can be given to the students.For example, a resistor can beincluded in series with Vs. Alternately, a different circuit from a text book can be given. You can alsochange the problem by specifying the current through one of the resistors and asking the user tosolvefor Vs.

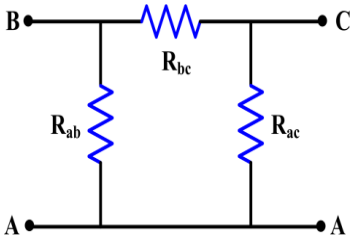
3	(a) Consider the RC circuit shown in the figure below. Plot the voltage across C and the chargingcurrentthroughC when theswitch isturned on. (b) What isthe risetimeofthecapacitorvoltage? 
4	 (a) The figure shows a diode-based rectifier.The diode conducts only when the input voltage is positive.Assume that it is an ideal diode. Plot the half-wave rectified waveform if the input to the rectifier is a 50-Hzsinewaveof200VRMS.Plottheoutputwaveformfor fourcyclesoftheinput. (b) FindtheaverageoftheHalfwave-rectifiedoutputinOctaveandverifyyouranswerusingtheformulafortheaverageoutput. (c) Plottheoutputofafull-wave rectifier. (d) FindtheRMSvalueoftheFullwave-rectifiedoutputinOctaveandverifyyouranswerusingtheformulafortheRMSvalue. (e) Assume that the input voltage is 2sin(500t)V and that the diode has a cut-in voltage of 0.6V.Plot thehalf-waveandfull-waverectifiedwaveformsand findtheiraverageandRMSvalues.
5	Youhavestudiedthatanyperiodicsignaloffrequencyfcanbedecomposedintoasumofsineandcosinewaveforms whose frequencies ae integral multiples of f.The resulting series is called the Fourier series.Considerthefollowingequation. $$x(t) = 4/\pi \times \sum_{k=1}^{n} [\![sin\,(2\pi f(2k-1)t)]\!]$$ (a) WriteanOctaveprogramtoreadfandnandplotx(t).Whatdoesx(t)resemble? (b) Howcanyoumodifyx(t)togenerateasquarewaveformoffrequencyf,butwhoseamplitudegoesfrom0to 2? (c) Generatex(t)assumingthatthesquarewavegoesfrom-1to1andhasafrequencyof1kHz.Take100samplesineachperiod.PerformanFFTanalysisofx(t).



enYparameters,obtaintheZparametersusingafunctioncalledY2Z()

(b) FindtheZandYparametersfortheT-network

(c) FindtheZandYparametersfortheDelta.Assumethatallresistorsare15Ohms.



(d) FindtheT-equivalentoftheDeltanetworkabove.

(e) FindtheT-equivalentoftheDeltanetworkabove. LettheTnetworkhavetheresistors Zb,Zc,Za.

7

(a) Representthenumber65asanunsignedintegerusingfewestnumberofbits
(b) Representthenumber-65asasignedmagnitudeintegerusingthefewestnumberofbits
(c) Representthenumber-65asaone'scomplementnumberusingfewestnumberofbits
(d) Representthenumber-65asatwo'scomplementnumberusingthefewestnumberofbits
(e) Representthenumber1965inhexadecimal
(f) FindthedecimalequivalentofthehexadecimalnumberABCDh
(g) Assumethat"10010101"isabinarynumber.Interpretitasanunsignednumberandconvertittodecimal.
(h) Memoryisorganizedintermsofbytes.Whena32-bitnumberisreadfromamemory,4byteshavetoberead.SupposethebytesarestoredasfollowsatlocationAinthememory.Inthelittle-endianrepresentation, the bytes will be organized into a 32-bit register as shown. Write a function whichconvertsa32-bitnumberfrombig-endiantolittle-endianformat.

MEM LOC M	00h
MEM LOC M+1	01h
MEM LOC M+2	02h
MEM LOC M+3	03h
MEM LOC M+4	04h
…	…

03	02	01	00

LittleEndian

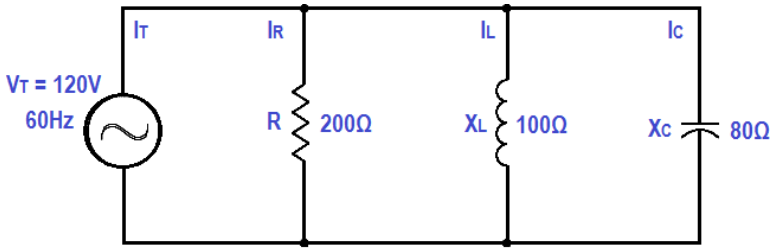
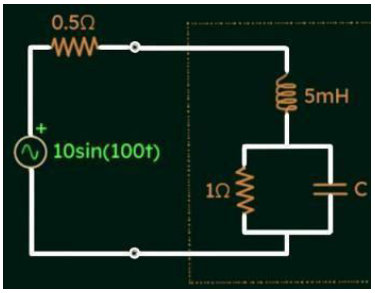
02 03

00 01

BigEndian

8 AseriescircuitconsistsofresistanceR,inductanceLandcapacitanceC.AsinusoidalvoltageofVsin(wt)isapplied to the series circuit. Assume V=100. Plot the current in the circuit and the input voltage for thefollowingcases.

(a) w=1000,R=5ohm,L=1mH,C=200uF;isthecurrentleadingorlagging?Whatisthepowerdissipationinthecircuit?
(b) w=10000,R=5ohm,L=1mH,C=200uF;isthecurrentleadingorlagging?Whatisthepowerdissi

	(c) Theresonantfrequencyw0,R=5ohm,L=1mH,C=200uF.Whatisthephasedifferencebetweenthevoltageandcurrent?Whatisthevalueofw?Whatisthepowerdissipation? Writeafunctiontoplotthevoltageandcurrent.TaketheinputsR,L,andCfromtheuser.
9	(a) ConsiderthecircuitshownbelowanddeterminetheinductanceLandcapacitanceC. (b) PlottheimpedanceoftheRLCcircuitshowninthefigureasthefrequencyisvariedfrom0to10kHz. (c) Findtheresonantfrequencyfromtheplot  (a) Parallel RLC Circuit
10	 Findthe valueofcapacitorCtomaximizethepowertransferredtothe load.(Theloadincludestheinductance.) **Courseoutcomes(CourseSkillSet):** Attheendofthecoursethestudentwillbeableto: ● Developproficiencyinoctave codinganddebuggingcomplexprogram flow. ● Understand the concepts of Matrices and apply the octave programming concepts to solve the Matrices. ● Acquire practical knowledge and apply the octave programming skills to solve Electric circuits. ● Develop aOctave program to analyze the continuous and discrete signals ● Understand the concept memory and to represent data and address using Octave Programming.
	AssessmentDetails(bothCIEandSEE) The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is50%. Theminimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to havesatisfied the academic requirements and earned the credits allotted to each course. The student has to secure not lessthan35% (18Marksout of 50) inthesemester-endexamination(SEE). **ContinuousInternalEvaluation(CIE):** CIEmarksfor thepractical course is**50Marks**. Thesplit-upofCIEmarksforrecord/journalandtestareintheratio **60:40**. • Each experiment to be evaluated for conduction with observation sheet and record write-up. Rubrics for theevaluation of the journal/write-up for hardware/software experiments designed by the faculty who is handling thelaboratorysessionandismadeknowntostudentsat the beginningof thepractical session

willbeevaluatedfor10marks.

- Totalmarksscoredby thestudentsarescaled downed to30marks(60%of maximum marks).
- Weightagetobegivenforneatnessandsubmissionofrecord/write-upon time.
- Department shall conduct 02 tests for 100 marks, the first test shall be conducted after the 8th week of thesemester andthese testshall beconductedafterthe14thweekofthesemester.
- In each test, write-up, conduction of experiment, acceptable result, and procedural knowledge will carry aweightage of60%andtherest40% forviva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability. Rubricssuggested inAnnexure-IIof Regulationbook
- Theaverage of02testsisscaleddownto **20marks**(40%ofthe maximummarks).

The Sum of scaled-down marks scored in the report write-up/journal and average marks of two tests is the total CIE marksscoredbythestudent.

SemesterEndEvaluation(SEE):

SEEmarksforthepractical courseis50Marks.

SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the UniversityAlllaboratoryexperimentsare to be includedforpracticalexamination.

(Rubrics)Breakupofmarksandtheinstructionsprintedonthecoverpageoftheanswerscripttobestrictlyadheredtoby theexaminers.**OR**based on thecourserequirementevaluation rubricsshallbedecided jointlybyexaminers.

Studentscanpickonequestion(experiment)fromthequestionslotpreparedbytheinternal/externalexaminersjointly.Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners. Generalrubrics suggested for SEE are mentioned here, write up-20%, Conduction procedure and result -60%, Viva-voce 20%of maximum marks. SEEf or practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50marks(however, based oncoursetype, rubricsshallbedecidedbythe examiners)

Change of experiment is allowed only once and 15% Marks allotted to the procedure part to be made zero.

Thedurationof SEEis03hours

Rubricssuggestedin Annexure-IIofRegulationbook

SuggestedLearningResources:

Textbooks:

Dr. P.J.G. Long, Department of Engineering University of Cambridge, "Introduction to Octave," can be downloaded from octavetut.pdf (cam.ac.uk)

DataStructuresLab using C			
CourseCode	BVL456D	CIEMarks	50
TeachingHours/Week(L:T:P:S)	0:0:2	SEEMarks	50
TotalHoursofPedagogy	15Sessions	Total	100
Credits	01	ExamHours	03

AdditionalOnehourmaybeconsideredforinstructionsif required

Courseobjectives:

- Applytheoreticalknowledgeofdatastructuresandalgorithmstopracticalprogrammingtasks.
- Gain hands-on experience in implementing and debugging data structures and algorithms through coding exercisesand projects.

Sl..NO	Experiments
1	Write a C Program to create a Student record structure to store, N records, each record having the structure shown below: USN, Student Name and Semester. Write necessary functions a. To display all the records in the file. b. To search for a specific record based on the USN. In case the record is not found, suitable message should be displayed. Both the options in this case must be demonstrated. (Use pointer to structure for dynamic memory allocation)
2	Write a C Program to construct a stack of integers and to perform the following operations on it: a. Push b. Pop c. Display The program should print appropriate messages for stack overflow, stack underflow, and stack empty.
3	Write a C Program to convert and print a given valid parenthesized infix arithmetic expression to postfix expression. The expression consists of single character operands and the binary operators + (plus), - (minus), * (multiply) and / (divide).
4	Write a C Program to simulate the working of a queue of integers using an array. Provide the following operations: a. Insert b. Delete c. Display
5	Write a C Program using dynamic variables and pointers to construct a stack of integers using singly linked list and to perform the following operations: a. Push b. Pop c. Display The program should print appropriate messages for stack overflow and stack empty.
6	Write a C Program to support the following operations on a doubly linked list where each node consists of integers: a. Create a doubly linked list by adding each node at the front. b. Insert a new node to the left of the node whose key value is read as an input c. Delete the node of a given data, if it is found, otherwise display appropriate message. d. Display the contents of the list. (Note: Only either (a,b and d) or (a, c and d) may be asked in the examination)
7	Write a C Program a. To construct a binary search tree of integers. b. To traverse the tree using all the methods i.e., inorder, preorder and postorder. c. To display the elements in the tree.
8	Write recursive C Programs for a. Searching an element on a given list of integers using the Binary Search method. b. Solving the Towers of Hanoi problem.
9	Write a program to traverse a graph using BFS method. Write a program to check whether given graph is connected or not using DFS method.
10	Design and develop a program in C that uses Hash Function H:K->L as H(K)=K mod m(reminder method) and implement hashing technique to map a given key K to the address space L. Resolve the collision (if any) using linear probing

Note: The students must be encouraged to create Leetcode account and work on Leetcode platform to improve the competency.

Courseoutcomes(CourseSkillSet):

Attheendofthecoursethestudentwillbeableto:

- Developproficiencyincodinganddebuggingcomplexalgorithmsanddatastructures.
- Acquire practical problem-solving skills by applying data structures and algorithms to real-world programmingchallenges.
- Develop a C program to perform arithmetic operation using data structure and operators.
- Understand the concept of graph theory and develop a C program for searching an element.
- Develop a C program to check the given graph is connected using different algorithms.

AssessmentDetails(bothCIEandSEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is50%. Theminimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to havesatisfied the academic requirements and earned the credits allotted to each course. The student has to secure not lessthan35% (18Marksout of 50) inthesemester-endexamination(SEE).

ContinuousInternalEvaluation(CIE):

CIEmarksfor thepractical course is**50Marks**.

Thesplit-upofCIEmarksforrecord/journalandtestareintheratio **60:40**.

- Each experiment to be evaluated for conduction with observation sheet and record write-up. Rubrics for theevaluation of the journal/write-up for hardware/software experiments designed by the faculty who is handling thelaboratorysessionandismadeknowntostudentsat the beginningof thepractical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up willbeevaluatedfor10marks.
- Totalmarksscoredby thestudentsarescaled downed to30marks(60%of maximum marks).
- Weightagetobegivenforneatnessandsubmissionofrecord/write-upon time.
- Department shall conduct 02 tests for 100 marks, the first test shall be conducted after the 8th week of thesemester andthese testshall beconductedafterthe14thweekofthesemester.
- In each test, write-up, conduction of experiment, acceptable result, and procedural knowledge will carry aweightage of60%andtherest40% forviva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability. Rubricssuggested inAnnexure-IIof Regulationbook
- Theaverage of02testsisscaleddownto **20marks**(40%ofthe maximummarks).

The Sum of scaled-down marks scored in the report write-up/journal and average marks of two tests is the total CIE marksscoredbythestudent.

SemesterEndEvaluation(SEE):

SEEmarksforthepractical courseis50Marks.

SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the UniversityAlllaboratoryexperimentsare to be includedforpracticalexamination.

(Rubrics)Breakupofmarksandtheinstructionsprintedonthecoverpageoftheanswerscripttobestrictlyadheredtoby theexaminers.**OR**based on thecourserequirementevaluation rubricsshallbedecided jointlybyexaminers.

Studentscanpickonequestion(experiment)fromthequestionslotpreparedbytheinternal/externalexaminersjointly.Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners. Generalrubrics suggested for SEE are mentioned here, write up-20%, Conduction procedure and result -60%, Viva-voce 20%of maximum marks. SEEf or practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50marks(however, based oncoursetype, rubricsshallbedecidedbythe examiners)

Change of experiment is allowed only once and 15% Marks allotted to the procedure part to be made zero.

Thedurationof SEEis03hours

Rubricssuggestedin Annexure-IIofRegulationbook

SuggestedLearningResources:

Textbooks:

- Data Structures using C, Reema Thareja, 2nd Edition, Oxford University Press, 2011
- IntroductiontotheDesignandAnalysisofAlgorithms,AnanyLevitin:2ndEdition,2009.Pearson.

- OnlineCourses:
  - Coursera:"Algorithms"byPrincetonUniversity(taughtbyRobertSedgewickandKevinWayne).
  - edX:"AlgorithmicDesignandTechniques"(offeredbyUCSanDiegoandHigherSchoolofEconomics).
- WebsitesandOnlineResources:
  - GeeksforGeeks:Offersawiderangeoftutorials,practiceproblems,andcodingchallengesrelatedtodatastructuresandalgorithms.

  - LeetCode:Providescodingchallengesthatarefrequentlyasked intechnicalinterviewsandcovera

varietyofalgorithmicconcepts.
    - HackerRank:Offerscodingchallengesandcompetitionswithafocusonalgorithmsanddatastructures.
    - Top Coder: Provides algorithmic challenges and competitions for practicing and improving problem-solving skills.
- YouTubeChannels:
    - Mycodeschool:Offersvideotutorialsonvariousdatastructuresandalgorithmstopics.
    - TheCodingTrain:Providesinteractivecodingtutorialsonalgorithmsanddatastructures.
- CodingPlatforms:
    - Code forces: Offers competitive programming challenges to improve algorithmic problem-solving skills.Hackerearth:Providescodingcompetitionsandchallengesalongwithtutorialsandpracticeproblems.