ವಿಶ್ವೇಶ್ವರಯ್ಯ ತಾಂತ್ರಿಕ ವಿಶ್ವವಿದ್ಯಾಲಯ
ವಿಟಿಯು ಅಧಿನಿಯಮ ೧೯೯೪ರ ಅಡಿಯಲ್ಲಿ ಕರ್ನಾಟಕ ಸರ್ಕಾರದಿಂದ ಸ್ಥಾಪಿತವಾದ ರಾಜ್ಯವಿಶ್ವವಿದ್ಯಾಲಯ
VISVESVARAYA TECHNOLOGICAL UNIVERSITY
State University of Government of Karnataka Established as per the VTU Act, 1994"JnanaSangama"
Belagavi-590018, Karnataka, India

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REF: VTU/BGM/BEC613D/700/2024-25/5762

DATE: 11 FEB 2025

CIRCULAR

Subject: BEC613D-FPGA System Design using Verilog updated Syllabus regarding

Reference: Chairperson BoS ECE VTU email dated 17.01.2025

Dear Sir/Madam,

This is with reference to the subject mentioned above. Based on feedback from stakeholders, the Chairperson, Board of Studies (BoS) in ECE, VTU Belagavi, has updated the syllabus for BEC613D—FPGA System Design using Verilog and corrected typographical errors.

A copy of the revised syllabus is attached for your reference.

All Principals of Engineering Colleges and Chairpersons/Program Coordinators of University Departments are hereby informed to disseminate this information to all concerned and update the syllabus content accordingly.

Encl: BEC613D Syllabus.

11/02/25

Registrar

To,

The Principals of affiliated and Constituent Engineering Colleges are under the ambit of the university.

The Chairpersons/Program Coordinator, university Department, at Kalburgi, Mysuru, Belagavi and Bengaluru

Copy to

1. The Registrar (Evaluation) VTU Belagavi for information and needful
2. The Director, ITI SMU VTU Belagavi, for information and to make arrangements to upload the circular on the VTU web portal for stakeholders' reference.
3. The Special Officer, QPDS section for information and needful
4. Office Copy

FPGA System design Using Verilog		Semester	VI
Course Code	BEC613D	CIE Marks	50
Teaching Hours/Week (L:T:P:S)	3:0:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	03
Examination type (SEE)	Theory		

Course objectives:

This course will enable students to:

- Understand the types of programmable logic devices and building blocks of FPGA and thus implement the design using Xilinx FPGAs.
- Understand the concepts of Advanced Logic design and implementation using Verilog HDL
- Designing different Digital applications using SM chart.

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

1. Lecture method (L) does not mean only the traditional lecture method, but a different type of teaching method may be adopted to develop the outcomes.
2. Show Video/animation films to explain the functioning of various techniques.
3. Encourage collaborative(Group)Learning in the class
4. Ask at least three HOTS(Higher-order Thinking) questions in the class, which promotes critical thinking.
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.
6. Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
7. Discuss how every concept can be applied to the real world and when that's possible, it helps improve the students' understanding.
8. Adopt the Flipped class technique by sharing the materials/Sample Videos before the class and having discussions on the topic in the succeeding classes.

Module-1

Introduction to Programmable Logic Devices:

Brief overview of Programmable Logic Devices, Simple Programmable Logic Devices (SPLDs) Complex Programmable Logic devices (CPLDs), Field-Programmable Gate Arrays (FPGAs)

(Text 1: 3.1,3.2 ,3.3,3.4) **RBT Level:** L1, L2, L3

Module-2

Advanced Digital Design Examples:

BCD to 7-Segment Display Decoder, BCD Adder, Traffic Light Controller, Synchronization and debouncing, Shift-and-Add Multiplier, Array Multiplier, Keypad Scanner (Excluding Test Bench)

(Text 1:4.1, 4.2, 4.4, 4.7,4.8, 4.9,4.11) **RBT Level:** L1, L2, L3

Module-3
SM Charts and Microprogramming : State Machine Charts, Derivation of SM Charts, SM chart for binary multiplier, Dice Game (Excluding Test Bench), Realization of SM Charts, Implementation of the Dice Game. Microprogramming, Linked State Machines. **(Text 1: 5.1, 5.2, 5.3 , 5.4 , 5.5 , 5.6)** **RBT Level:** L1, L2, L3
Module-4
Floating-Point Arithmetic: Representation of Floating-Point Numbers, Floating-Point Addition, Other Floating-Point Operations. Multi valued Logic and Signal Resolution, Built-in Primitives, User-Defined Primitives, SRAM Model, Rise and Fall Delays of Gates, Model for SRAM Read/Write System, Rise and Fall Delays of Gates **(Text 1:7.1,7.3,7.4, 8.3, 8.4, 8.5,8.6 8.7,8.8)** **RBT Level:** L1, L2, L3
Module-5
Designing with Field Programmable Gate Arrays: Implementing Functions in FPGAs, Implementing Functions Using Shannon's Decomposition, Carry Chains in FPGAs, Cascade Chains in FPGAs , Examples of Logic Blocks in Commercial FPGAs ,Dedicated Multipliers in FPGAs, FPGAs Capacity: Maximum gates versus Usable gates, Design Translation. **(Text 1: 6.1,6.2,6.3, 6.4,6.5 , 6.7, 6.10, 6.11) RBT Level:** L1, L2, L3
Course outcome (Course Skill Set) At the end of the course the student will be able to: 1. Apply the concept of Programmable logic devices to implement digital design. 2. Design and implementation of Advanced logic design using Verilog HDL 3. Understand the concept of SM Chart and design complex digital circuits using SM Chart. 4. Performing the Floating-point arithmetic operations and designing of Memories 5. Designing and performance evaluation of advanced digital design using FPGAs

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks.
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks).
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course **(duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks.

Suggested Learning Resources:

Text Book:

1. Digital Systems Design Using Verilog, First Edition, Charles H. Roth, Jr. The University of Texas at Austin, Lizy Kurian John, The University of Texas at Austin, Byeong Kil Lee, The University of Texas at San Antonio.

Reference Books:

1. Advanced FPGA Design Architecture, Implementation, and Optimization Steve Kilts Spectrum
2. ASIC and FPGA Verification: A guide to component Modelling. Richard Munden, Morgan Kaufmann Publishers is an imprint of Elsevier.
3. Processor Design, System-on-Chip Computing for ASICs and FPGAs, Jari Nurmi Finland Tampere University of Technology Sringer Publications.
4. The design Warrior's guide to FPGA Clive 'Max' Maxfield Elsevier Publications

ActivityBasedLearning(SuggestedActivitiesinClass)/Practical-Based Learning

- Group Discussion/Quiz.
- Demonstration of Verilog and FPGA concepts.
- Case Study on small design and implementation on FPGA's.